DIAGRAMS AND CIRCUIT DESCRIPTION

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).

Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

Abbreviations are based on ANSI Y1.1-1972.

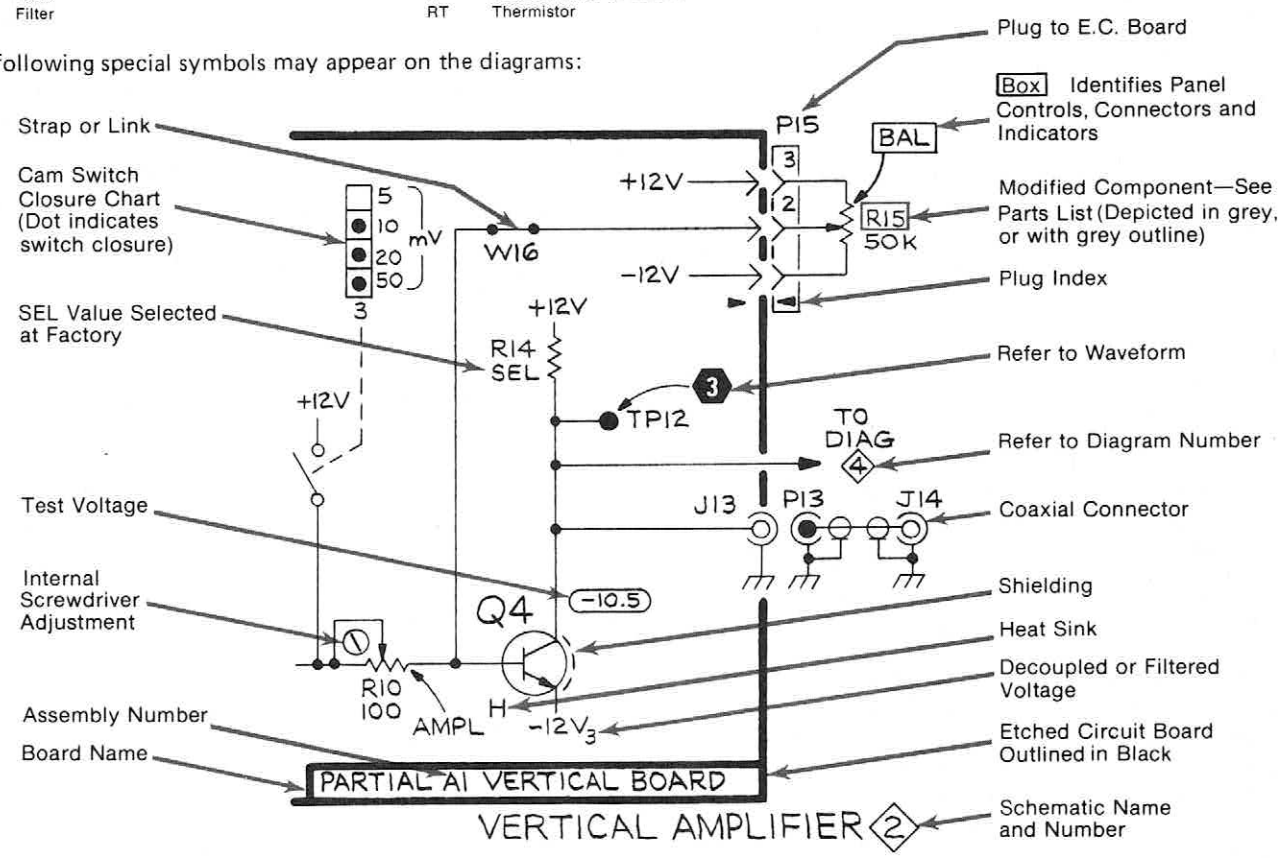
Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc)	H	Heat dissipating device (heat sink, heat radiator, etc)	S	Switch or contactor
AT	Attenuator, fixed or variable	HR	Heater	T	Transformer
B	Motor	HY	Hybrid circuit	TC	Thermocouple
BT	Battery	J	Connector, stationary portion	TP	Test point
C	Capacitor, fixed or variable	K	Relay	U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
CB	Circuit breaker	L	Inductor, fixed or variable	V	Electron tube
CR	Diode, signal or rectifier	M	Meter	VR	Voltage regulator (zener diode, etc.)
DL	Delay line	P	Connector, movable portion	W	Wirestrap or cable
DS	Indicating device (lamp)	Q	Transistor or silicon-controlled rectifier	Y	Crystal
E	Spark Gap, Ferrite bead	R	Resistor, fixed or variable	Z	Phase shifter
F	Fuse	RT	Thermistor		
FL	Filter				

The following special symbols may appear on the diagrams:



BLOCK DIAGRAM DESCRIPTION

VERTICAL INPUT

Signals to be displayed on the crt are applied to either the channel 1 (Y) or channel 2 input connector. The input signals are amplified by the preamplifier circuits. Each preamplifier circuit includes separate input coupling, attenuators, gain switching, variable attenuators, balance, and gain adjustments.

A Trigger Pickoff circuit in each channel supplies a sample of the vertical input signal to the Trigger Input Amplifier via the Trigger Switching circuit and the SOURCE switch.

VERTICAL SWITCHING

The Vertical Mode switch selects which channel supplies the trigger signal. The vertical signal passes through the Input Buffer Amplifier circuit which isolates the preamplifier circuits from the Delay Line Driver. The output of each Input Buffer Amplifier is connected to the Delay Line Driver through a Diode Gate circuit. The Diode Gate circuits are controlled by the Vertical Switching circuit to select the channel(s) to be displayed. An output from the Vertical Switching circuit (through the Chop Blanking Pulse Generator) is connected to the Z Axis Amplifier to blank switching transients in the chop mode (SEC/DIV at 1 ms or slower). A sync pulse from the sweep (via the Alternate Sync Pulse Amplifier) switches the display between channels at the end of each sweep in the alternate mode (SEC/DIV at .5 ms or faster).

VERTICAL AMPLIFIER

The vertical input signal goes from the Delay Line Driver through the Delay Line to the Vertical Output Amplifier. The Delay Line provides approximately 200 ns delay in the vertical signal. This allows the sweep generator circuit time to initiate a sweep before the vertical signal reaches the crt vertical deflection plates. The Vertical Output Amplifier provides final amplification of the signal to drive the crt vertical deflection plates. One section of the BEAM FINDER switch, when pressed, causes the display to compress vertically to aid in locating off-screen displays. Another section affects the horizontal circuitry.

TRIGGER

The Trigger circuit produces a logic triggering signal to trigger the sweep. Trigger signals are selected by the SOURCE switch from three sources: external trigger (via the External Trigger Input Buffer circuit), vertical amplifier input signal (internal), or the line voltage at the secondary of T700. (No trigger signal is produced during X-Y operation.)

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The selected trigger signal is amplified and inverted by the Trigger Input Amplifier. The trigger signal passes through coupling capacitor, C2132, to the Trigger Level Comparator, which determines the voltage level (on the trigger waveform) at which triggering occurs. The SLOPE switch determines whether the sweep triggers on the positive-going or negative-going portion of the trigger signal. A Schmitt trigger circuit produces the logic trigger signal.

SWEEP AND HORIZONTAL AMPLIFIER

The Sweep circuit, when triggered by the Trigger circuit, produces a linear sawtooth output signal to the Horizontal Amplifier. The slope of the sawtooth is controlled by the SEC/DIV switch. When the sawtooth output reaches a predetermined level, the Holdoff circuit resets the Sweep circuit, blanks the crt (through the Z Axis Amplifier) and prevents subsequent triggers from initiating another sweep until the sweep reset is completed.

The sawtooth output from the Sweep circuit is amplified by the Horizontal Output Amplifier circuit to produce horizontal deflection on the crt. When the SOURCE switch is in the X-Y position, the X signal, from the External Trigger Input Buffer, is applied to the Horizontal Amplifier. One section of the BEAM FINDER switch, when pressed, causes the display to compress horizontally to aid in locating off-screen displays.

CRT CIRCUIT

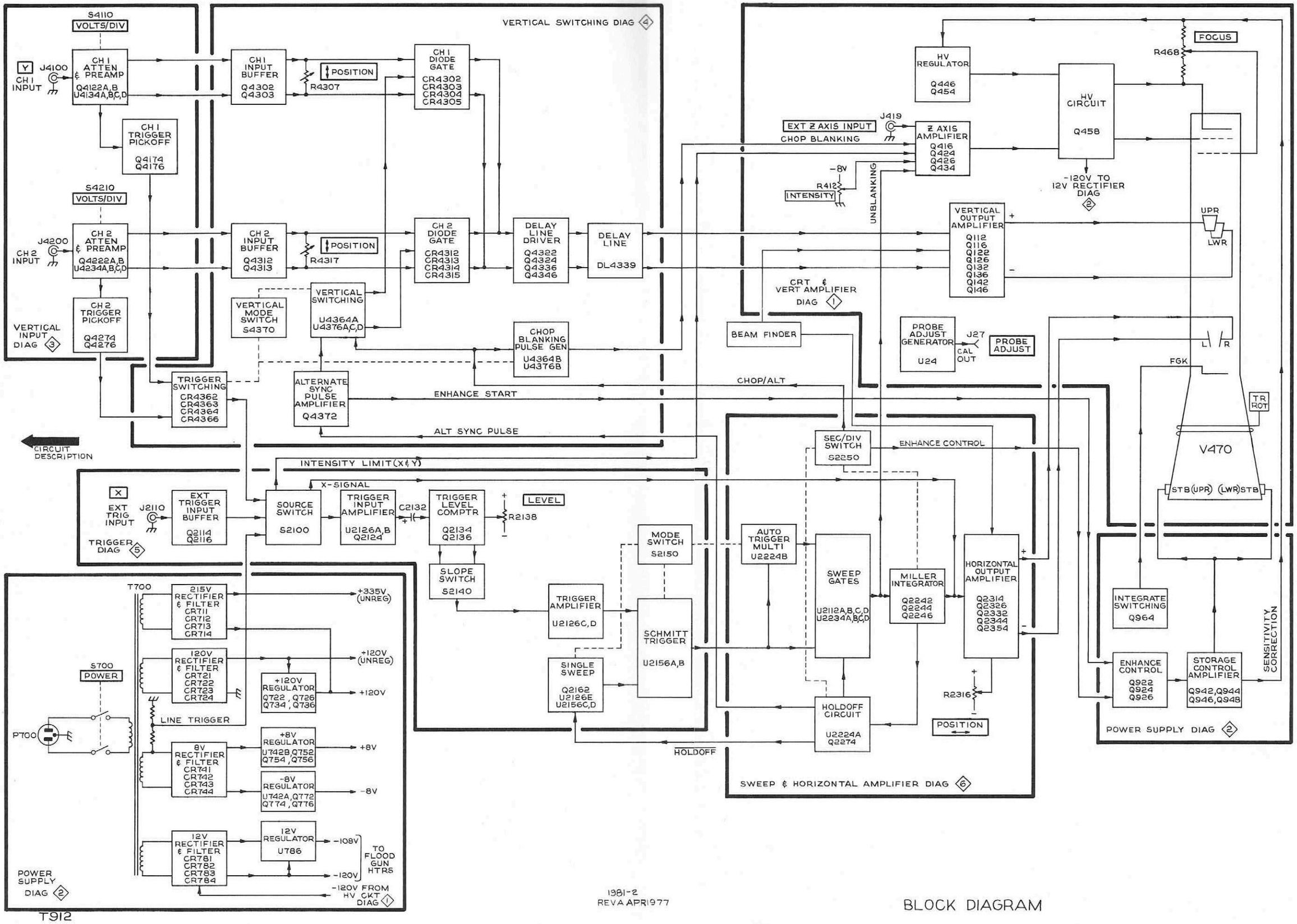
The Z Axis Amplifier determines the crt intensity and blanking. The Z Axis Amplifier sums the current inputs from several sources: INTENSITY control, X-Y intensity limit, unblanking signal from sweep circuit, chop blanking signal from the Vertical Switching circuit, and EXT Z AXIS INPUT connector, J419.

Output of the Z Axis circuit controls the trace intensity through the HV circuit. The HV circuit provides the voltages (greater than 100 V) necessary for operation of the crt.

The Probe Adjust Generator provides a square-wave voltage output for checking voltage probes.

POWER SUPPLY AND STORAGE

The Power Supply circuits provide the low-voltage power necessary for operation of the instrument. The Storage circuit provides the voltages and controls necessary to store waveforms. The ENHANCE control circuit increases the writing rate in single sweep. The INTEGRATE switching circuit allows successive sweeps to build up a charge on the crt storage grid so very fast waveforms can be stored.



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BLOCK DIAGRAM

CRT & VERT AMPL CIRCUIT DESCRIPTION

PROBE ADJUST

The Probe Adjust circuit provides an output of approximately 0.5 V peak-to-peak negative from ground at approximately 1 kHz.

When the output (pin 6) of U24 is positive, the voltage divider, R22-R23, sets pin 3 at a positive voltage. Feedback through R24 charges C24 until the pin 2 level reaches the same positive voltage as pin 3. When pin 3 and pin 2 are at the same voltage, U24 output (pin 6) switches from positive to negative. The output of U24 is about 7.2 V either positive or negative. Then C24 starts charging negative. When pin 2 and pin 3 are at the same voltage again, U24 output (pin 6) switches positive, and the cycle repeats.

During the positive half cycle, CR26 is forward biased and CR27 is reverse biased, keeping the output at ground level. During the negative half cycle, CR26 is reverse biased and CR27 is forward biased, causing current to flow from ground through R27, CR27 and R26 to −8 V. This sets the output level to approximately −0.5 V.

VERTICAL OUTPUT AMPLIFIER

The vertical output amplifier circuit provides final amplification for the signal to drive the vertical deflection plates of the crt.

The vertical output amplifier consists of two push-pull cascode amplifier stages. The first stage consists of Q112-Q116, Q122-Q126, and associated circuitry, and the second stage consists of Q132-Q136, Q142-Q146 and associated circuitry. Adjustment R126 adjusts the gain to compensate for variations in the sensitivities of different crt's.

Components R102, C102, R133, and C133 provide high frequency compensation. Series peaking coils LR138 and LR148 are used to improve the bandwidth of the last stage.

When BEAM FINDER button S410A is pressed, R131 is added to the resistance at the emitters of Q132 and Q142, limiting the current.

This limits the maximum vertical deflection to within the crt screen area. Another section of the BEAM FINDER switch limits the horizontal deflection.

Z AXIS CIRCUIT

The Z Axis Amplifier controls the crt intensity level from several inputs: the INTENSITY control, unblanking signal from the sweep circuit, chop blanking signal from the vertical amplifier, and external signals from the EXT Z AXIS INPUT connector (also intensity limit signal during X-Y operation). The INTENSITY control, R412, varies the trace intensity from off to maximum brightness, overriding all other inputs to the Z Axis Amplifier. The unblanking signal from the sweep circuit blanks the signal during retrace and holdoff. The chop blanking signal (with the vertical in the DUAL TRACE chop mode) blanks the crt during the channel switching interval to eliminate vertical chopping noise from appearing on the display. The EXT Z AXIS INPUT connector, through J419, allows control of the trace intensity from an external source.

The current signals from the various inputs are connected to the emitter of Q416. The algebraic sum of the signals determines the collector conduction level. In case of overdrive from any input, Q416 cuts off and CR416 conducts the excess current to ground and thereby prevents the output stage from saturating.

Transistors Q424, Q426, Q434, and associated circuitry form an inverting operational amplifier. Components R423 and C423 are the feedback elements. Any current into the input summing point, the base of Q424, results in an output voltage at the collectors of Q426 and Q434. This output voltage controls the display intensity level by changing the dc voltage level at the junction of R462, C463, and C464.

HIGH VOLTAGE OSCILLATOR

Transistor Q458 and associated circuitry make up the high-voltage oscillator that produces the drive for high-voltage transformer T460. When the instrument is turned on, current through Q454 provides forward bias for Q458. Transistor Q458 conducts and the collector current increases, which develops a voltage across the primary (Q458 collector) winding of T460. This produces a corresponding voltage increase in the feedback winding of T460, which is connected to the base of Q458, and Q458 conducts even harder. Eventually the rate of collector current increase in Q458 becomes less than that required to maintain the voltage across the collector winding, and the output voltage drops. This turns off Q458 by way of the feedback voltage to the base. The voltage waveform at the collector of Q458 is a sine wave at the resonant frequency of T460. During the negative half cycle, Q458 remains off and the field collapses in the primary of T460. When the field is collapsed sufficiently, the base of Q458 becomes forward biased into conduction again and the cycle begins anew. The amplitude of sustained oscillation depends upon the average current delivered to the base of Q458 by the regulator circuitry. The frequency of oscillation is approximately 50 kHz. Components C458 and R458 decouple the unregulated +120 V supply line.

HIGH-VOLTAGE REGULATOR

Transistors Q446-Q454 and associated circuitry control the output voltage of the High Voltage supply. Components R443 and C443 provide a slow start up for the high-voltage oscillator. When the instrument is turned on, the +120 V supply charges C443 through R443. The voltage increases until it is sufficient to forward bias CR443, holding the voltage at slightly above +8 volts. This forms the reference for the high-voltage regulator.

The resulting current in R444A (100 μA) turns on Q446 and Q454, providing base current for Q458. This starts the high voltage oscillator, causing a negative voltage to develop at the crt cathode.

Resistors R444B, C, D, and R468 sample the cathode voltage. The high voltage increases until the cathode voltage is −2700 V. At this point the current in R444B is approximately the same as the current in R444A with Q446 barely conducting.

Any change in the level at the base of Q446 produces an error signal at the collector of Q446, which is amplified by Q454 and applied to the base of Q458 through the feedback winding of T460. Regulation occurs as follows:

If the cathode voltage at the −2700 V point starts to go positive (less negative), this positive-going change is applied to the base of Q446. Q446 conducts harder, which in turn causes Q454 to conduct harder. This results in greater bias current to the base of Q458 through the feedback winding of T460. Now, Q458 is biased closer to its conduction level so that it comes into conduction sooner to produce a larger induced voltage in the secondary of T460. This increased voltage appears as a more negative voltage at the crt cathode to correct the original positive-going change. By sampling the output from the crt cathode supply in this manner, the total output of the high-voltage supply is held relatively constant.

Components R446, R453, R459, C457 and R457 help prevent instabilities in the high-voltage oscillator.

HIGH VOLTAGE RECTIFIERS AND OUTPUT

The high voltage transformer, T460, has 2 output windings. One winding is rectified by CR465 to produce the dc voltage for the crt cathode. Components C465, R465, and C466 filter the dc voltage. Two taps on this winding provide power for the storage circuitry. Components CR468 and C467 rectify and filter the −220 V supply. Components CR467, C468, C469 and R469 rectify and filter the −120 V supply. The crt filament is referenced to the cathode voltage by R466, thereby preventing cathode to filament breakdown.

A second winding is used to control the crt intensity. Components CR463, C462, C463, C464, R462, and R463 rectify and filter the secondary voltage to provide approximately −2785 V which is applied to the crt grid. The entire winding is referenced to the output of the Z Axis Amplifier whose output voltage variations are used to control the crt intensity by varying the grid to cathode voltage. The dc path for the Z Axis signal to the grid is through R462, CR463, R463 and the transformer winding. Resistor R462 isolates the transformer capacitance from the Z Axis Amplifier. Capacitors C463 and C464 provide a path for fast changes in the Z Axis output to the crt grid. Resistor R464 provides a discharge path for C462, C463, and C464. Glow lamps DS463 and DS465 prevent the grid-to-cathode voltage from rising high enough to cause breakdown within the crt during turn-on or when the cathode or grid is shorted to ground.

CRT CONTROL CIRCUITS

Crt display focus is controlled by FOCUS control R468. ASTIG adjustment R477, which is used in conjunction with the FOCUS control to provide a well-defined display, varies the voltage on the astigmatism grid.

Trace Rotation adjustment R472 controls the current through L472 and affects both vertical and horizontal rotation of the trace by varying the magnetic field around the crt. Components R478 and C478 decouple the first accelerator electrode from the +120 V supply.

VOLTAGE CONDITIONS

Voltages shown on this schematic diagram were measured with a TEKTRONIX DM 501 Digital Multimeter. Voltage measurements can vary as much as ±20%. No signals were applied to the vertical input or the X (external trigger) input. See waveform conditions for T912 control settings.

WAVEFORM CONDITIONS

Waveforms below were monitored with a TEKTRONIX 7704A Oscilloscope, 7B71 Time Base, 7A15 Amplifier, and 10X probe. The oscilloscope input coupling was set to ac. Waveforms may vary as much as ±20%.

A 1 kHz, 50 mV sine wave was applied to CH 1 input and a 1 kHz, 50 mV square wave was applied to CH 2 input. A TEKTRONIX FG 501 Function Generator provides either of the input waveforms.

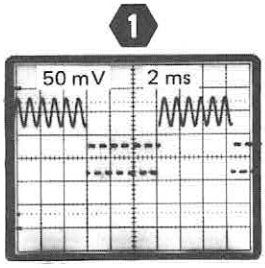
The T912 controls were set as follows:

VOLTS/DIV (both)	20 mV
AC-GND-DC (both)*	DC
Vertical Mode	DUAL TRACE
SOURCE	INT
MODE	AUTO
SLOPE	+OUT
SEC/DIV*	.5 ms
STORE*	Nonstore (button OUT)

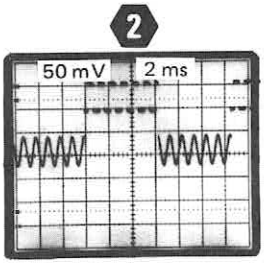
The other controls were set as needed to obtain a display.

The CH 1 POSITION control was adjusted so that the bottom of the sine wave on the first horizontal graticule line above the center and the CH 2 POSITION control was adjusted so that the top of the square wave was on the first horizontal graticule line below the center.

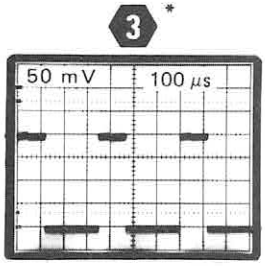
*For waveforms 3 and 4, the SEC/DIV switch was set to 20 μs, the AC-GND-DC controls were set to GND, and the STORE button was set to store (button in).



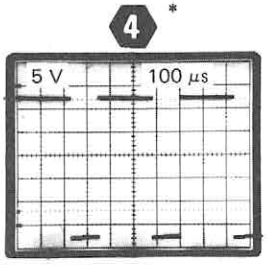
WAVEFORM POSITIONS VARY WITH POSITION CONTROL SETTING



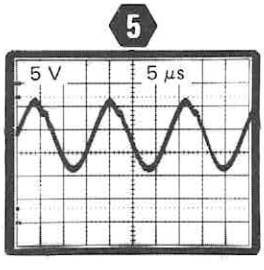
WAVEFORM POSITIONS VARY WITH POSITION CONTROL SETTING

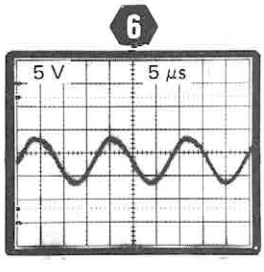


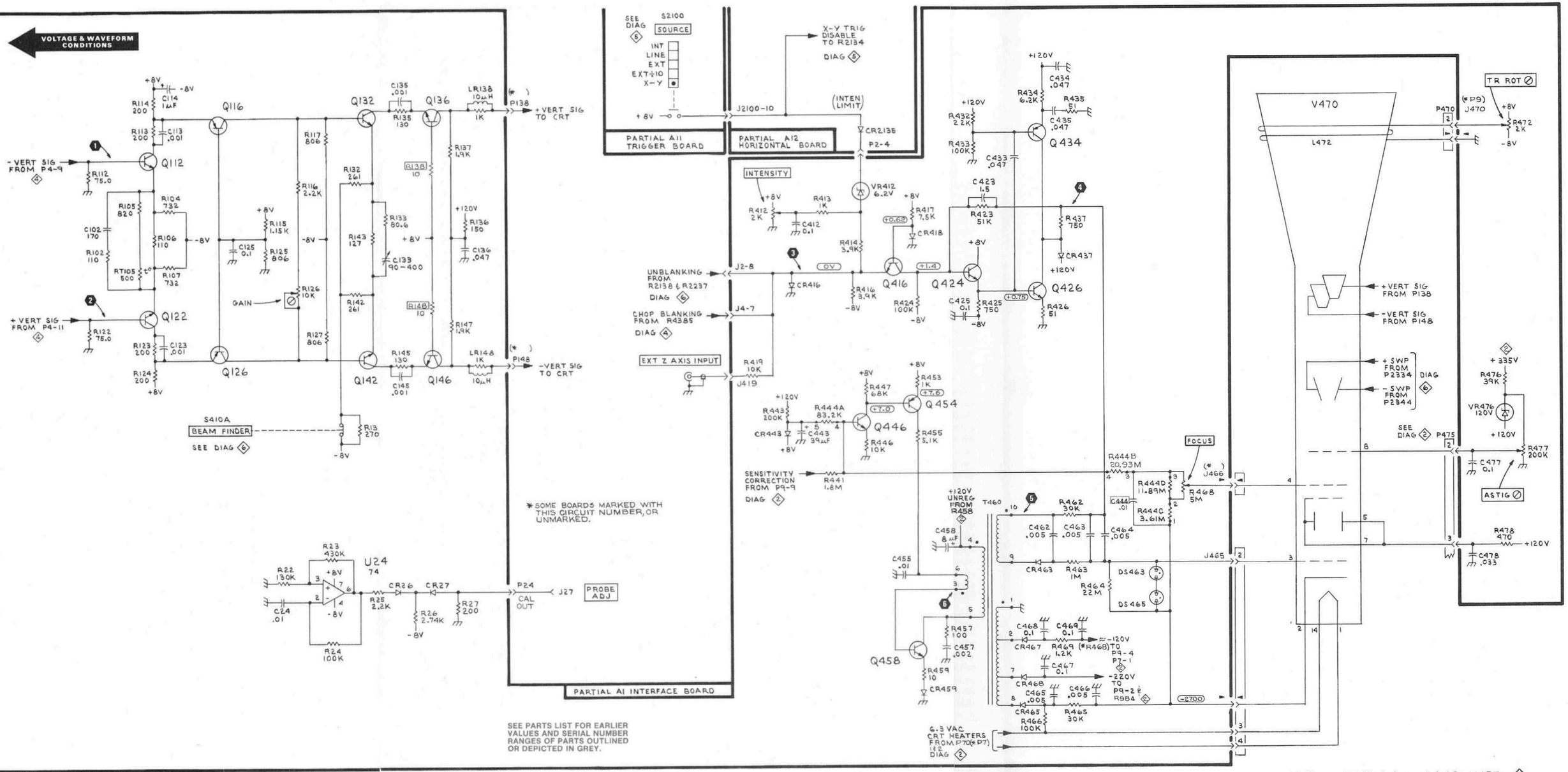
AMPLITUDE AND PULSE WIDTH VARY WITH INTENSITY AND SEC/DIV SETTINGS



AMPLITUDE AND PULSE WIDTH VARY WITH INTENSITY AND SEC/DIV SETTINGS







CRT & VERTICAL AMPLIFIER 4

POWER SUPPLY & STORAGE CIRCUIT DESCRIPTION

POWER INPUT

Ac power is applied to the primary of T700 through line fuse F700, POWER switch S700, Line Selector switch S701, and Range Selector switch S705.

The Line Selection switch, S701, connects the split primary windings of T700 in parallel for 120 V operation or in series for 240 V. When changing the nominal line voltage, also change the line fuse. See parts list for correct fuse values.

The Range Selector switch, S705, selects either LO (100 or 220 V) or HI (120 or 240 V) nominal line-voltage range.

SECONDARY CIRCUITS

The secondary circuit supplies three regulated voltages: −8 V, +8 V, and +120 V.

Operational amplifiers U742B (+8 V supply) and U742A (−8 V supply) have differential inputs that monitor output voltage variations and provide correction signals to the series-regulating transistors. For example, suppose the +8 volt supply drops. This negative change is coupled to the inverting input of U742B through sense resistor R756, causing pin 7 to go positive. Since the voltage across VR746 remains essentially constant, Q754 and Q756 follow this change and raise the output voltage back to +8 volts. In the +120 volt supply, Q726 acts as the feedback amplifier with its base being the inverting input. The regulating action is the same as in the +8 and −8 volt supplies. Zener diode, VR762, provides a 5 volt reference for the −8 V supply, which in turn provides the reference for the +8 and +120 V supplies. The series regulating elements in the +120 V and +8 V supplies are transistors Q734-Q736 and Q754-Q756. The series regulating element in the −8 V supply is a modified Darlington configuration consisting of Q774 and Q776. Current limiting circuits provide short-circuit protection for each regulated supply. The following describes the +8 V current-limiting circuit. The other current-limiting circuits operate similarly.

In the +8 V supply, Q752 is normally biased off. Under normal conditions, the base of Q752 is set at about +8 V. As the supply current increases, the voltage drop across R754 increases. Since the Q756 emitter-base diode voltage difference remains constant, the increasing voltage on Q756 emitter due to the R754 voltage drop causes a corresponding increase at the base of Q756. This voltage is applied to voltage divider R752 and R753, causing the base of Q752 to go more positive. When the supply current increases sufficiently beyond the normal operating current, Q752 turns on. The collector of Q752 moves in the negative direction, which begins turning off Q754-Q756 and creates a foldback condition. (see Fig. 7-1). Transistor Q756 continues to conduct some current when the supply is limited, dropping enough voltage across R754 to keep Q752 biased on.

A +335 volt unregulated supply is provided for the storage circuit. This supply is stacked on top of the +120 volt regulated supply.

A regulated 12.6 volt dc supply is provided for the flood gun heaters. The supply output is referenced to −120 volts (from high-voltage power supply). Regulator U784 provides the regulation.

Current divider, R741, R742, R2102, provides a sample of the line voltage for line triggering.

POWER-ON LAMP CIRCUIT

The ON lamp, DS796, remains on as long as the line voltage does not vary more than approximately 10% from the nominal selected line voltage (100, 120, 220, or 240 V). When the line voltage is not within the 10% limit, the ON lamp blinks.

As long as Q796 is conducting, DS796 remains on. If Q796 is biased off, DS796 goes out, allowing C796 to charge through R796 and R797. When C796 reaches about 80 V, it discharges through DS796, causing it to turn on momentarily. Capacitor C796 again is charged through R796-R797 and discharged through DS796. This cycle repeats, causing the ON lamp to blink until the line voltage is within the 10% limit and Q796 conducts.

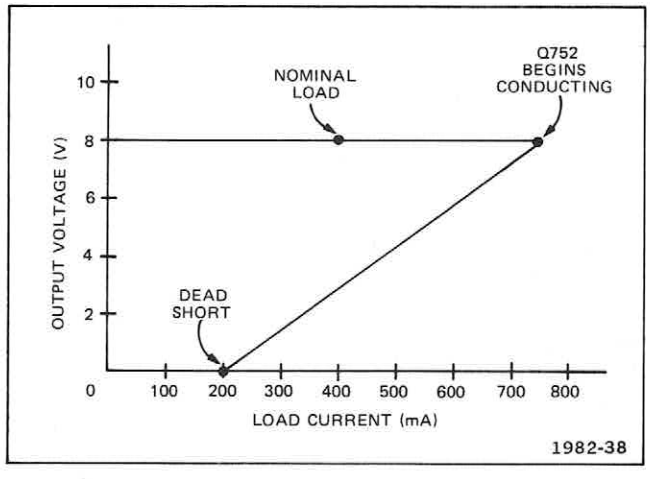


Fig. 7-1. Foldback circuit action.

When the 120 V unregulated supply at voltage divider R792 and R793 increases to more than about 10% above the nominal value, Q792 turns on and Q796 turns off, causing DS796 to blink. When the 120 V unregulated supply at voltage divider R794 and R795 decreases to less than about 10% below the nominal value, Q796 turns off, causing DS796 to blink.

STORAGE CIRCUITS

Storage is the retention on the crt screen of a displayed event. The T912 employs a direct-view bistable storage cathode ray tube. T912 Storage functions include Store, Integrate, Enhance, and Erase. In addition to the basic writing gun elements, which allow conventional oscilloscope operation when the storage circuitry is inactive, a bistable storage crt contains several additional elements to provide the storage functions. A storage screen contains a special coated surface that continues to emit light when bombarded by electrons from a flood gun when the surface has been written by the writing gun and shifted to the stored state. The flood gun is a low-energy electron gun that directs a large cone of electrons toward the entire crt screen. Collimation electrodes shape the flood spray for uniform coverage of the storage target.

The Storage Circuitry provides the voltages to operate the flood guns, collimation electrodes, and storage target backplates (STB). The T912 crt contains upper and lower backplates, which are connected externally to operate as a single plate. An Erase circuit produces a waveform to erase stored written information. The Enhance Generator permits storing of fast single sweeps, and the INTEGRATE switch provides a stored image from a number of repetitive sweeps, each of which would be too fast to store alone as a single event.

The control amplifier, consisting of Q948, Q946, Q944, and Q942, determines the crt storage target (STB) voltage level. The control amplifier operates as a shunt feedback stage with an emitter follower in the output. The current into the bases of Q942 and Q944 controls the voltage output at the emitters of Q946 and Q948. The high voltage is divided by R946 and R945 so that about half of it is across Q948 and the rest across Q946. Resistors R944 and R943 divide the voltage across Q944 and Q942.

During nonstore operation, the voltage across R915 adds enough current to the bases of Q944 and Q942 to saturate them. The storage target backplate (STB) is held at the same potential as the crt storage cathode (pin 6). In the store mode, R934 sets the level on the STB terminals by adjusting the current into the bases of Q944 and Q942. During storage, the voltage level on the STB electrodes (ENHANCE LEVEL R926 fully ccw) is approximately +60 V, depending on the setting of R934 Store Level control.

Pushing ERASE button S910A changes the voltage applied to R914 from −120 V to −220 V, thus applying a more negative voltage to the bases of Q942 and Q944, reducing base current and decreasing conduction. This creates a positive going pulse at the Q946 emitter, which is applied to the STB terminals causing the entire crt screen to illuminate (flood). The crt screen remains flooded as long as the ERASE button is held in. When the ERASE button is pushed in, and the voltage at the R912-R914 junction changes to −220 V; CR912 is biased on and C912 assumes a charge of 100 V (−120 V on positive plate and −220 V on negative plate). When the ERASE button is released, the −220 V at R914 is removed and C912 discharges through R913. This applies a positive going voltage to the bases of Q942 and Q944, which increases base current and emitter to collector conduction; this produces a negative-going transition at the STB terminals, which erases stored written information. As C912 discharges, the storage target returns to the storage level.

The Enhance circuit allows the stored writing rate for single sweep to be increased about ten times. The Enhance circuit is enabled only when the MODE switch is is SINGLE SWP. When the MODE switch is in AUTO or NORM, +8 V is applied to R922 which forces Q922 off and Q924 on. Setting the MODE switch to SINGLE SWP allows the P9 pin 10 side of R922 to float. The Enhance circuit is than activated by the negative-going pulse at the end of each sweep. Capacitor C923 differentiates this pulse. The differentiated pulse turns Q922 on, and Q924 off, which turns Q926 on. The current through Q926 produces a negative voltage coupled through C926 to the base of Q922 and holds Q922 on. The circuit stays in this state until C926 discharges far enough for Q922 to turn back off. While Q924 is off, less current will flow through R932, resulting in a positive pulse on the storage target. The pulse width varies from about 0 to 4 ms, depending on the setting of ENHANCE LEVEL control R926. A single sweep that is too fast for the crt to store will result in a charge on the storage target that is below the writing threshold of the crt. A positive pulse (enhance pulse) immediately following this single sweep can raise the charged area of the storage target above the writing threshold. In this manner, the effective writing rate is increased.

When the INTEG button is pressed, Q964 is turned off and the flood gun cathode floats. This allows repetitive sweeps to build up a charge on the storage target. Each sweep adds to the charge until the writing threshold is reached. When the button is released, Q964 saturates and the flood gun cathode returns to −120 V. Those crt target areas that charged up to the writing threshold now appear as a stored image.

VOLTAGE CONDITIONS

Voltages shown on this schematic diagram were measured with a TEKTRONIX DM 501 Digital Multimeter. Voltage measurements can vary as much as ±20%. No signals were applied to the vertical input or the X (external trigger) input. See waveform conditions for T912 control settings.

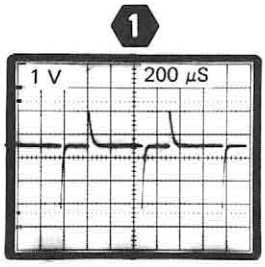
WAVEFORM CONDITIONS

Waveforms below were monitored with a TEKTRONIX 7704A Oscilloscope, 7B71 Time Base, 7A15 Amplifier, and 10X probe. The oscilloscope input coupling was set to ac. Waveforms may vary as much as ±20%.

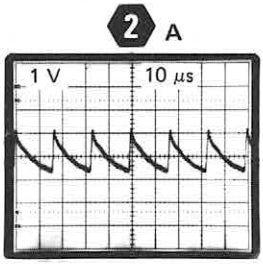
The T912 controls were set as follows:

SEC/DIV	20 μs/div
STORE	Store (button in)
AC-GND-DC (both)	GND
SOURCE	INT
MODE	AUTO

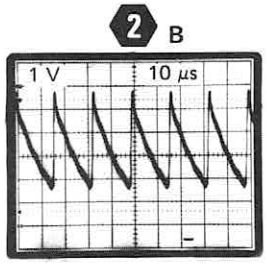
The other controls were set as needed to obtain a display.



AMPLITUDE VARIES
WITH ENHANCE
CONTROL SETTING



ERASE BUTTON OUT



PRESS AND HOLD
ERASE BUTTON IN

VOLTAGE & WAVEFORM CONDITIONS

S701 LINE VOLTAGE SELECTOR

S705 (RANGE)

120V LOW 240V HIGH

F700 1.0 A FAST

POWER S700

P700

brn blu

SAFETY EARTH GROUNDED TO MAIN CHASSIS

grn-yel

T912

T700

CR711 CR713 CR712 CR714 C712 10μF R712 1M

CR721 CR722 CR723 CR724 C722 100μF R722 47K

P720 B720 C720 5μF

Q734 Q736 Q722 (*CR722) CR732 R732 1.0K (*) R733 64.9K CR734 R734 10

R726 100K Q726

F722 0.15A

P7-2 TO R476 ◇1 +335V

P7-4 +120V (UNREG) R458 (*) R458 51 TO T460 PIN 4 ◇1 +120V (UNREG)

P7-3 +120V

CR738 C738 3.3μF R736 118K CR737 R737 8.06K -8V

R741 390 R742 56K CR742 CR741 CR744 CR743 C742 2200μF C743 2200μF

U742B 1/2 5558 R745 4.3K R746 1K C746 .01 VR746 9.1V

+120V (UNREG) R747 100K Q754 Q756 Q752 R752 221 R753 2.43K R754 0.75Ω CR758 C758 100μF R756 8.51K C756 .01 R757 8.51K

P7-8 R2102 1.5K LINE TRIGGER TO P2-1 DIAG ◇5 C2102 0.1

P7-9

P7-11

P7-5 +8V

C801 1μF +8V TO J2-3 & P9-7

P7-7

U742A 1/2 5558 R772 4.53K R773 1K R774 2.55K C774 .01 C778 100μF R764 2.43K R765 221 Q772 Q774 Q776 R775 0.75Ω CR778 VR762 5.1V R762 560 R763 1.8K C763 .01 CR764 CR765 R766 390

P7-6 -8V

(*P7) P70 6.3 VAC CRT HEATER TO V470 DIAG ◇1

U784 7800 P784 CR781 CR784 CR782 CR783 C782 2200μF CR786 12.6V TO FLOOD GUN HEATERS V470 THIS DIAG

P7-1 -120V FROM T460 DIAG ◇4

A2 LOW VOLTAGE POWER SUPPLY BOARD

(*P470) J9 +335V +120V +8V -8V -120V -220V FROM T460 DIAG ◇4 TO R984

ALTERNATE WIRING ON SOME BOARDS CR952 VR951 R951 P950-1,-8 P950-3

S915 STORE

S910A ERASE

-120V -220V R912 1.3K C912 0.5μF R913 130K R914 150K CR912

R915 75K

ENHANCE START PULSE FROM J4-4 DIAG ◇4 C923 .001 R923 162K R924 25.5K Q922 Q924 R925 3.65K R928 100 C928 0.1

ENHANCE CONTROL FROM J2-5 DIAG ◇5 Q926 C926 .056 R922 8.2K R927 20K R930 25K ENHANCE PULSE HEIGHT R926 20K R932 107K R933 39K CR932 R934 50K

ENHANCE LEVEL STORE LEVEL

S910B INTEG

R962 130K R961 360K

VR964 110V R964 10K Q964 C964 220μF R963 100K C963 1μF

SENSITIVITY CORRECTION TO R441 DIAG ◇1

A3 STORAGE BOARD

+335V R946 68K Q948 R945 68K Q946 +121.6 +44.8 +44.4 R951 47K VR951 TP945 CR945 +19.3 R944 100K Q944 -81.4 R943 100K Q942 -51.0 CR943 R954 50K R953 82K CR952 C953 .02 R955 47K COLLIMATION 2 +120V R957 50K +32.0 COLLIMATION 1

P950 STB (UPPER) STB (LOWER) V470 CE-5 CE-3 CE-2 CE-1 FLOOD GUN ANODE J982 wh-yel +120V R982 50K GEOMETRY

FLOOD GUN BIAS -120V R984 500K -220V +154.0 SEE DIAG ◇4 P475 4 9,12 J9(*P470) 6

12.6V FROM P784 THIS DIAG -120V 10 11

PARTIAL A1 INTERFACE BOARD

+120V (UNREG) C796 1μF (POWER) ON DS796 R796 100K R797 2M Q796 R794 137K R795 8.66K +120V (UNREG) R792 169K R793 8.66K -8V Q792

* SOME BOARDS MARKED WITH THIS CIRCUIT NUMBER, OR UNMARKED.

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

SEE PARTS LIST FOR SEMICONDUCTOR TYPES.

REV.A, APR 1977
1981-6

POWER SUPPLY & STORAGE ◇2

VERT INPUT CIRCUIT DESCRIPTION

Since Channel 1 and Channel 2 vertical input circuits are identical, only Channel 1 is discussed in detail. The 4100 series circuit numbers identify the Channel 1 components and 4200 series numbers identify the Channel 2 components.

INPUT COUPLING SWITCH

Vertical input signal is ac-coupled, dc-coupled, or grounded by S4100. In the DC position, the input signal is coupled directly to the VOLTS/DIV switch attenuator. In the AC position, the input signal passes through C4102 to the attenuator. In the GND position, the signal path from the input connector to the attenuator is grounded through C4102-R4102. This provides a ground reference without disconnecting the signal from the input connector. In the GND position, C4102 is charged to the average signal level through R4102 so that the trace remains on screen when S4100 is changed to the AC position.

VOLTS/DIV SWITCH

The VOLTS/DIV switch selects attenuator ratio and preamplifier gain to determine the deflection factor. The basic 1X deflection factor of the vertical deflection system is 2 mV/division. At this setting, no attenuators are switched in and the gain switching curcuit sets the preamplifier gain to maximum. To provide the complete range of deflection factors indicated on the front panel, precision attenuators are switched in and out of the attenuator and gain switching circuit.

The attenuators are frequency compensated voltage dividers that provide constant attenuation at all frequencies within the bandwidth of the instrument. The input RC characteristics (approximately 1 MΩ times approximately 30 pF) are maintained for each setting of the VOLTS/DIV switch. The attenuator circuit consists of a 10X and a 100X attenuator. 1000X is obtained when the 10X and 100X attenuators are cascaded.

The gain switching circuit consists of R4143 through R4147 and three VOLTS/DIV switch contacts. Three preamplifier gains are selected: 1X (maximum), 2.5X reduction, and 5X reduction. Refer to Table 7-1 for the attenuator and gain switching sequence.

PREAMPLIFIER

The signal from the input attenuator is connected to source follower Q4122A via C4123 and R4123. Resistor R4122 determines the 1 MΩ input resistance and R4123 limits current drive to the gate of Q4122A. Diode CR4123 protects the circuit from high negative-going input signals by limiting the voltage at the gate of Q4122A to about −8 volts. The Q4122A gate-drain junction provides protection from high positive-going signals by limiting the gate voltage to about +8 volts. FET Q4122B provides a constant-current source for Q4122A. For some serial numbers, Q4122 substrate (pin 8) is provided with a bias to compensate for possible substrate leakage. This bias is derived by the voltage divider action of R4128 and R4129 between +8 volts and ground.

Transistors U4134B and U4134C are emitter followers. The signal at the emitter of U4134B follows the signal at the gate of Q4122A. Divider network R4143 through R4147 attenuates the signal from U4134B which drives the base of U4134A. DC BAL, R4132, adjusts for minimum trace shift when switching between adjacent positions of the VOLTS/DIV switch.

Paraphase amplifier stage U4134A and U4134D converts the single-ended signal at the base of U4124A to a push-pull current signal. These current signals are fed to the delay line driver stage via buffer stages Q4302 and Q4303 (see diagram 4). Resistors R4155 and R4165 provide compensation to maintain average power during voltage excursions. Capacitors C4155 and C4165 reduce Miller effect through U4134A and U4134D.

The components connected between U4134A and U4134D emitters compensate for high-frequency losses in the preamplifier. Gain adjustment R4151 determines the gain of the preamplifier. The VAR control, R4152, provides uncalibrated deflection factors between VOLTS/DIV switch settings by attenuating the signal to the base of U4134A. When R4152 is rotated clockwise, its full resistance is in series with R4162, and the deflection factors are calibrated.

TABLE 7-1

Attenuator and Gain Switching Sequence

VOLTS/DIV Setting	Attenuator (signal attenuation)	Gain Switch (preamp gain reduction)
2 mV	1X	1X
5 mV	1X	2.5X
10 mV	1X	5X
20 mV	10X	1X
50 mV	10X	2.5X
.1 V	10X	5X
.2 V	100X	1X
.5 V	100X	2.5X
1 V	100X	5X
2 V	1000X	1X
5 V	1000X	2.5X
10 V	1000X	5X

TRIGGER PICKOFF

A sample of the vertical voltage signal from the emitters of U4134A and U4134D is applied to Q4176 and Q4174, where it is converted to a current signal. This current signal is applied to the trigger input amplifier (see diagram 5) via trigger source switching circuitry (see diagram 4). When the SOURCE switch is set to INT, approximately −4 volts from the trigger input amplifier appears at the Q4176 collector circuit, reverse biasing CR4367 (see diagram 4). When the source switch is set to LINE, EXT, EXT ÷ 10, or X-Y, the internal trigger signal is disconnected from the trigger input amplifier, permitting CR4367 to conduct and set the collector of Q4176 at about −3 volts. This maintains conduction of Q4176, providing a constant load to prevent distortion of the main vertical signal.

VOLTAGE CONDITIONS

Voltages shown on this schematic diagram were measured with a TEKTRONIX DM 501 Digital Multimeter. Voltage measurements can vary as much as ±20%. No signals were applied to the vertical input or the X (external trigger) input. See waveform conditions for T912 control settings.

WAVEFORM CONDITIONS

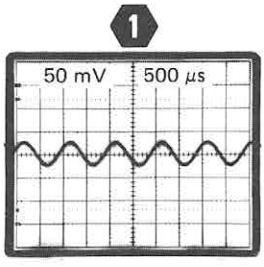
Waveforms below were monitored with a TEKTRONIX 7704A Oscilloscope, 7B71 Time base, 7A15 Amplifier, and 10X probe (1X probe where noted). The oscilloscope input coupling was set to ac. Waveforms may vary as much as ±20%.

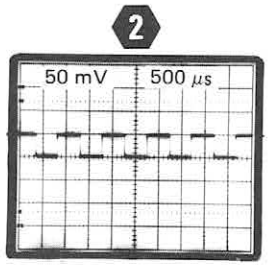
A 1 kHz, 50 mV sine wave was applied to CH 1 input and a 1 kHz, 50 mV square wave was applied to CH 2 input. A TEKTRONIX FG 501 Function Generator provides either of the input waveforms.

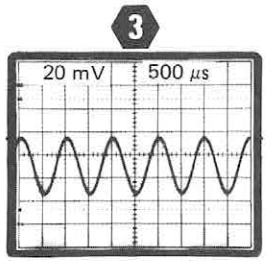
The T912 controls were set as follows:

VOLTS/DIV (both)	10 mV
AC-GND-DC (both)	DC
Vertical Mode	CH 1
SOURCE	INT
MODE	AUTO
SLOPE	+OUT
SEC/DIV	.5 ms

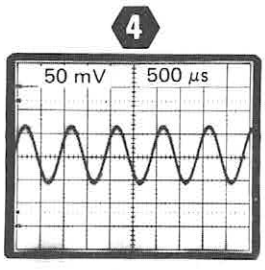
The other controls were set as needed to obtain a display.

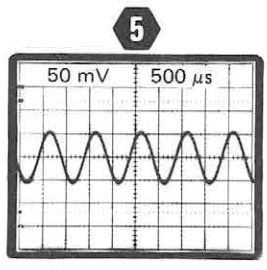






USE 1X PROBE





VOLTAGE & WAVEFORM CONDITIONS

VOLTS/DIV S4110 (SHOWN IN 2mV)

(SHOWN IN AC)

(CH1 INPUT SWITCH) S4100 — AC, GND, DC

J4110 (CH1 INPUT) Y

R4102 1M, C4102 .022, C4101 6.8, R4104 240, C4104 2-18, C4105 0.5-3, R4105 990K, C4106 300, R4106 18, R4107 10.1K, R4108 33, C4113 2-18, C4114 1-5.5, R4114 900K, C4116 22, R4116 111K, R4117 10, R4118 150

J4100 -1

C4123 0.01, R4123 470K, CR4123, R4122 1M, Q4122 SUBSTRATE

R4128 82K, U4134B 1/5 3086, *Q4122A, *Q4122B, R4126 20, R4127 20, R4129 1.2K, R4137 1.5K, R4136 1.5K, J4100-4, J4100-3

CH1 DC BAL

U4134C 1/6 3086, R4132 25K, R4133 15K, R4134 150, R4138 61.9

C4143, R4144 150, R4145 50, R4146 50, R4143 43.2, R4147 20

J4100-2

R4161 392, (CH1) GAIN R4151 1K, VAR (CH1) R4152 1K CW (CAL), R4162 52.3

U4134A 1/5 3086, U4134D 1/5 3086

C4158 .01, C4153 100, R4158 11K, R4163 54.9, C4168 .001, R4168 9.1K, R4164 2.15K, R4154 2.15K, C4155 470, R4155 1.5K, R4156 604, R4166 604, R4165 1.5K, C4165 470

Q4176, R4174 3.9K, R4173 24.9, R4175 3.9K, Q4174, +8V, -8V

CH1 TRIG SIG TO CR4364 & CR4362 DIAG 4

CH1 -VERT SIG TO Q4302

CH1 +VERT SIG TO Q4303

DIAG 4

A6 CH1 VERTICAL ATTENUATOR BOARD

TO CR4123, R4123 & C4123

*Q4122 BELOW SN B010550

VOLTS/DIV S4210 (SHOWN IN 2mV)

(SHOWN IN AC)

(CH2 INPUT SWITCH) S4200 — AC, GND, DC

J4210 (CH2 INPUT)

R4202 1M, C4202 .022, C4201 6.8, R4204 240, C4204 2-18, C4205 0.5-3, R4205 990K, C4206 300, R4206 18, R4207 10.1K, R4208 33, C4213 2-18, C4214 1-5.5, R4214 900K, C4216 22, R4216 111K, R4217 10, R4218 150

J4200 -1

C4223 0.01, R4223 470K, CR4223, R4222 1M, Q4222 SUBSTRATE

R4228 82K, U4234B 1/5 3086, Q4222A, Q4222B, R4226 20, R4227 20, R4229 1.2K, R4237 1.5K, R4236 1.5K, J4200-4, J4200-3

CH2 DC BAL

U4234C 1/5 3086, R4232 25K, R4233 15K, R4234 150, R4238 61.9

C4243, R4244 150, R4245 50, R4246 50, R4243 43.2, R4247 20

J4200-2

R4251 1K, GAIN (CH2), VAR (CH2) R4252 1K, R4261 392, R4262 52.3

U4234A 1/5 3086, U4234D 1/5 3086

C4258 .01, C4253 100, R4258 11K, R4263 54.9, C4268 .001, R4268 9.1K, R4264 2.15K, R4254 2.15K, C4255 470, R4255 1.5K, R4256 604, R4266 604, R4265 1.5K, C4265 470

Q4276, R4274 3.9K, R4273 24.9, R4275 3.9K, Q4274, +8V, -8V

CH2 TRIG SIG TO CR4366 DIAG 4

CH2 -VERT SIG TO Q4312

CH2 +VERT SIG TO Q4313

DIAG 4

A7 CH2 VERTICAL ATTENUATOR BOARD

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

SEE PARTS LIST FOR SEMICONDUCTOR TYPES.

PARTIAL A8 VERTICAL BOARD

T912

REV. A, APR. 1977
1981-9

VERTICAL INPUT 3

VERT SWITCHING CIRCUIT DESCRIPTION

Since Channel 1 and Channel 2 vertical circuits are identical, only Channel 1 is discussed in detail. The 4100 series circuit numbers identify the Channel 1 components and 4200 series numbers identify the Channel 2 components.

Digital logic devices are used to perform some of the functions in this instrument. LO and HI designations are used in this circuit description to indicate the state of the digital circuit. HI indicates the more positive of the two levels. The specific voltages that constitute a LO and HI logic state, may vary between individual devices.

PREAMP BUFFER

The buffer stages Q4302 and Q4303 isolate the preamplifier from the delay line driver. POSITION control R4306 varies the dc voltage at the bases of Q4322 and Q4324 to vertically position the trace on the crt.

DELAY LINE DRIVER

The delay line driver is a push-pull feedback amplifier stage composed of Q4322, Q4324, Q4336, Q4346, and associated circuitry. A sample of the output of Q4346 and Q4336 is fed back through R4336-R4328 and R4346-R4342 to the bases of Q4322 and Q4324. Due to this feedback, this stage forms an inverting operational amplifier with a virtual ground at the bases of Q4322 and Q4324. Any current into these virtual grounds (null points) causes an output voltage at the emitters of Q4336 and Q4346 that is proportional to the feedback resistance.

Components C4333, C4334, C4344, R4333, R4334, and R4344 provide compensation (peaking) to correct for delay line losses.

DELAY LINE

The delay line, DL4339, provides approximately 200 ns delay in the vertical signal. This allows the sweep generator circuit time to initiate a sweep before the vertical signal reaches the crt vertical deflection plates.

VERTICAL SWITCHING

The vertical switching circuit determines whether CH 1 or CH 2 is connected to the vertical output amplifier. in the DUAL TRACE alternate or chopped modes, both channels are alternately displayed on a time shared basis.

The diode gates, consisting of four diodes each, act as switches that allow either of the vertical preamplifier signals to be coupled to the delay line driver. Diodes CR4302, CR4303, CR4304, and CR4305 control the CH 1 output; CR4312, CR4313, CR4314, and CR4315 control the CH 2 output. These diodes are controlled by flip-flop U4364A, which in turn is controlled by Vertical Mode switch, S4370.

When the Vertical Mode switch is in the CH 1 position, pin 4 of U4364A is held LO, causing pin 5 to go HI. A HI at pin 5 (a voltage higher than at the bases of Q4322 and Q4324) reverse biases CR4302 and CR4303 and forward biases CR4304 and CR4305. This allows the CH 1 signal to pass to the delay line driver. When pin 5 is HI, pin 6 is LO, causing the cathodes of CR4312 and CR4313 to be connected to a voltage much lower than on the bases of Q4322 and Q4324. Diodes CR4312 and CR4313 are now forward biased and diodes CR4314 and CR4315 are reverse biased, preventing the CH 2 signal from passing to the delay line driver.

In the CH 2 mode, the above conditions are reversed. Diodes CR4312 and CR4313 are reverse biased, passing the CH 2 signal and blocking the CH 1 signal.

In the DUAL TRACE Vertical Mode, CH 1 and CH 2 are alternately connected to the delay line driver. There are two dual trace modes: chopped and alternate. These modes are determined by the SEC/DIV switch setting. Chopped mode is obtained for sweep speeds of 1 ms and slower; alternate is obtained for sweep speeds of 0.5 ms and faster.

In the chopped mode pin 2 of U4376A is ungrounded, allowing the multivibrator, U4376A and U4376D, to free run at about 250 kHz. The output at pin 8 of U4376C serves as a clock pulse for U4364A, which in turn switches the diode gates at the 250 kHz rate. The clock pulse is also fed to U4364B, which provides an output pulse to the Z Axis amplifier to blank out the transition between CH 1 and CH 2 traces. If pin 13 of U4364B goes LO, the output pin 9 is set LO, causing pin 6 of U4376B to go HI. This causes pin 13 of U4364A to go HI after being delayed by C4386 charging through R4386.

The clock pulse applied to pin 11 of U4364B causes pin 9 to go HI, which in turn, after passing through the inverter and after some delay, sets pin 13 LO again. This causes pin 9 to go LO again. The positive-going voltage pulse (whose width is determined by R4386 and C4386) is converted to current by R4385-R4384 and sent to the Z Axis Amplifier to blank switching transients.

In the alternate mode, pin 2 of U4376A is grounded, preventing multivibrator operation, thus keeping pin 10 of

U4376C HI. At the end of each sweep, the base of Q4372 receives a current pulse, driving it into saturation. The resulting negative-going pulse at the collector is fed through C4372 to pin 9 of U4376C causing pin 8 to go HI. This in turn switches U4364A to pass either CH 1 or CH 2 to the delay line driver at the end of each sweep. Pin 12 of U4364B is grounded through the SEC/DIV switch and prevents an output at pin 9.

The Vertical Mode switch also selects the appropriate internal triggering source for CH 1 and CH 2. With the Vertical Mode switch set to CH 1 and DUAL TRACE, CR4364 is forward biased and the signal from the CH 1 trigger pickoff goes to the sweep circuit. In these modes, CR4363 is connected to the −8 volts, thus reverse biasing CR4366, preventing the CH 2 trigger signal from entering the trigger input amplifier. With the Vertical Mode switch set to CH 2, CR4366 becomes forward biased while CR4364 is reverse biased because CR4362 is now connected to −8 volts.

VOLTAGE CONDITIONS

Voltages shown on this schematic diagram were measured with a TEKTRONIX DM 501 Digital Multimeter. Voltage measurements can vary as much as ±20%. No signals were applied to the vertical input or the X (external trigger) input. See waveform conditions for T912 control settings.

WAVEFORM CONDITIONS

Waveforms below were monitored with a TEKTRONIX 7704A Oscilloscope, 7B71 Time Base, 7A15 Amplifier, and 10X probe. The oscilloscope input coupling was set to ac. Waveforms may vary as much as ±20%.

A 1 kHz, 50 mV sine wave was applied to CH 1 input and a 1 kHz, 50 mV square wave was applied to CH 2 input. A TEKTRONIX FG 501 Function Generator provides either of the input waveforms.

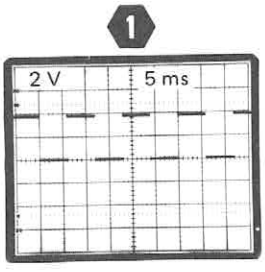
The T912 controls were set as follows:

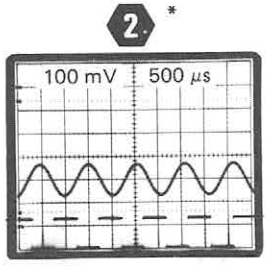
VOLTS/DIV (both)	20 mV
AC-GND-DC (both)	DC
Vertical Mode	DUAL TRACE
SOURCE	INT
MODE	AUTO
SLOPE	+OUT
SEC/DIV	.5 ms

The other controls were set as needed to obtain a display.

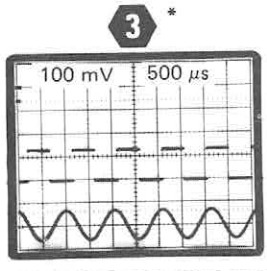
The CH 1 POSITION control was adjusted so that the bottom of the sine wave was on the first horizontal graticule line above the center and the CH 2 POSITION control was adjusted so that the top of the square wave was on the first horizontal graticule line below the center.

***Screen positions for waveforms 2, 3, 4, and 5 are affected by settings of T912 POSITION controls.**





ADJUST TRIGGERING AS NECESSARY



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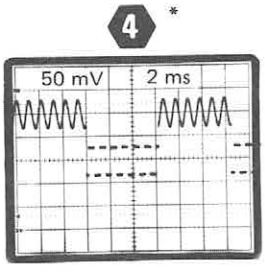
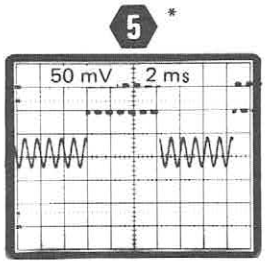
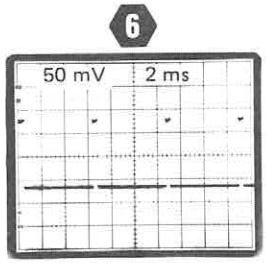






VOLTAGE & WAVEFORM CONDITIONS

FROM DIAG 3

CH 1 -VERT SIG FROM R4155 (+5.1)

CH 1 +VERT SIG FROM R4165 (+5.1)

Q4302

Q4303

+8V

R4302 357

R4303 432

(+2.2) (+4.4) (+2.2)

R4306 20K

POSITION (CH 1)

R4307 20K -8V

CR4304 CR4302 CR4303 CR4305

FROM DIAG 3

CH 2 -VERT SIG FROM R4255

CH 2 +VERT SIG FROM R4265

Q4312

Q4313

R4316 20K

POSITION (CH 2)

R4317 20K -8V

C4368 180

CR4314 CR4312 CR4313 CR4315

R4366 470

R4368 240

R4370 470

R4369 240

R4325 604 (-0.8)

R4328 2.0K

R4322 7.32K (+1.4) -8V

R4323 7.32K (+1.4)

Q4322

(+2.1) +8V

R4324 576

Q4324

R4342 2.0K

R4326 604 (-0.8)

R4327 422 -8V

Q4336

R4336 2.0K (+0.06)

R4333 47K

C4334 0.5-3

R4334 25K

C4333 22

C4344 2-18

R4338 1K

+8V C4338 0.1

R4344 25K

R4348 1K

R4346 2.0K (+0.06)

Q4346

R4349 100 -8V

C4349 0.1

(-6.2)

R4337 75

R4347 75

DL4339 ≈200mS

DIAG 1

P4-9 -VERT SIG TO Q112

P4-10

P4-11 +VERT SIG TO Q122

P4-12

FROM DIAG 3

CH 1 TRIG SIG FROM Q4176

CH 2 TRIG SIG FROM Q4276

CR4364 CR4362 CR4366

CR4363

C4363 .01

C4362 .01

+5V R4364 4.7K

+5V R4365 4.7K

C4366 0.1

C4365 0.1

U4364A 1/2 7474

R4367 620

CR4367

VR4367 4.3V -8V

P4-2 TRIG SIG TO J2-2

DIAG 5

P4-3 +8V

TO DIAG 3

(CH 1) +8V1

(CH 2) +8V2

C4392 1MF R4394 47

C4394 0.1 R4395 47

C4395 0.1 R4392 51

+5V VR4392 5.1V

P4-1 TO J7-7

FROM DIAG 2

C4393 1MF

-8V P4-8 -8V

TO DIAG 3

(CH 1) -8V1

(CH 2 R4132) -8V2

C4396 0.1 R4396 47

C4397 0.1 R4397 47

S4370 VERTICAL MODE

CH 2

DUAL TRACE (CH 1 TRIG)

CH 1

CH1 CH2 CH1 CH2

-8V DUAL TR DUAL TR

+5V R4382 4.7K

C4370 .01

U4376D 1/4 7400

R4377 2.7K

C4375 470

C4377 470

R4375 2.7K

+5V R4373 10K

U4376A 1/4 7400

U4376C 1/4 7400

U4364B 1/2 7474

+5V R4384 1K

R4385 6.2K

C4385 15

C4386 .001

R4386 300

U4376B 1/4 7400

P4-7 CHOP BLANKING TO Q416

DIAG 1

+5V R4372 2.7K

C4372 47

Q4372

R4374 10K

R4371 1K

C4371 .001

ALT SYNC PULSE FROM R2276

DIAG 6

J2-6 P4-5

P4-4 ENHANCE CONTROL TO P9-3

DIAG 2

J2260-7

S2250 SEC/DIV

J2260-12 (CHOP/ALT)

J2-7 P4-6

SEE DIAG 6

S: .5 .2 .1 50 20 10 5

mS: 2 1 .5 .2 .1 50 20 10 5

μS: 2 1 5

+5V C4364 0.1 U4364 7474

+5V C4376 0.1 U4376 7400

PARTIAL A13 TIMING BOARD

PARTIAL A12 HORIZ BOARD

PARTIAL A1 INTERFACE BOARD

PARTIAL A8 VERTICAL BOARD

PARTIAL A1 INTERFACE BOARD

T912

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

SEE PARTS LIST FOR SEMICONDUCTOR TYPES.

1981-11
REV.A APR 1977

VERTICAL SWITCHING 4

TRIGGER CIRCUIT DESCRIPTION SN B010315-UP

Digital logic devices are used to perform some of the functions in this instrument. LO and HI designations are used in this circuit description to indicate the state of the digital circuit. HI indicates the more positive of the two levels. The specific voltages that constitute a LO and HI logic state may very between individual devices.

INPUT AND SWITCHING

SOURCE Switch

The SOURCE switch, S2100, selects trigger signals from INT, LINE, X-Y, EXT, and $\frac{\text{EXT}}{10}$.

INT. Signal from the trigger pickoff circuit in the vertical amplifier is connected to the trigger input amplifier, U2126A.

LINE. A sample of the line voltage, obtained from the power transformer, is connected to the trigger input amplifier U2126A.

EXT. Externally applied signals pass through buffer amplifier Q2104-Q2106. FET Q2104 is a source follower and Q2106 is a current source. Transistor Q2108 and R2103 convert the voltage signal at the buffer output to a current for application to the trigger input amplifier. When EXT is selected, the collector of Q2108 is connected to the trigger input amplifier (U2126A) by SOURCE switch S2100.

$\frac{\text{EXT}}{10}$. The output of the buffer amplifier Q2104-Q2106 is connected to R2101. Resistor R2101 converts the buffer output voltage to a current that is connected to the trigger input amplifier via S2100.

X-Y. Signals from the X (EXT) input are routed to the horizontal amplifier via Q2104, S2100, And CR2186. The SOURCE switch connects +8 volts to R2184, forward biasing CR2186 and providing current to the horizontal amplifier to center the crt display. Also, +8 volts is applied to CR2182 and R2134 to switch the sweep into the NORM mode and to disable the trigger circuit.

MODE Switch

The MODE switch (S2150) selects four triggering modes: AUTO, NORM, SINGLE SWP, and RESET.

AUTO. Allows the sweep to free run in the absence of a triggering signal. See Sweep circuit description for details.

NORM. Connects +8 volts to R2223 in the sweep generator circuit. Allows the sweep to run only when a suitable triggering signal is present.

SINGLE SWP. Places the sweep circuit in NORM and removes +8 V from R2165 activating the single sweep circuitry. The previous sweep has left pin 5 of U2156B HI, which allows the Schmitt trigger to start the sweep on the first trigger signal applied after the MODE switch is put in SINGLE SWP.

RESET. Applies +8 V to R2160, which turns off Q2162. When RESET is released, Q2162 turns on, resulting in a HI (through U2126E and U2156D) at pin 5 of U2156B.

TRIGGER INPUT AMPLIFIER

The trigger input amplifier consists of U2126A, U2126B, Q2124, and associated circuitry. Resistors R2127 and R2128 set the amplifier input at −4 volts. The inverting configuration and feedback from the emitter of Q2124 form an inverting operational amplifier with a null point at the base of U2126A. Any current into the null point produces a voltage at the output proportional to the feedback resistor R2123. Diode CR2124 prevents the emitter of Q2124 from going below ground and reversing the voltage across C2132.

TRIGGER LEVEL COMPARATOR

Differential amplifier Q2134-Q2136 functions as a comparator. The LEVEL control R2138 selects the point on the waveform that starts a sweep. Capacitor C2132 ac couples the trigger signal to the comparator. As the trigger signal at the base of Q2134 passes through the same voltage level as the base of Q2136 (set by LEVEL control), the signal at the collector of U2126D passes through the threshold (about 1 volt) of Schmitt trigger U2156A-U2156B producing a logic trigger signal. The trigger signals at the collectors of Q2134 and Q2136 are of opposite polarity. This allows SLOPE switch S2140 to invert the signals applied to trigger input amplifier U2126D, C. When the SLOPE switch is in the +OUT position, the output at the collector of U2126D is in phase with the trigger source signal. Transistors U2126C and U2126D convert the current signal from the collectors of Q2134 or Q2136 to a voltage signal for triggering the Schmitt trigger.

SINGLE SWEEP CIRCUIT

The single sweep circuit consists of Q2162, U2126E, U2156C, and U2156D and associated circuitry.

Putting the MODE switch S2150 in SINGLE SWP activates the single sweep circuit by removing +8 V from R2165. The next trigger signal to occur starts a sweep. At the end of the sweep, pin 9 of U2156C goes low for the holdoff period. Feedback from pin 11 of U2156D to pin 10 of U2156C holds pin 5 of U2156B LO. While pin 5 of U2156B is LO, the Schmitt trigger cannot operate and another sweep does not occur until the Schmitt trigger is reset.

When the MODE switch is put in RESET, +8 V is applied to R2160, turning off Q2162. While Q2162 is off, C2162 discharges through R2162 and R2163. When the MODE switch is put back in SINGLE SWP after being in RESET, Q2162 is turned on. The collector of Q2162 goes from ground to about +8 V. This positive-going transition is coupled through C2162 to U2126E. This turns U2126E on and causes a LO at pin 13 of U2156D, which in turn causes a HI at pin 5 of U2156B. Again, the first trigger signal starts a sweep.

SCHMITT TRIGGER

The Schmitt trigger for the NORM and AUTO triggering modes consists of U2156A, U2156B, and associated circuitry. Hysteresis of this trigger circuit is determined by R2152, R2153, and R2147.

When the MODE switch is in AUTO or NORM, R2165 is connected to +8 V and U2126E is saturated. This holds pin 13 of U2156D LO and pin 5 of U2156B HI. As long as pin 5 of U2156B is HI the Schmitt Trigger is enabled. The positive feedback through R2153 causes fast switching at pin 4 of U2156B, producing a logic trigger signal at pin 6.

VOLTAGE CONDITIONS

Voltages shown on this schematic diagram were measured with a TEKTRONIX DM 501 Digital Mulitmeter. Voltage measurements can vary as much as ±20%. No signals were applied to the vertical input or the X (external trigger) input. See waveform conditions for T912 control settings.

WAVEFORM CONDITIONS

Waveforms below were monitored with a TEKTRONIX 7704A Oscilloscope, 7B71 Time Base, 7A15 Amplifier, and 10X probe. The oscilloscope input coupling was set to ac. Waveforms may vary as much as ±20%.

A 1 kHz, 50 mV sine wave was applied to CH 1 input and a 1 kHz, 50 mV square wave was applied to CH 2 input. A TEKTRONIX FG 501 Function Generator provides either of the input waveforms.

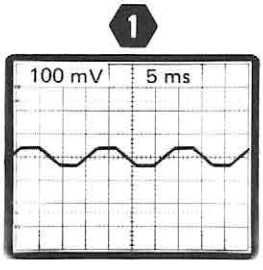
The T912 controls were set as follows:

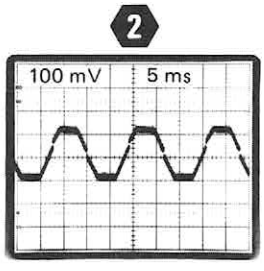
VOLTS/DIV (both)	20 mV
AC-GND-DC (both)	DC
Vertical Mode	DUAL TRACE
SOURCE	LINE
MODE	AUTO
SLOPE	+OUT
STORE	Non store (button out)
SEC/DIV	.5 ms

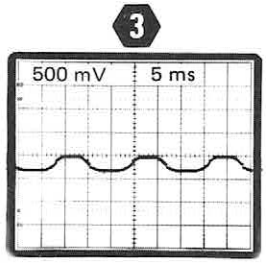
The other controls were set as needed to obtain a display.

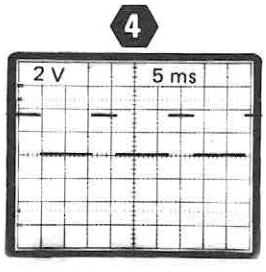
NOTE

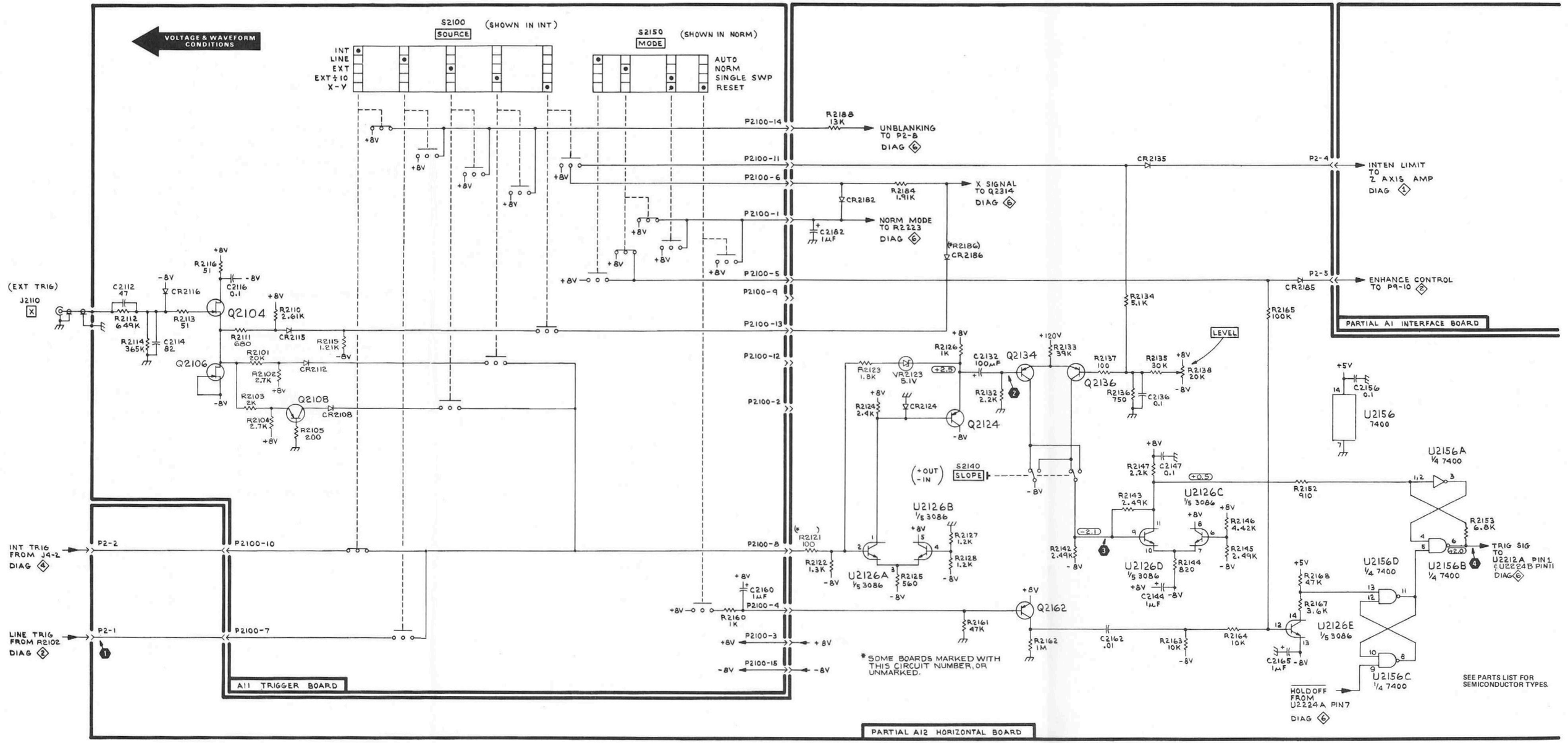
To obtain voltages and waveforms on the Horizontal board, the Vertical Amplifier must be operated separately from the instrument, using a Vertical Amplifier Extender Troubleshooting Fixture. See Troubleshooting Equipment and Vertical Amplifier Replacement in the Service Information section of this manual.











T912

REV A APR 1977
1981-23

(SN B010315 & UP)

TRIGGER 5

TRIGGER CIRCUIT DESCRIPTION (For SN B010100 through SN B010314)

Digital logic devices are used to perform some of the functions in this instrument. LO and HI designations are used in the circuit description to indicate the state of the digital circuit. HI indicates the more positive of the two levels. The specific voltages which constitute a LO and HI logic state may vary between individual devices.

INPUT AND SWITCHING

SOURCE Switch

The SOURCE switch, S2100, selects trigger signals from INT, LINE, X-Y, EXT, and $\frac{\text{EXT}}{10}$.

INT. Signal from the trigger pickoff circuit in the vertical amplifier is connected to the trigger input amplifier U2126A.

LINE. A sample of the line voltage, obtained from the power transformer, is connected to the trigger input amplifier U2126A.

EXT. External trigger signals applied to J2110 external trigger (X) input are connected to the trigger input amplifier, U2126A, via input buffer amplifier Q2114-Q2116 and coupling capacitor C2123. Diode CR2116 protects Q2114 from large negative-going trigger signals. (The Q2114 gate-drain junction provides protection from large positive-going signals by limiting the Q2114 gate voltage to about +8 volts.) Transistor Q2116 provides a relatively constant current source for Q2114. Resistor R2111 sets the external trigger sensitivity and converts the voltage signal to a current signal.

$\frac{\text{EXT}}{10}$. Resistors R2119 and R2120, with R2111, form a current divider to attenuate the external trigger signal by a factor of 10. Diodes CR2115 and CR2186 form a current switch that prevents external trigger signals from coupling into the horizontal amplifier in EXT and $\frac{\text{EXT}}{10}$.

X-Y. Signals from the X (EXT) input are routed to the horizontal amplifier via Q2114, S2110, and CR2186. The SOURCE switch connects +8 volts to R2184, forward biasing CR2186 and providing current to the horizontal amplifier to center the crt display. Also, +8 volts is applied to CR2182 and R2134 to switch the sweep into the NORM mode and to disable the trigger circuit.

MODE Switch

The MODE switch (S2150) selects four triggering modes: AUTO, NORM, SINGLE SWP, and RESET.

AUTO. Allows the sweep to free run in the absence of triggering signal. See Sweep circuit description for details.

NORM. Connects +8 volts to R2223 in the sweep generator circuit. Allows the sweep to run only when a suitable triggering signal is present.

SINGLE SWP. Places the sweep circuit in NORM and removes +8 V from R2165 activating the single sweep circuitry. The previous sweep has left pin 5 of U2156B HI, which allows the Schmitt trigger to start the sweep on the first trigger signal applied after the MODE switch is put in SINGLE SWP.

RESET. Applies +8 V to R2160, which turns off Q2162. When RESET is released, Q2162 turns on, resulting in a HI (through U2156E) at pin 5 of U2156B.

TRIGGER INPUT AMPLIFIER

The trigger input amplifier consists of U2126A, U2126B, Q2124, and associated circuitry. Resistors R2127 and R2128 set the amplifier input at −4 volts. The inverting configuration and feedback from the emitter of Q2124 form an inverting operational amplifier with a null point at the base of U2126A. Any current into the null point produces a voltage at the output proportional to the feedback resistor R2123. Diode CR2124 prevents the emitter of Q2124 from going below ground and reversing the voltage across C2132.

TRIGGER LEVEL COMPARATOR

Differential amplifier Q2134-Q2136 functions as a comparator. The LEVEL control R2138 selects the point on the waveform that starts a sweep. Capacitor C2132 ac couples the trigger signal to the comparator. As the trigger signal at the base of Q2134 passes through the same voltage level as the base of Q2136 (set by LEVEL control), the signal at the collector of U2126D passes through the threshold (about 1 volt) of Schmitt trigger U2156A-U2156B producing a logic trigger signal. The trigger signals at the collectors of Q2134 and Q2136 are of opposite polarity. This allows the SLOPE switch S2140 to invert the signals applied to the trigger input amplifier U2126D, C. When the SLOPE switch is in the +OUT position, the output at the collector of U2126D is in phase with the trigger source signal. Transistors U2126C and U2126D convert the current signal from the collectors of Q2134 or Q2136 to a voltage signal for triggering the Schmitt trigger.

SINGLE SWEEP CIRCUIT

The single sweep circuit consists of Q2162, U2126E, U2156C, and U2156D and associated circuitry.

Putting the MODE switch S2150 in SINGLE SWP activates the single sweep circuit by removing +8 V from R2165. The next trigger signal to occur starts a sweep. At the end of the sweep, pin 9 of U2156C goes low for the holdoff period. Feedback from pin 11 of U2156D to pin 10 of U2156C holds pin 5 of U2156B LO. While pin 5 of U2156B is LO, the Schmitt trigger cannot operate and another sweep does not occur until the Schmitt trigger is reset.

When the MODE switch is put in RESET, +8 V is applied to R2160 turning off Q2162. While Q2162 is off, C2162 discharges through R2162 and R2163. When the MODE switch is put back in SINGLE SWP after being in RESET, Q2162 is turned on. The collector of Q2162 goes from ground to about +8 V. This positive-going transition is coupled through C2162 to U2126E. This turns U2126E on and causes a LO at pin 13 of U2156D, which in turn causes a HI at pin 5 of U2156B. Again, the first trigger signal starts a sweep.

SCHMITT TRIGGER

The Schmitt trigger consists of U2156A, U2156B, and associated circuitry. Hysteresis of the trigger circuit is determined by R2152, R2153, and R2147.

When the MODE switch is in AUTO or NORM, R2165 is connected to +8 V and U2126E is saturated. This holds pin 13 of U2156D LO and pin 5 of U2156B HI. As long as pin 5 of U2156B is HI the Schmitt Trigger is enabled. The positive feedback through R2153 causes fast switching at pin 4 of U2156B, producing a logic trigger signal at pin 6.

VOLTAGE CONDITIONS

Voltages shown on this schematic diagram were measured with a TEKTRONIX DM 501 Digital Mulitmeter. Voltage measurements can vary as much as ±20%. No signals were applied to the vertical input or the X (external trigger) input. See waveform conditions for T912 control settings.

WAVEFORM CONDITIONS

Waveforms below were monitored with a TEKTRONIX 7704A Oscilloscope, 7B71 Time Base, 7A15 Amplifier, and 10X probe. The oscilloscope input coupling was set to ac. Waveforms may vary as much as ±20%.

A 1 kHz, 50 mV sine wave was applied to CH 1 input and a 1 kHz, 50 mV square wave was applied to CH 2 input. A TEKTRONIX FG 501 Function Generator provides either of the input waveforms.

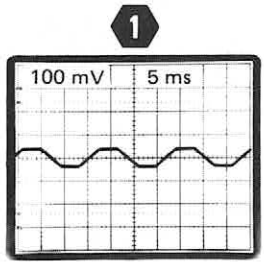
The T912 controls were set as follows:

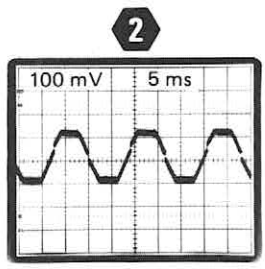
VOLTS/DIV (both)	20 mV
AC-GND-DC (both)	DC
Vertical Mode	DUAL TRACE
SOURCE	LINE
MODE	AUTO
SLOPE	+OUT
STORE	Non store (button out)
SEC/DIV	.5 ms

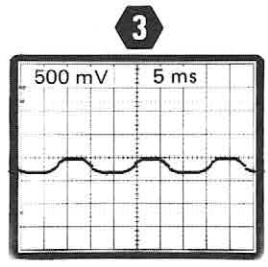
The other controls were set as needed to obtain a display.

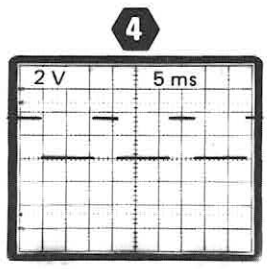
NOTE

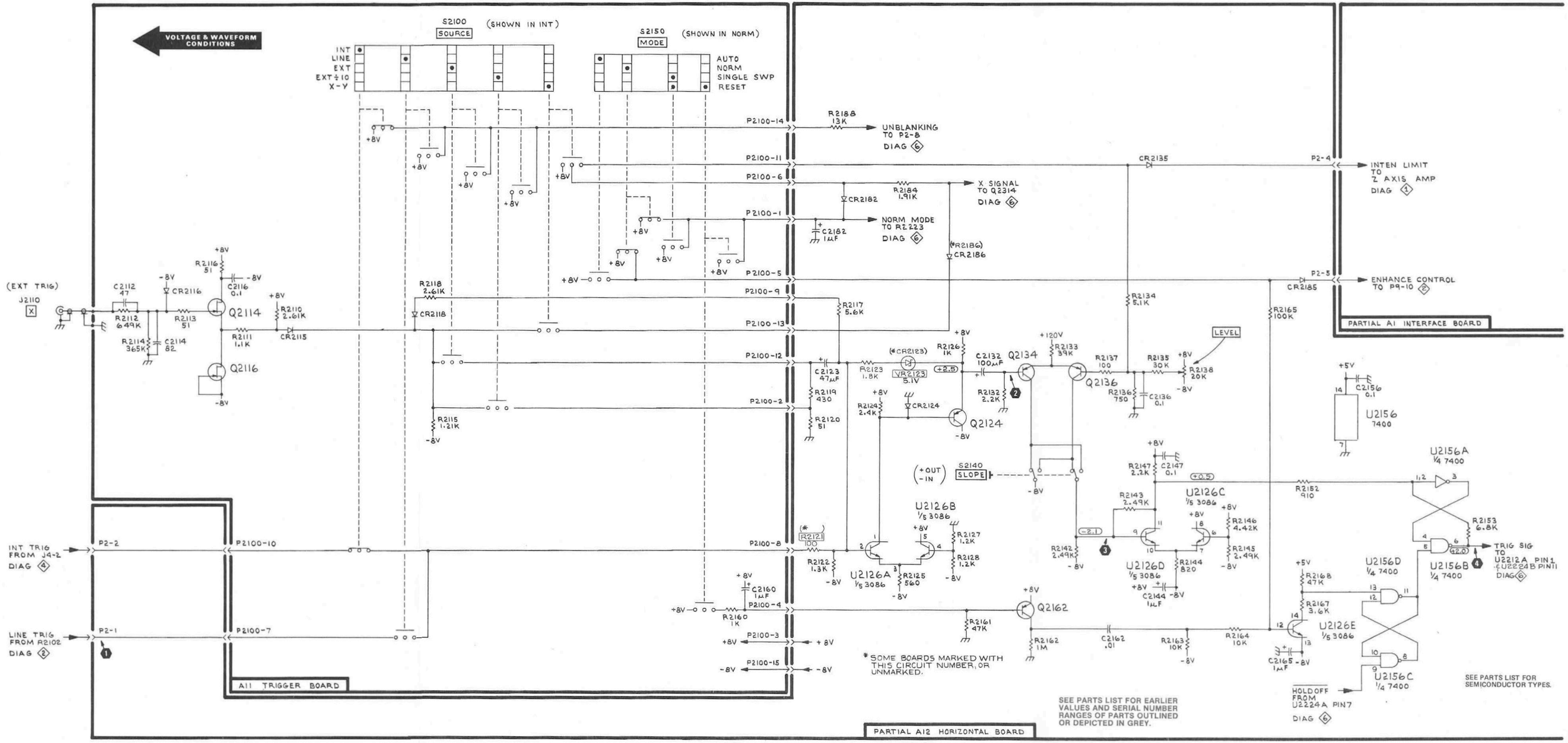
To obtain voltages and waveforms on the Horizontal board, the Vertical Amplifier must be operated separately from the instrument, using a Vertical Amplifier Extender Troubleshooting Fixture. See Troubleshooting Equipment and Vertical Amplifier Replacement in the Service Information section of this manual.











T912

REV A APR 1977
1981-13

(SN B010100-B010314) TRIGGER 5

SWEEP AND HORIZ AMPL CIRCUIT DESCRIPTION

Digital logic devices are used to perform some of the functions in this instrument. LO and HI designations are used in this circuit description to indicate the state of the digital circuit. HI indicates the more positive of the two levels. The specific voltages which constitute a LO and HI logic state may vary between individual devices.

SWEEP

The sweep is produced by a Miller Integrator circuit consisting of Q2242, Q2244, and Q2246. A sweep ramp is initiated at the collector of Q2246 when pin 3 of U2234A goes LO, and is terminated when pin 3 goes HI (see Timing diagram, Fig. 7-2).

In the NORM triggering mode, pin 2 of U2212A is HI allowing a positive-going trigger signal at pin 1 of U2212A to cause pin 3 of U2234A to go LO (via U2212D and U2234C). This reverse biases CR2233 and CR2234, and allows the timing capacitor (selected by the SEC/DIV switch, S2250) to charge, producing a sweep ramp at the collector of Q2246. When the sweep ramp reaches about 12 volts, Q2274 turns on. This causes pin 7 of U2224A to go LO, pin 8 of U2234C to go LO, and pin 3 of U2234A to go HI. When pin 3 of U2234A goes HI, CR2233 and CR2234 are forward biased, terminating the sweep. Pin 7 of U2224A remains LO for a length of time (holdoff time) determined by C2275, C2274, R2275, and R2279. Three holdoff times are selected by the SEC/DIV switch, S2250. After the selected holdoff time, U2224A pin 7 goes HI. This allows the next trigger signal to switch pin 3 of U2234A LO and again start the sweep.

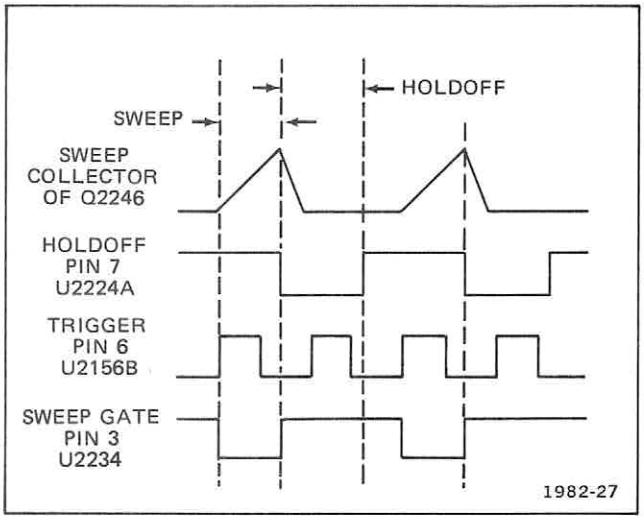


Fig. 7-2. Timing Diagram: sweep generator and sweep gate.

In the AUTO triggering mode, when no trigger signal occurs at pin 11 of U2224B for about 50 ms, pin 10 of U2224B goes LO, causing the sweep to start after the holdoff time ends. This allows the sweep to free run and provide a reference display. When a trigger signal is present, pin 11 of U2224B goes HI, then LO (when trigger signal ends), and the time constant of C2226 and R2226 prevents pin 10 from going LO as long as the repetition rate of the trigger signal is higher than about 20 Hz.

When pin 3 of U2234A goes HI, the current set by R2236, R2235, and R2237 is sent to the Z Axis Amplifier to blank the crt during hold-off.

HORIZONTAL AMPLIFIER

The horizontal amplifier converts the single-ended signal to a push-pull signal, which drives the crt horizontal deflection plates. The input of the horizontal amplifier comes from either the sweep generator or the X (external trigger) input connector. In the X-Y mode, the trace is shifted to the center of the screen by the current through R2184. In the AUTO and NORM modes, the input to the horizontal amplifier is a linear ramp from the sweep generator.

Transistors Q2314, Q2326, and associated circuitry, form an operational amplifier with a variable gain range of over 10 to 1. The gain is set by feedback elements R2312, R2323, and X1-X10 control, R2322. The horizontal POSITION control, R2316 positions the crt display horizontally by varying the current into the base of Q2314.

When the BEAM FINDER switch, S410B, is pressed, the dynamic range of Q2326 is decreased. This limits the horizontal deflection to the crt screen area. The BEAM FINDER switch also limits the vertical deflection to the crt screen area.

Transistors Q2332, Q2334, Q2344, and associated circuitry form a paraphase amplifier. Transistor Q2332 is a low-impedance input for Q2334. Horiz Cal adjustment R2332, sets the gain of the paraphase amplifier. When the current through the collector of Q2334 increases, the current through the collector of Q2344 decreases and is 180° out of phase with the current at the collector of Q2334. The resulting signal to the crt deflection plates is a push-pull signal. Diode CR2334 prevents Q2334 from saturating when R2322 is in the X10 position.

Since Q2334 is a shunt feedback amplifier and Q2344 is a common base amplifier, any noise in the 120 V power supply will appear as a part of the output. To prevent the noise from appearing on the crt screen, an operational amplifier, consisting of Q2354 and associated circuitry,

supplies an inverted sample of the power supply noise to the output. Now, any noise in the 120 volt power supply appears common mode to the horizontal deflection plates, preventing horizontal deflection of the noise signal. Resistor R2354 provides feedback for the operational amplifier.

VOLTAGE CONDITIONS

Voltages shown on this schematic diagram were measured with a TEKTRONIX DM 501 Digital Multimeter. Voltage measurements can vary as much as ±20%. No signals were applied to the vertical input or the X (external trigger) input. See waveform conditions for T912 control settings.

WAVEFORM CONDITIONS

Waveforms below were monitored with a TEKTRONIX 7704A Oscilloscope, 7B71 Time Base, 7A15 Amplifier, and 10X probe. The oscilloscope input coupling was set to ac. Waveforms may vary as much as ±20%.

A 1 kHz, 50 mV sine wave was applied to CH 1 input and a 1 kHz, 50 mV square wave was applied to CH 2 input. A TEKTRONIX FG 501 Function Generator provides either of the input waveforms.

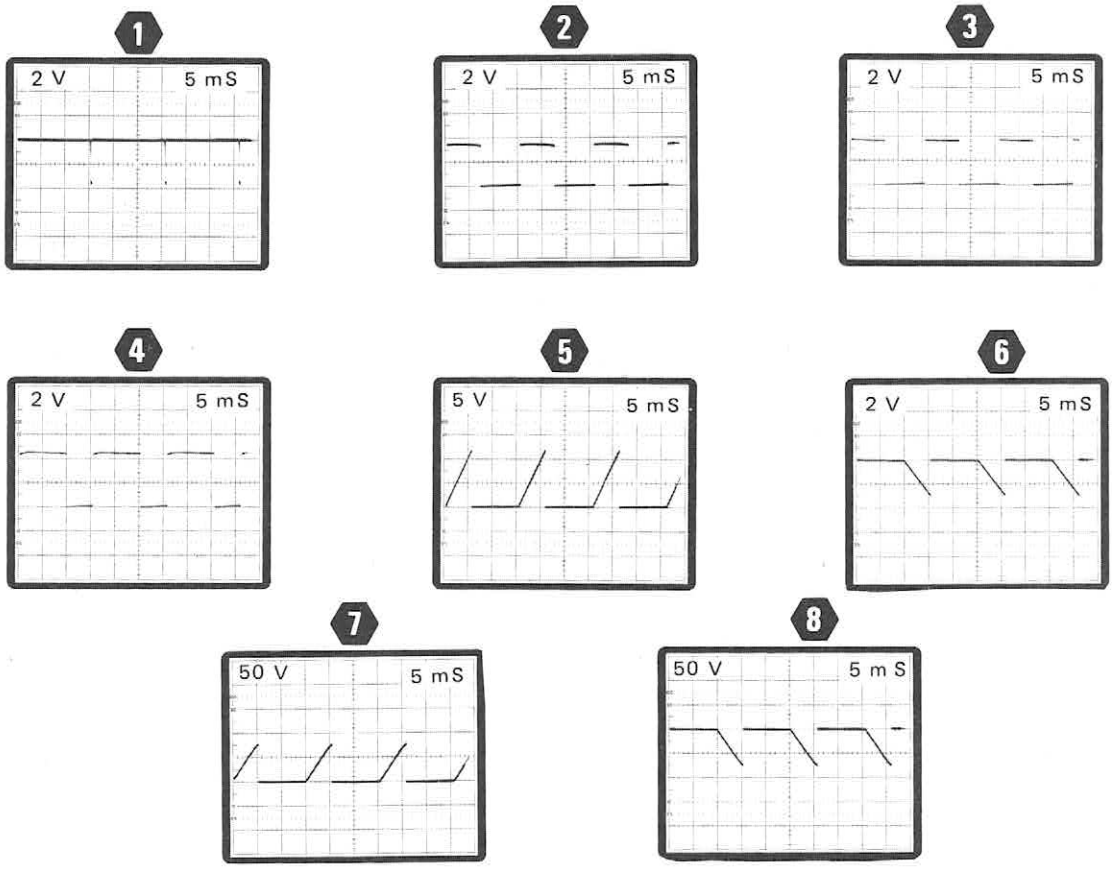
The T912 controls were set as follows:

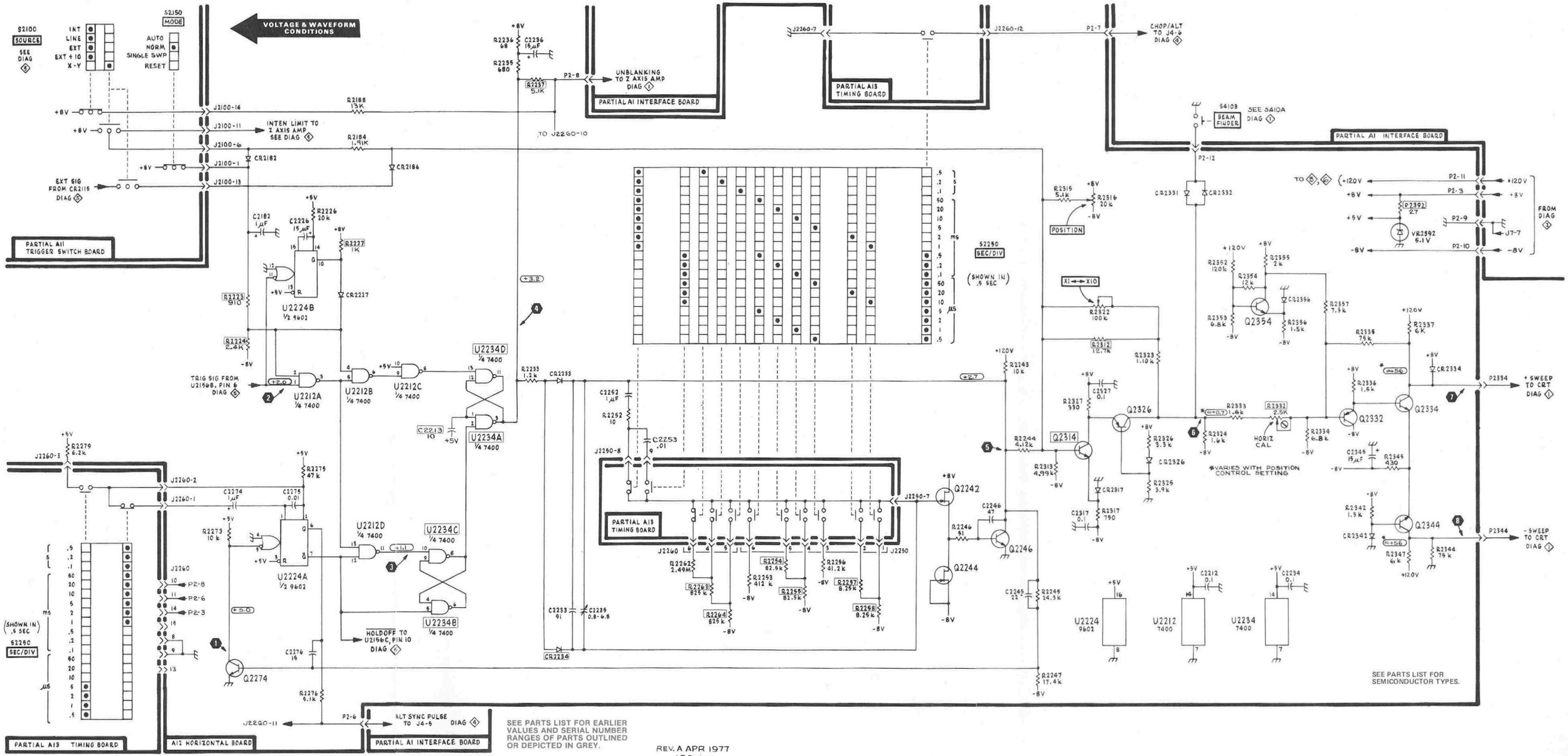
VOLTS/DIV (both)	20 mV
AC-GND-DC (both)	DC
Vertical Mode	DUAL TRACE
SOURCE	LINE
MODE	AUTO
SLOPE	+OUT
SEC/DIV	.5 ms
STORE	Non store (button out)

The other controls were set as needed to obtain a display.

NOTE

To obtain voltages and waveforms on the Horizontal board, the Vertical Amplifier must be operated separately from the instrument using a Vertical Amplifier Extender Troubleshooting Fixture. See Troubleshooting Equipment and Vertical Amplifier Replacement in the Service Information section of this manual.




VOLTAGE & WAVEFORM CONDITIONS
S2100 SOURCE
INT
LINE
EXT
EXT ÷ 10
X-Y
S2150 MODE
AUTO
NORM
SINGLE SWP
RESET
PARTIAL AII TRIGGER SWITCH BOARD
PARTIAL AI INTERFACE BOARD
PARTIAL AI3 TIMING BOARD
PARTIAL AI2 HORIZONTAL BOARD
INTEN LIMIT TO Z AXIS AMP SEE DIAG 4
UNBLANKING TO Z AXIS AMP DIAG 1
CHOP/ALT TO J4-6 DIAG 4
BEAM FINDER SEE 54108 SEE 54IOA DIAG 1
TO 5, 6
FROM DIAG 2
EXT SIG FROM CR2115 DIAG 4
TRIG SIG FROM U2150B, PIN 6 DIAG 4
HOLDOFF TO U2156C, PIN 10 DIAG 4
ALT SYNC PULSE TO J4-5 DIAG 4
TO J2260-10
S2250 SEC/DIV
(SHOWN IN .5 SEC)
S2260 SEC/DIV
POSITION
X1 ↔ X10
HORIZ CAL
*VARIES WITH POSITION CONTROL SETTING
+ SWEEP TO CRT DIAG 1
- SWEEP TO CRT DIAG 1
SEE PARTS LIST FOR SEMICONDUCTOR TYPES.
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
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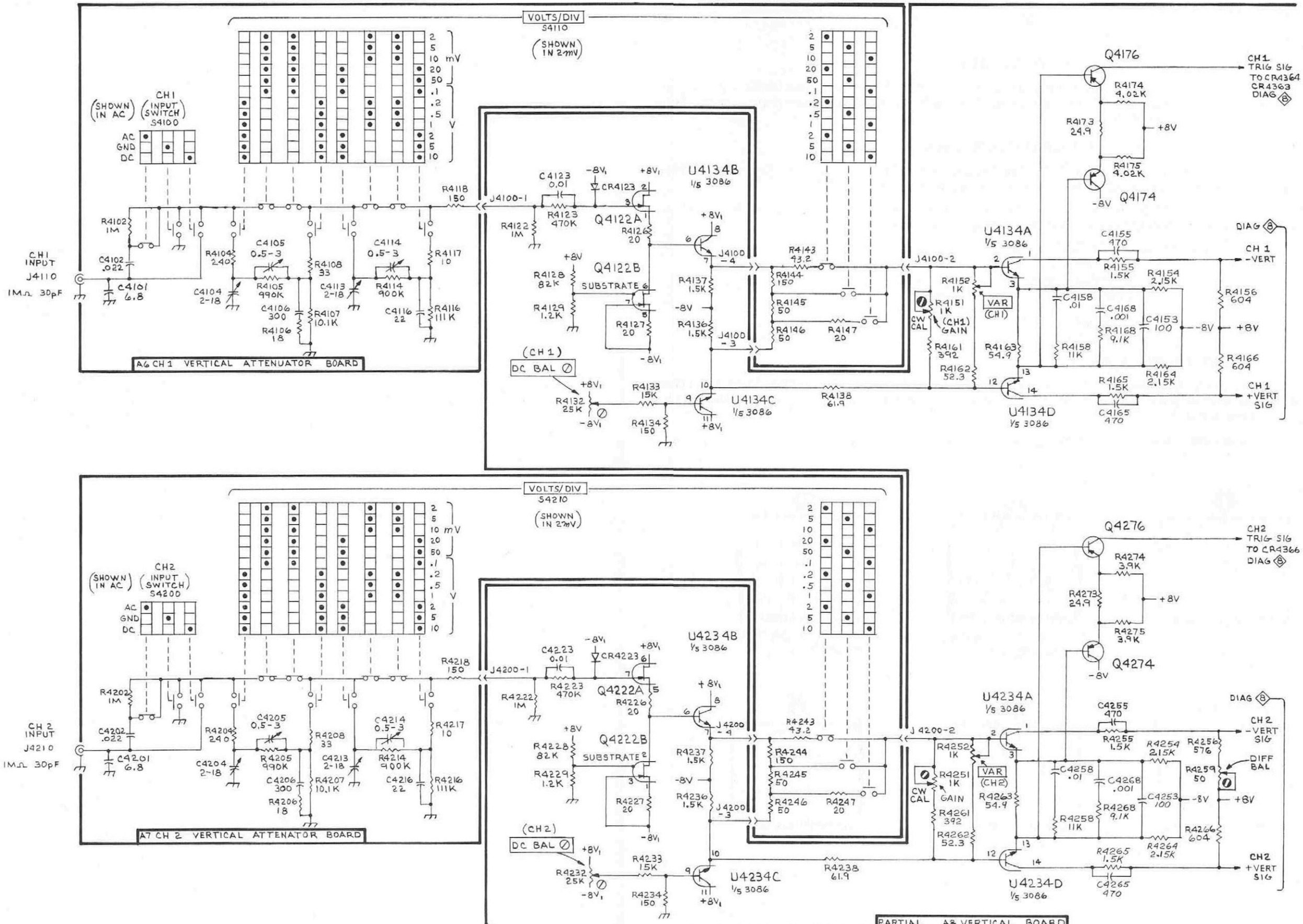
T912
SWEEP & HORIZONTAL AMPLIFIER 6



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OPTION 1 VERTICAL INPUT ⟨7⟩

VOLTAGE CONDITIONS

Voltages shown on this schematic diagram were measured with a TEKTRONIX DM 501 Digital Multimeter. Voltage measurements can vary as much as ±20%. No signals were applied to the vertical input or the X (external trigger) input. See waveform conditions for T912 control settings.

WAVEFORM CONDITIONS

Waveforms below were monitored with a TEKTRONIX 7704A Oscilloscope, 7B71 Time Base, 7A15 Amplifier, and 10X probe. The oscilloscope input coupling was set to ac. Waveforms may vary as much as ±20%.

A 1 kHz, 50 mV sine wave was applied to CH 1 input and a 1 kHz, 50 mV square wave was applied to CH 2 input. A TEKTRONIX FG 501 Function Generator provides either of the input waveforms.

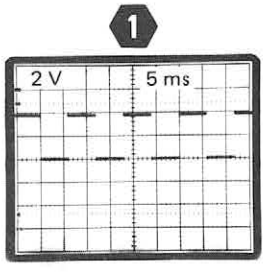
The T912 controls were set as follows:

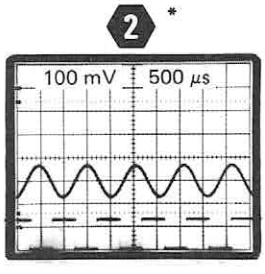
VOLTS/DIV (both)	20 mV
AC-GND-DC (both)	DC
Vertical Mode	DUAL TRACE
SOURCE	INT
MODE	AUTO
SLOPE	+OUT
SEC/DIV	.5 ms

The other controls were set as needed to obtain a display.

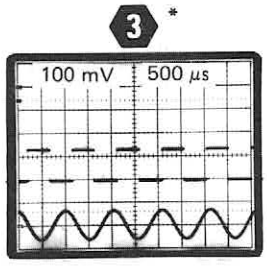
The CH 1 POSITION control was adjusted so that the bottom of the sine wave was on the first horizontal graticule line above the center and the CH 2 POSITION control was adjusted so that the top of the square wave was on the first horizontal graticule line below the center.

***Screen positions for waveforms 2, 3, 4, and 5 are affected by settings of T912 POSITION controls.**





ADJUST TRIGGERING AS NECESSARY



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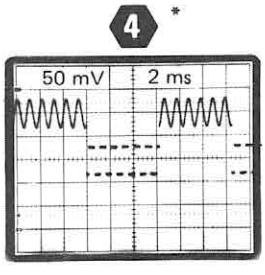

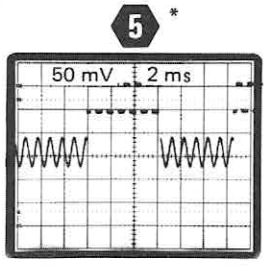

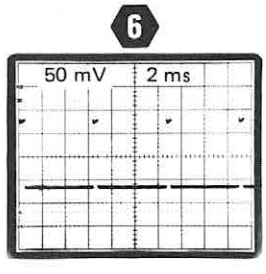

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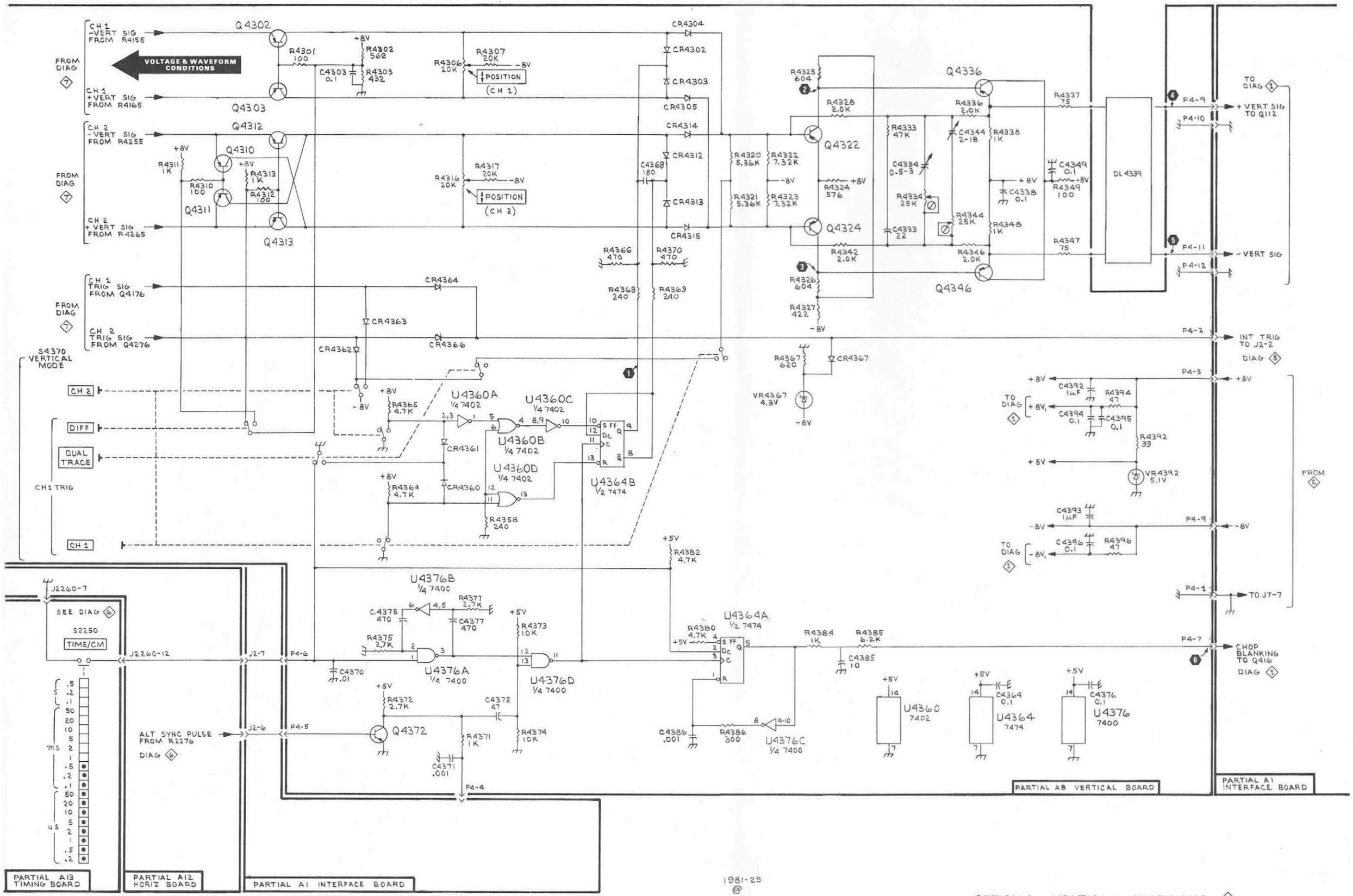

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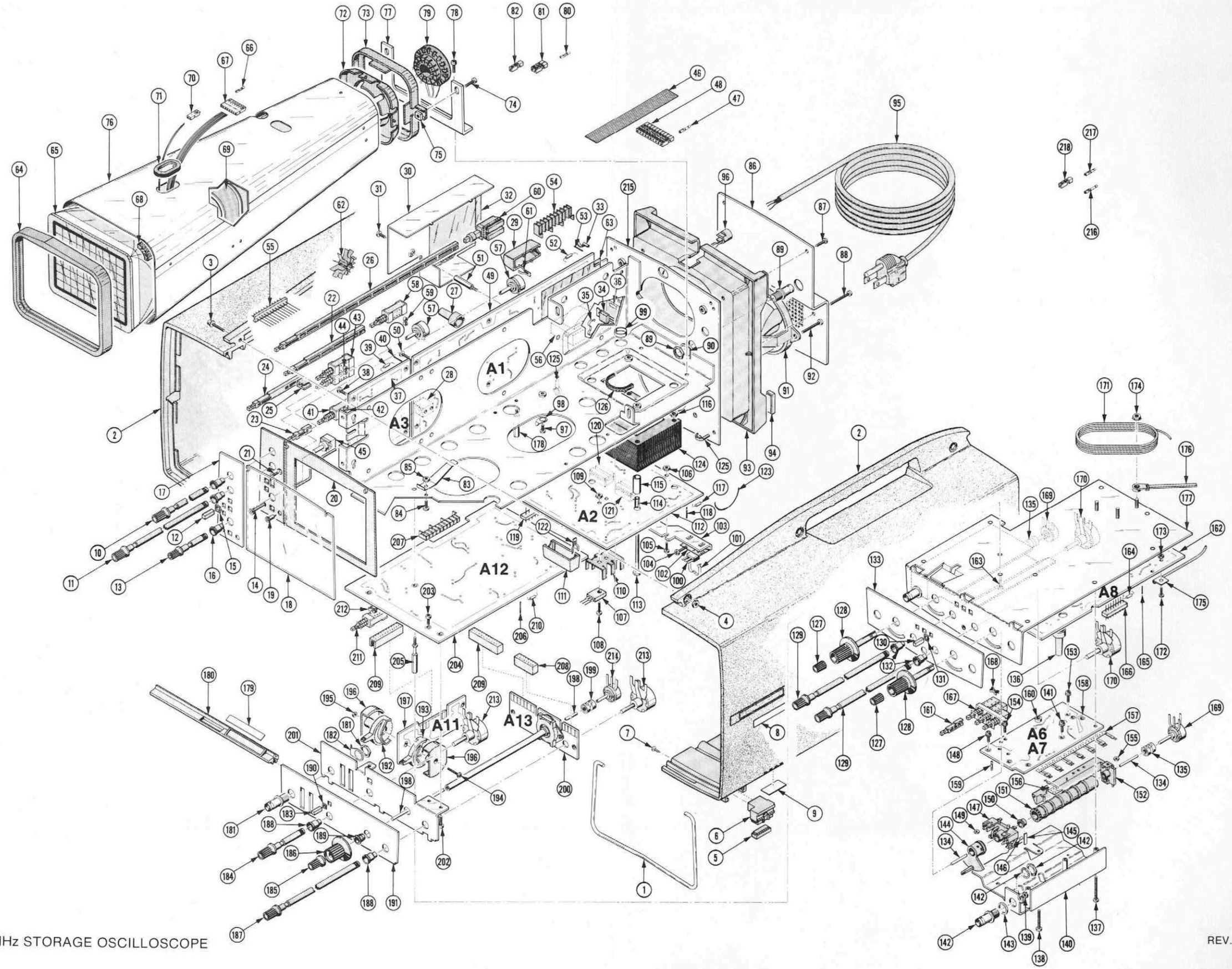
OPTION 1 VERTICAL SWITCHING 8



T912 10 MHz STORAGE OSCILLOSCOPE

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