## TEKTRONIX

TTY PロRT INTERFACE FロR 4010－SERIES TERMINALS WITH<br>INTERDATA 70 COMPUTERS

（ロこ1－ロロ93－ロ2）

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Fig. 1-1. TTY Port Interface.

## MODIFICATION AND INSTALLATION INSTRUCTIONS

## Introduction

This manual describes the circuit changes and interconnections necessary to allow the Tektronix 4010-Series Computer Display Terminals to communicate with Interdata Computer Model 70.

The installation instructions for this computer Interface are divided into two parts. Section 1 of this manual covers the specific modifications and installation; Section 4 gives a procedure for testing the system a part at a time to localize troubleshooting.

The Interface consists of a Control Card, a Relay Card with connectors and mounting hardware, two interconnecting cables, and a computer modification kit.


The computer, Teletype console, and terminal must be turned off before modifying the system.

If the Interface was ordered with the terminal, the installation will already have been completed by the factory. The modifications to the computer will need to be done later in this procedure. Refer to Section 4 for the system checkout. If the Interface is being field-installed, the procedure is as follows:

1. Install the Control Card into the minibus in the Pedestal.


Do not install or remove any cards or boards while the power is on. Severe circuit damage may result.
2. Attach the Relay Card Assembly to the rear panel of the Pedestal using the four screws. If two interfaces are being installed, a two-hole rear panel will be needed (see the Tektronix Dual Interface manual, custom modification, for more detail).
3. Connect the two cables from the Relay Card to the Control Card.
4. Proceed to Section 4 for the system checkout. The following describes the modifications referred to in the checkout.
a. Install all straps on the Control Card as shown in Fig. 1-2.
b. Install all straps on the Relay Card as shown on the Relay Card Diagram.

## General Information

Before installing this Tektronix modification, become familiar with the system by operating some simple programs with the Teletype console. It is best to use programs that exercise turnaround from the INPUT mode to the OUTPUT mode of the Interdata Computer. As a minimum, a "debug" program that executes a core dump will suffice.

## Interdata Computer Adaptation

1. Gain access to the computer circuit boards by removing the Model 70 control panel/cover.
2. Remove the metal bar holding in the boards.
3. Locate the TTY Interface board. This board has a black cable connected between it and the Teletype console.
4. Remove the TTY Interface board from the computer.
5. Remove the Interdata-supplied Teletype cable assembly by loosening the two $4-40$ captive screws and pulling the connector carrier forward.
6. Plug in the Tektronix-manufactured Interface cable assembly, and secure it with the two $4-40$ screws and spacers provided.
(Completely read step 7 before attempting to attach the 5 -wire ribbon connector).
7. The ribbon connector plugs into the Tektronix Interface cable assembly at the 5-pin connector provided. Match the $\Delta$ symbol on the connector housing to the $\Delta$ symbol etched on the circuit board to ensure the proper connector wiring sequence. ICs on the Interdata 70 board are numbered on the circuit etch, e.g., A71, A72, A73, etc. IC number A100 is very close to the 10 -pin AMP connector used by the Teletype cable assembly. To attach the ribbon cable, proceed as follows:
a. Solder the free end of the wht/brn wire to IC A100 pin 14 ( +5 volts).
b. Solder the free end of the wht/red wire to IC A113 pin 4 (R DATA CLAMP).
c. Solder the free end of the wht/orn wire to IC A100 pin 5 (TMGI).
d. Solder the free end of the wht/yel wire to IC A60 pin 13 (CLOCK DISABLE).
e. Solder the free end of the wht/grn wire to IC A60 pin 12 (CLKI).

(NOTE: The original Interdata TTY cable may be replaced at any time. If the 5-pin ribbon connector is allowed to simply hang loose, the Interdata/Teletype console configuration will operate as originally intended. In effect, no electrical modifications are installed until the ribbon cable is plugged into the Tek tronix Interface cable assembly).

## NOTE

If a high-speed reader or magnetic tape cassette unit is interfaced to the terminal bus, it will be desirable to increase the terminal's data transmission baud rate. This necessitates the removal of capacitor C21 ( $2.2 \mu \mathrm{~F}$ ) on the Interdata Teletype Interface board to increase the data receiver bandwidth. Terminal transmission rate is then increased by the variable baud adjustment, R50, until the pulse train at TP1 measures approximately 20 kHz .
8. Plug the Interdata TTY Interface board into the computer mainframe.
9. Replace the metal bar that holds in the Interface board.
10. Pass the cable connected to the Interface board to the rear of the computer and out through the back.
11. Replace the front control panel/cover.

## Switch And Strap Positions

Before connecting the various interconnecting cables, check the Interface unit switch and strap positions listed in Table 1-1 and Fig. 1-2.

TABLE 1-1

| Switch And Strap Positions |  |
| :--- | :---: |
| Strap/Switch |  |
| Interface Card |  |
| BAUD SHIFT | Position |
| TSUP | IN |
| 16X | OUT |
| CLOCK | OUT |
| MAX BAUD | X8 |
| TSL | 154 |
| INPUT | IN |
| INTERFACE CLOCK | 232 |
| TDATA | NORMAL |
| R DATA | INVERT |
| TAPEFETCH | INVERT |
| CLEAR TO SEND | OUT |
| READER ON | HIGH |
| ECHO | NORMAL |

TABLE 1-1 (cont)
Switch And Strap Positions

| Strap/Switch | Position |
| :---: | :---: |
| Interface Card |  |
| PARITY | $A$ to $A B ; C$ to $C D$ |
| BIT 8 | IN |
| TTY MASTER OPT | No Strap |
| Back Panel |  |
| AUX/TTY (S7) | TTY |
| Relay Board |  |
| CLEAR TO SEND | No Strap |
| TTY LEVEL | D to G |
| PULL UP/DOWN | No Strap |
| TTY REC DATA | $100 \Omega, 1 / 2 \mathrm{~W}$ resistor, B to C |
| Potentiometer Adjustments |  |
| Interface Card |  |
| 880 Hz | 880 Hz at TP2 |
| VAR BAUD RATE | Approximately 3 kHz at TP1 |

## Terminal Adaptation

1. Connect the cable (012-0313-00 or optional 012-0312-00) from the Interdata TTY Interface board to J261 of the Tektronix terminal.
2. Connect the Interdata Teletype console to J267 on the rear of the terminal using cable 012-0311-00.
3. This concludes the electrical connection of the terminal/Interdata Interface. Before turning the power on, check all switch and strap positions according to Table 1-1 and Fig. 1-2. Refer to the terminal Users Manual for specific operating instructions.

## Circuit Description

Connector Board Circuitry. The SN7474N flip-flop performs a dual function. When not being cleared by signal TMGI (low clearing), the output at CLKI is a 4 X baud-rate clock.

Prior to this modification, the signal DAO did several things. On its falling edge, it cleared the parallel-to-shift register in the TTY board, and transferred data in parallel into that register. The rising edge made TMGI go high, enabling the oscillator (now disabled) to oscillate. It also opened the gate for the start bit to go on the line, since the design assumed that the Teletype console was always ready, and it changed the status of the BYSI signal to tell the processor that the TTY controller was not ready to accept another character.

When the terminal runs at 154 K baud, it is sometimes writing a character or making a vector, and is not ready. This is indicated to the computer by the absence of Interface Clock. The signal R DATA CLAMP holds the start bit off the output data line until the Interface Clock is again started to the terminal. R DATA CLAMP is controlled by TMGI and X8 clock via one-half the SN7474N and the SN75451 open collector driver.

## ELECTRICAL PARTS LIST

Replacement parts should be ordered from the Tektronix Field Office or Representative in your area. Changes to Tektronix products give you the benefit of improved circuits and components. Please include the instrument type number and serial number with each order for parts or service.

## ABBREVIATIONS AND REFERENCE DESIGNATORS

| A | Assembly, separable or repairable | $\mathrm{FL}$ | Filter | PTM | paper or plastic, tubular molded |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AT | Attenuator, fixed or variable |  | (heat sink, etc.) | R | Resistor, fixed or variable |
| B | Motor | HR | Heater | RT | Thermistor |
| BT | Battery | J | Connector, stationary portion | S | Switch |
| C | Capacitor, fixed or variable | K | Relay | T | Transformer |
| Cer | Ceramic | L | Inductor, fixed or variable | TP | Test point |
| CR | Diode, signal or rectifier | LR | Inductor/resistor combination | U | Assembly, inseparable or |
| CRT | cathode-ray tube | M | Meter |  | non-repairable |
| DL | Delay line | Q | Transistor or silicon- | V | Electron tube |
| DS | Indicating device (lamp) |  | controlled rectifier | Var | Variable |
| Elect. | Electrolytic | P | Connector, movable portion | VR | Voltage regulator (zener diode, |
| EMC | electrolytic, metal cased | PMC | Paper, metal cased |  | etc.) |
| EMT | electrolytic, metal tubular | PT | paper, tubular | WW | wire-wound |
| F | Fuse |  |  | Y | Crystal |


| Ckt. No. | Tekłronix Part No. | Serial/Model Eff | No. Disc | Description |
| :---: | :---: | :---: | :---: | :---: |
| CONNECTORS |  |  |  |  |
| $\mathrm{J} 2671^{1}$ | 131-0458-00 |  |  | Receptacle, electrical, 15 pin, female |
| P261 ${ }_{2}$ | $131-0570-00$ |  |  | Receptacle, electrical, 25 pin, male |
| P267 ${ }^{2}$ | 131-0459-00 |  |  | Receptacle, electrical, 15 pin, male |
| ASSEMBLY |  |  |  |  |
|  | 670-1982-00 |  |  | TELETYPE RELAY Circuit Board Assembly |
| CAPACITORS |  |  |  |  |
| C5 | 283-0177-00 |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C6 | 283-0178-00 |  |  | $0.1 \mu \mathrm{~F}$, Cer, $100 \mathrm{~V},+80 \%-20 \%$ |
| DIODE |  |  |  |  |
| CR5 | 152-0185-00 |  |  | Silicon, selected from 1N4152 or 1N3605 |
| CONNECTOR |  |  |  |  |
| J261 | 131-0812-00 |  |  | Receptacle, electrical, 25 pin, female |
| RELAY |  |  |  |  |
| K5 | 148-0045-00 |  |  | Armature, $12 \mathrm{VDC}, 185 \Omega$ coil |
| RESISTORS |  |  |  |  |
|  |  |  |  |  |
| $B-C^{3}$ | 315-0101-00 |  |  | $100 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| SWITCH |  |  |  |  |
| S3 | 260-1206-00 |  |  | Togg1e |
| 1Supplied with 012-0433-00, interconnecting cable.3 Supplied with 012-0311-00, interconnecting cable.Resistor |  |  |  |  |


| Ckt. No. | Tektronix Part No. | Serial/Model Eff | No. Disc | Description |
| :---: | :---: | :---: | :---: | :---: |
| ASSEMBLY |  |  |  |  |
|  | 670-2930-00 |  |  | CLOCK Circuit Board Assembly |
| CAPACITOR |  |  |  |  |
| C16 | 283-0177-00 |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| DIODE |  |  |  |  |
| CR10 | 152-0141-02 |  |  | Silicon, 1N4152 |
| TRANSISTORS |  |  |  |  |
| Q10 | 151-1021-00 |  |  | Silicon, FET, selected from 2N4391 |
| Q12 | 151-0190-00 |  |  | Silicon, NPN, 2N3904 or TE3904 |
| RESISTORS |  |  |  |  |
| R10 | 315-0302-00 |  |  | $3 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R12 | 315-0752-00 |  |  | $7.5 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R14 | 315-0302-00 |  |  | $3 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| INTEGRATED CIRCUITS |  |  |  |  |
| U10 | 156-0041-00 |  |  | Dual 15 MHz D-type pos.-edge-trig. flip-flop, SN7474N |
| U12 | 156-0094-00 |  |  | Dual peripheral driver, SN75451P |




[^0]| Index No. | Tektronix <br> Part No. | Serial/Model No. Eff Disc | $\begin{aligned} & Q \\ & t \\ & y \end{aligned}$ |  | 23 | 4 | Description |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 211-0016-00 |  | 2 | SCREW, 4-40 x 0.625 inch, PHS |  |  |  |  |
| 52 | 131-0589-00 |  | 5 | TERMINAL, pin, 0.46 inch long |  |  |  |  |
| 53 | 131-0621-00 |  | 6 | CONNECTOR, terminal |  |  |  |  |
| 54 | 352-0201-01 |  | 1 | HOLDER, terminal connector, 5 wire (brown) HOLDER, terminal connector, 5 wire (red) |  |  |  |  |
|  | 352-0201-02 |  | 1 |  |  |  |  |  |
|  | 020-0076-00 |  | 1 | COMPONENT KIT (not shown) |  |  |  |  |
|  | - - - |  | - | component kit includes: |  |  |  |  |
|  | 131-0707-00 |  | 5 | CONNECTOR, terminal |  |  |  |  |
|  | 352-0163-00 |  | 1 | HOLDER, terminal connector, 5 wire |  |  |  |  |
|  | 175-0828-00 |  | ft | WIRE, electrical, 5 wire ribbon, 1 foot |  |  |  |  |

ACCESSORIES
1 MANUAL, instruction



## DESCRIPTION

## Introduction

The Teletype Port Interface allows the 4010-Series Computer Display Terminals to communicate with a computer through the same port used by teletype machines. It places a relay circuit in the path between the teletype machine and the computer, permitting either the Terminal or the teletype machine to be selected for operation.

The Interface accepts parallel data from the Terminal, converts it to serial data and sends it to the computer. Conversely, it receives serial data from the computer, converts it to parallel data, and places it on the Terminal data bus lines.

Clock circuits within the Interface control input and output rates, and provide an Interface Clock signal for use by the computer. More detail regarding the clock circuits can be found in the Clock Information Section.

In an auxiliary mode of operation, the Interface acts as a link between the computer to which it is dedicated, and a second computer which is connected through a second interface. The second interface may be any of the various types designed for use in the Terminal.

The Teletype Port Interface consists of a Control Card which fits into the Terminal Pedestal, a Relay Board and cable assembly which is built into a Mounting Bracket, a modification kit for the computer, and cables as necessary to complete the installation. The Control Card contains numerous strappable options, and the Relay Board has several soldered options. These options are connected as required for the specific computer installation. The Mounting Bracket fastens into the Terminal pedestal, making its control switch, the computer cable connector, and the teletype cable connector externally accessible at the back surface of the pedestal.

## Control Card Block Description

The control card consists principally of Receiving, Transmitting, and Timing Circuitry. Timing is controlled by the 4.9 MHz from the terminal, the TTY Clock, or the Transmit Clock. Any one of the three sources may be used to control the Interface Clock. The Clock Select Multiplexer U21, permits one of the three sources to be applied to Receive Maximum Baud Counter U23. The counter outputs the same frequency as either the TTY Clock or the Transmit Clock, but divides down the 4.9 MHz Clock. This output is applied to the Interface Clock and to the Receive Sync circuit. With the 16X option out, the input to U9 and U25A is divided by 8 before it is applied to the Transmit and Receive circuits. The proper Transmit and Receive frequencies are selected in the Interface Clock and sent to the computer. This signal is normally 1 to 16 times the Transmit or Receive rate depending upon computer requirements.

Clock Select device U21 is controlled by Transmit Detect Gate U99A and Baud Shift Strap, Receive Circuit U41A, and Teletype Select Circuit U31D.

## Description-TTY Port Interface

The Transmit Circuitry latches data entered on the Bit 1 through Bit 8 lines. When a $\overline{C S T R O B E}$ arrives the data is strobed to the outputs of U69 and U89. These outputs drive the transmit shift registers and the bit 8 parity checker. Data bits are sequentially clocked out of U17A and passed through the transmit level changer to provide the serial data for the computer. When transmission has been completed, U37A provides a high output, indicating that another character may be loaded. It also causes the Clock Select to change its output if the Baud Shift Strap is at the IN position.

One of the circuits associated with transmission is the Break circuit. At any time the Break signal is received, it holds U17B zero-set. If the interface switch is at the TTY position and the INTF signal is received, U37D is disabled. Additional data cannot pass through it and a Break signal is held on the $T$ DATA line until the Break signal is removed and U17A has clocked twice to one-set U17B.

The Receive Circuitry consists of the level changer, sync, shift register, and bus gates. Under quiescent conditions, the Receive Register flip-flops are all zero-set. The first one contains a Stop Bit and the rest have been zero-set by the pulse from U35B. As long as the R DATA IN line does not contain information, the clock pulses from U25A continuously clock these zeros through the Receive Register. When a Start Bit arrives on the R DATA IN line, U25A is reset to begin a new count cycle. Highs and lows are then received on the R DATA IN line according to the character being received. These are clocked through the Receive Register until the Stop Bits are received.

Miscellaneous Circuits. The TAPEFETCH signal permits a high speed reader to input data through the interface. The TAPEFETCH option strap must be at the IN position and a $\overline{\text { READ TAPE signal must be }}$ received through Q35. However, many TTY PORT interfaces use the CLEAR TO SEND level changers to drive the TAPEFETCH gate. If the TSL strap (teletype strap) is at the IN position, $\overline{R E A D ~ T A P E ~ s i g n a l ~ a l s o ~}$ causes a high from U29C which does a number of things. It causes the Clock Select circuit to accept the TSL Clock for the output of U21. It causes U33A to deliver a low to U19A and Q21. This causes TERMI. $\overline{\text { NAL SELECT }}$ and TTY RELAY to both go high, selecting the teletype for operation rather than the terminal's high speed tape reader. The U7 output goes low for a brief period of time, preventing Clock pulses from passing through during switch-over time. When the READ TAPE signal is removed, U23A is disabled until switch-over to terminal operation has been accomplished.

INDICATOR 1 goes low whenever CLEAR TO SEND condition exists, or whenever data is ready to be transmitted. INDICATOR 2 exists whenever a complete character is contained in Receive Register.

## Operating Modes

To avoid computer damage, the computer must be turned off before connecting the Terminal system to the computer.

Operating modes of the Terminal equipped with a TTY Port Interface are controlled principally by the Interface switch (back surface of the pedestal and by the keyboard LOCAL/LINE switch. The following modes can be achieved):

| MODE | INTERFACE <br> TTY/AUX <br> SWITCH | KEYBOARD <br> LOCAL/LINE <br> SWITCH | OTHER |
| :--- | :---: | :---: | :---: |

The Terminal Mode permits normal transfer of data between the computer and the Terminal, with the teletype machine inactivated.

The Local (Teletype) Mode suppresses the Interface and permits normal interchange between the teletype and the computer.

Auxiliary Mode causes data input to the Teletype Port Interface to be sent to a second interface, where it is routed to a second computer without being acted on by the Terminal. The data input can be from any source, including the keyboard or the Teletype Port Interface's computer. Data returned by the second interface is routed to the Teletype Port Interface's computer. The TTY Master Option strap cannot be connected to the second interface in this mode. (In this mode, the Terminal responds only to data received from the second interface if the AUX TSUP strap is OUT. If AUX TSUP is $I N$, the Terminal is blanked to all inputs.)

Tape Reading Mode permits tape inputs from a peripheral reader (Terminal Mode).

Break Mode occurs whenever the system is in Terminal Mode and the BREAK key is pressed. The Break condition exists for a minimum of 1.1 ms longer than the BREAK key is held down. The INTERFACE CLOCK signal is changed to 110 Hz (or an appropriate multiple) during Break Mode, and a steady spacing signal (high) appears on the Interface output line (T DATA strap in NORM position).

## Clock Information

Three clock sources are provided in the Interface-a fixed 4.9 MHz from the Terminal, an 800 Hz to 25 kHz Variable Oscillator, and an 880 Hz TSL (Teletype Select) Oscillator. These sources are used as follows:

CLOCK IMPLEMENTATION

| Clock | Baud Shift Strap Position |  |  |
| :--- | :--- | :--- | :--- |
|  | OUT | IN | ON |
| Fixed |  |  |  |
| $(4.9 \mathrm{MHz})$ | Controls baud rate <br> and INTERFACE <br> CLOCK rate during <br> transmit and receive | Controls baud rate <br> and INTERFACE <br> CLOCK rate during <br> receive | Controls baud rate <br> and INTERFACE <br> CLOCK rate during <br> transmit |
| Variable |  | Controls baud rate <br> and INTERFACE <br> CLOCK rate during <br> transmit and receive |  |
| $>25 \mathrm{kHz})$ |  | Controls INTERFACE CLOCK rate in Teletype Mode and during Break Mode |  |

## Description-TTY Port Interface

Regardless of which clock source is used, the clock signal passes through a strap option (16X) which divides it down by 8 (16X OUT) before it is applied to either the transmit or receive register circuitry. This transmit/receive clock signal is equal to, or is a sub-multiple of the INTERFACE CLOCK signal, with relationship being expressed by the Clock strap option position (X1, X2, X4, or X8). In some computer installations, the INTERFACE CLOCK must be sixteen times the transmit/receive frequency. Then the 16 X strap option is placed IN and a strap is connected between the 16X OUT pin and the output connection of the Clock option.

The 4.9 MHz clock is affected by one other option-the MAX BAUD strap. With the 16 X option OUT, MAX BAUD provides one of the following transmit/receive rates: $307,154,77,38$, or 19 kHz . If the 16 X option is IN, these rates are reduced to one half the value stated for any one position of the MAX BAUD strap. As stated in the previous paragraph, the Clock option provides a selected multiple of the rate for the INTERFACE CLOCK signal.

Conventional transmit/receive frequencies and INTERFACE CLOCK frequencies available from the three sources are listed in the following tables:

FIXED SOURCE OUTPUTS

| $\begin{gathered} \text { MAX BAUD } \\ \text { Strap } \\ \text { Position } \\ \hline \hline \end{gathered}$ | Transmit/Receive Frequency (kHz) |  | INTERFACE CLOCK Freq ( kHz ) |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{gathered} \hline \text { CLOCK } \\ \times 1 \end{gathered}$ | $\begin{gathered} \hline \text { CLOCK } \\ \times 2 \end{gathered}$ | $\begin{gathered} \text { CLOCK } \\ \text { X4 } \end{gathered}$ | $\begin{gathered} \hline \text { CLOCK } \\ \text { X8 } \end{gathered}$ |
|  | 16X OUT | ${ }^{1} 16 \mathrm{X}$ IN |  |  |  |  |
| 307 | 307 | 154 | 307 | 614 | 1228 | 2456 |
| 154 | 154 | 77 | 154 | 307 | 614 | 1228 |
| 77 | 77 | 38 | 77 | 154 | 307 | 614 |
| 38 | 38 | 19 | 38 | 77 | 154 | 307 |
| 19 | 19 | 9.7 | 19 | 38 | 77 | 154 |

VARIABLE SOURCE OUTPUTS

${ }^{1}$ Normally used only in conjunction with CLOCK X8.

TSL SOURCE OUTPUTS

| Oscillator <br> Frequency | INTERFACE CLOCK Frequency |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | CLOCK <br> X1 | CLOCK <br> X2 | CLOCK <br> X4 | CLOCK <br> X8 |
|  | 110 | 220 | 440 | 880 |
| ${ }^{2} 1760 \mathrm{~Hz}$ |  |  |  | 1760 |

[^1]
## Switches

The only switch inherent to the Interface is the TTY-AUX switch which is located on the Interface mounting bracket, accessible at the back of the pedestal. It provides mode control as follows:

## Switch Position TTY

OFF

AUX Permits dedicated computer to communicate with a second computer if a second interface is installed and the LOCAL/LINE switch is at LINE; TTY Master Option must not be connected to second interface or it will be suppressed.

## Operation

Selects Terminal Mode when Terminal switch is at LINE; selects teletype for operation with the computer when the Terminal switch is at LOCAL; TTY Master Option must be connected to suppress other installed interfaces.

Unmarked mid-position; isolates the Terminal and connects the teletype to the computer.

## Indicators

Although no indicators are included with the Interface, it does control INDICATOR 1 and INDICATOR 2 (second and third from left on the Terminal keyboard). INDICATOR 1 represents computer busy. It lights in response to data being loaded in the output latches or in response to a false CLR TO SEND signal. INDICATOR 2 responds to the Terminal being busy. It lights whenever a complete character is contained in the input register.

## Test Points

Test points on the Control Card provide access to the following signals:

## Options on Control Card

Listed as positioned from left to right on the circuit card.

## Option

## Function

16X

AUX TSUP

BAUD SHIFT AUX position. OUT permits normal operation.

IN selects Fixed receiving rate and Variable transmit rate.
OUT selects Fixed rate for both transmit and receive.
ON selects Variable rate for both transmit and receive.

Variable Oscillator output
TSL Oscillator output
High equals clear to send
INTF signal from rear-panel switch

| TP 1 | Variable Oscillator output |
| :--- | :--- |
| TP 2 | TSL Oscillator output |
| TP 3 | High equals clear to send |
| TP 4 | INTF signal from rear-panel switch |

IN position asserts $\overline{T S U P}$, inhibiting Terminal display when back panel switch is in

OUT provides relationship between INTERFACE CLOCK and transmit/receive rate as indicated by Clock option; IN provides an INTERFACE CLOCK which is 16 times the transmit/receive rate, if the OUT position of the 16 X option is connected to the Clock option output (center) pin. With IN selected, all values indicated by the MAX BAUD option are reduced to half the value indicated on the board.

| Option | Function |
| :---: | :---: |
| CLOCK | Determines the relationship between the INTERFACE CLOCK and the transmit/receive rate. Options are $\mathrm{X} 1, \mathrm{X} 2, \mathrm{X} 4$, and X 8 . |
| MAX BAUD | Selects Fixed transmit/receive rate of $19 \mathrm{k}, 38 \mathrm{k}, 77 \mathrm{k}, 154 \mathrm{k}$, or 307 k baud. The rate decreases to one half the value indicated when the 16 X option is IN. |
| TSL | OUT position only generates TAPEFETCH signal (if strapped IN) in response to $\overline{R E A D ~ T A P E ~ s i g n a l . ~ I N ~ p o s i t i o n ~ c a u s e s ~ t h e ~ f o l l o w i n g ~ a d d i t i o n a l ~ f u n c t i o n s: ~ s e l e c t s ~}$ TSL Clock source; causes Relay Card to select teletype operation. |
| INPUT | Selects appropriate level conversion for TTY or RS232 compatibility. |
| INTERFACE CLOCK | Selects polarization of INTERFACE CLOCK signal with respect to transmit/receive data. NORMAL selects an in-phase condition while INVERT selects $180^{\circ}$ phase relationship. |
| BIT 8 | With ON selected, bit 8 is sent as data. With IN selected, bit 8 is determined by the SEND 8 signal; it is sent as data with SEND 8 low, and is sent as a space or mark (depending on PARITY option) when SEND 8 is high. |
| T DATA | NORMAL transmits mark as negative voltage; INVERT transmits mark as positive voltage. |
| PARITY | Effective only with BIT 8 option IN and $\overline{\text { SEND } 8}$ high. It then provides the following: |
|  | STRAP POSITIONS BIT 8 |
|  | AB to $A, C D$ to $C$ Mark <br> $A B$ to $B, C D$ to $C$ Odd Parity <br> $A B$ to $A, C D$ to $D$ Even Parity <br> $A B$ to $B, C D$ to $D$ Space |
| R DATA | Choice of NORMAL (mark positive voltage) or INVERT (mark negative voltage) input data. |
| TAPE FETCH | IN position allows $\overline{\text { READ TAPE }}$ input signal to control the TAPE FETCH output signal. OUT position holds high on TAPE FETCH line. |
| CLEAR TO SEND | HIGH accepts high-true CLR TO SEND signals and LOW accepts low-true CLR TO SEND signals, regardless of whether received on the positive or negative bus line. Positive bus input must be grounded (via a strap or the Relay Card) if negative bus is in use. Option must be connected to high if neither bus is in use. |
| READER ON | NORMAL for high-true or INVERT for low-true READ TAPE signal; controls $\overline{\text { READER ON }}$ output, which controls TAPE FETCH if strapped IN, and/or teletype switchover if TSL is strapped IN. |
| ECHO | IN causes local display of data transmitted by the Terminal; OUT does not provide local echo. |

## Option

## Function

TTY MASTER OPT
Selects which bus line (or lines) imposes suppression signal on Terminal minibus when TTY operation is selected by TTY/AUX switch; typically set to SP1. Suppression signal inactivates other interfaces connected to bus line.

## Options on TTY Relay Board

CLEAR TO SEND
Selects positive or negative CLEAR TO SEND bus. A to $D$ accepts positive bus; $B$ to $D$ and $A$ to $C$ accepts negative bus and grounds positive bus.

## TTY LEVEL

Selects voltage level to be placed on the teletype receive data line during Terminal operation: D-G ground; F-H, +5 V ; E-I, -15 V . (Values given are typical. Actual values are determined by the computer.)

## PULL UP/DOWN

Pulls Terminal R DATA line low ( $B$ to $A$ ), or high ( $B$ to $C$ ), if strapped.

## TTY REC DATA

If $B$ to $C$ is strapped, connects the teletype R DATA line to preset level (determined by TTY LEVEL strap) during Terminal operation. If $A$ to $C$ is strapped, connects teletype R DATA line to AC ground, via $0.1 \mu \mathrm{~F}$. If A to B is strapped, provides level selected by TTY LEVEL strap on pin 7 of board's teletype connector.

## Cable and Connector Information

The computer cable connects to J261 on the Interface's TTY Relay Board, and the teletype machine cable connects to a second connector on the TTY Relay Board mounting bracket. This second connector has a cable which fastens to J164 on the TTY Relay Board. Two cables, soldered to the same board, go to the Interface's TTY Control Card, where they connect to J161 and J162. The TTY Control Card connects to the Terminal through a minibus connector. Details regarding J261 are provided here. Refer to the schematic for J161, J162, and J164 details, and to the Terminal Manual for minibus details.

## J261 CONNECTOR INFORMATION

| (Required Circuits) |  |
| :--- | :--- |
| Pin | Signal |
| 1 | Protective Ground (Frame) |
| 2 | Transmitted Data (T DATA) |
| 3 | Received Data (R DATA) |
| 4 | Teletype Transfer Relay (TTY RELAY) |
| 5 | READ TAPE (Customer Applied Option) |
| 6 | CLR TO SEND (POS BUS) |
| 7 | Signal Ground (GND) |
| 12 | CLR TO SEND (NEG BUS) |
| 15 | INTERFACE CLOCK |
| 19 | $-15 V$ (RELAY RETURN) |

## Description-TTY Port Interface

## Accessories

## Standard

1 Instruction Manual (Number varied to conform with specific applications.)

## SPECIFICATIONS

## Electrical Specifications

## Communications Mode

Serial data transfer. Start-stop asynchronous.

## Data Signal Conversión

## T DATA

Converted from 8 bit parallel form to serial form; bit 8 may be converted to parity.

## R DATA

Converted from 8 bit serial form to parallel form.

## Data Bit Format



## Receiving

1 start bit, 7 data bits, 1 parity bit (or data bit), 1 or more stop bits.

## Transmitting

Same format as Receiving but transmits 2 stop bits.

## T DATA

Strappable option permits normal or inverted signal operation.

## Normal

$$
\text { Mark, } \leqslant-5 \mathrm{~V} \text {; Space, } \geqslant+5 \mathrm{~V}
$$

Inverted
Mark, $\geqslant+5 \mathrm{~V}$; Space, $\leqslant-5 \mathrm{~V}$.

## R DATA

Strappable option permits normal or inverted signal operation. A second strap option permits RS232 or TTY compatibility operation.

## Specifications-TTY Port Interface

232 Input Impedance
$4.7 \mathrm{k} \Omega$.

## 232 Normal Levels

Mark, 0 to -25 V ; Space, +3 V to +25 V .
232 Inverted Levels
Mark, +3 V to +25 V ; Space, 0 to -25 V .
TTY Input Impedance
$750 \Omega$ to -15 V .

## TTY Normal Levels

Mark, +15 V to -1 V ; Space, -8 V to -25 V .
TTY Inverted
Mark, -8 V to -25 V ; Space, -15 V to -1 V .

## CLR TO SEND

Either polarity input may be selected.
Positive Bus (J261, Pin 6)
$1 \mathrm{k} \Omega$ to +5 V , TTL compatible. Presents an equivalent 3 TTL load to driving circuit.
Negative Bus (J261, Pin 12)
$4.7 \mathrm{k} \Omega$ to -15 V . Suitable for open-collector PNP (grounded emitter) driving circuit.

## READ TAPE

Either polarity can be selected as active by READER ON option strap. Active signal activates high speed tape reader with TAPE FETCH option IN, or puts Terminal in Local Mode and activates teletype with TSL option strap IN.

## Input Characteristics

$4.7 \mathrm{k} \Omega$ to +15 V . Presents an equivalent 2 TTL load to driving circuit. If left open, remains at a +7 V level.

Level Requirements

$$
\leqslant+0.8 \mathrm{~V} \text { and } \geqslant+2.4 \mathrm{~V}
$$

## BREAK

Causes a break interval of 1.1 to $\mathbf{2 . 2}$ ms longer than the Break key is held down.

## Timing

See Clock Information (Section 2) for additional details.

## Transmitted Data

With Baud Shift strap OUT, it is controlled by a sub-harmonic of the Terminal's 4.9 MHz clock.

With Baud Shift strap IN or ON, it is controlled by the Interface's Variable oscillator, or a sub-harmonic of it.

## Received Data

With Baud Shift strap OUT or IN, it is controlled by a sub-harmonic of the Terminal's 4.9 MHz clock.

With Baud Shift strap ON, it is controlled by the Interface's Variable oscillator.

## INTERFACE CLOCK (TTL Compatible; Fanout of 4)

On Line Mode, Transmit/Receive: A multiple ( $\mathrm{X} 1, \mathrm{X} 2, \mathrm{X} 4$, or X 8 ) of the transmit/receive baud rate, as determined by the position of the Clock strap. The INTERFACE CLOCK signal is interrupted after receipt of a character for only such time as is required by the Terminal to process the data, thus maximizing the receiving rate. The clock stops in either a logical one ( $\geqslant 3 \mathrm{~V}$ ) or logical zero ( $\leqslant 0.5 \mathrm{~V}$ ) as selected by Interface Clock strap.

On Line Mode, Not Transmitting or Receiving: INTERFACE CLOCK is controlled by a sub-harmonic of the Terminal's 4.9 MHz clock when the Baud Shift strap is OUT or IN. It is equal to the Interface's Variable oscillator frequency or a sub-haromnic of it when the Baud Shift strap is ON.

Local Mode: Equal to the Interface's TSL oscillator frequency or a sub-harmonic of it.

## Oscillators

Fixed (4.9 MHz)
Refer to the Terminal User's Manual for specifications.
Variable
Range: $\leqslant 800 \mathrm{~Hz}$ to $\geqslant 25 \mathrm{kHz}$.
Accuracy: Within $\pm 5 \%$ of initial setting.
TSL (Teletype Select)
Range: $\leqslant 800 \mathrm{~Hz}$ to $\geqslant 1200 \mathrm{~Hz}$; normally set to 880 Hz . (The oscillator must be physically changed to convert to 1760 Hz , as is required by some installations.)

## Environmental Specifications

Conform with those for the 4010 series Terminals.

## INSTALLATION and SYSTEM CHECKOUT

If the following steps are taken in sequence, a TTY Port Interface installation will progress smoothly and in a logical manner. Installation will proceed with various sub-sections checked out at each phase of the procedure. Specific installation details referred to in this procedure are given in Section 1.

1. Before attempting any installation, check the Terminal in "LOCAL" mode. Normal responses can be found in the Users Manual or the handbook "Talking to the Computer".
2. Next attach a "mini-modem" and checkout the Terminal "LINE". The mini-modem connection is accomplished by connecting pins 2 (T Data) and 3 ( R Data) together at the interface connector J261. Successful "looping" of data will be accomplished only if the R Data and T Data straps on the Control Card are set for opposing polarities; one "normal" and the other "invert".
3. The next step disturbs the existing system as little as possible and is accomplished by unplugging the Teletype machine from the computer and plugging it into J267 at the rear of the Terminal Pedestal. Plug the terminal interface cable into the computer at the same connector where the teletype machine was plugged in. Put the Terminal in "LOCAL" and power up the computer, Terminal, and Teletype. Proper teletype operation in this configuration, checks out the relay cutover circuit and most of the interface cable connections.
4. Next, make sure the Teletype interface control card in the Terminal is strapped in accordance with the installation instructions given for the particular computer type being used. Strap the control card so that the Terminal will transmit and receive at 110 Baud. This is accomplished by placing the "BAUD SHIFT" strap to the "ON" position and adjusting R50, the "VARIABLE BAUD RATE" potentiometer for $880 \mathrm{~Hz}(1.14 \mathrm{~ms})$ at TP 1. If 880 Hz cannot be reached with R50, a small amount of extra capacitance may have to be temporarily added in parallel with C50, a $.001 \mu \mathrm{~F}$ capacitor adjacent to R50. Place the Terminal "ON LINE", power up the system, and if all is normal, the Terminal should be in 110 Baud communication with the computer. So far no modifications have been made to the computer and either the Terminal or the teletype machine may be exercised with either being selected by the "LINE/LOCAL" rocker switch on the Terminal. This step checks out the terminal level changers, serial registers, decoding, and basic terminal operation.
5. The installation mods can now be installed on the computer I/O card with everything still set as in step 4 above. After the mods are installed (listed in Section 1), the system should still be operable at 110 Baud but will have flagging for erase interval, page full, hard copy busy, etc. If step 5 does not work, the problem must be in the mods just installed. If everything is satisfactory, go on to step 6.
6. Enable high speed operation. This is accomplished by placing the "BAUD SHIFT" strap to "IN" and adjusting R50 for approximately 20 kHz at TP1. The Terminal should now run as in step 5 , but at a much greater speed.

This should enable you to solve any installation problem as it occurs rather than trying to sort it out after having completed the entire installation procedure.


## SECTION 5 PARTS LISTS ELECTRICAL PARTS LIST

Replacement parts should be ordered from the Tektronix Field Office or Representative in your area. Changes to Tektronix products give you the benefit of improved circuits and components. Please include the instrument type number and serial number with each order for parts or service.

## ABBREVIATIONS AND REFERENCE DESIGNATORS

| A | Assembly, separable or | FL | Filter | PTM | paper or plastic, tubular |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AT | Attenuator, fixed or variable |  | Heat dissipating device (heat sink, etc.) | R | Resistor, fixed or variable |
| B | Motor | HR | Heater | RT | Thermistor |
| BT | Battery | J | Connector, stationary portion | S | Switch |
| C | Capacitor, fixed or variable | K | Relay | T | Transformer |
| Cer | Ceramic | L | Inductor, fixed or variable | TP | Test point |
| CR | Diode, signal or rectifier | LR | Inductor/resistor combination | U | Assembly, inseparable or |
| CRT | cathode-ray tube | M | Meter |  | non-repairable |
| DL | Delay line | Q | Transistor or silicon- | $V$ | Electron tube |
| DS | Indicating device (lamp) |  | controlled rectifier | Var | Variable |
| Elect. | Electrolytic | P | Connector, movable portion | VR | Voltage regulator (zener diode, |
| EMC | electrolytic, metal cased | PMC | Paper, metal cased |  | etc.) |
| EMT | electrolytic, metal tubular | PT | paper, fubular | WW | wire-wound |
| F | Fuse |  |  | $Y$ | Crystal |

TTY PORT INTERFACE-CONTROL CARD

| Ckt. No. | Tektronix Part No. | Serial/Model No. Eff Disc |  |  | Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ASSEMBLIES |  |  |  |  |  |
|  | 670-1981-01 |  | 7248 |  | TTY CONTROL Circuit Card Assembly (common to 4010 TTY) |
|  | 670-1981-02 | 7249 | 7307 |  | TTY CONTROL Circuit Card Assembly (common to 4010 TTY) |
|  | 670-1981-03 | 7308 |  |  | TTY CONTROL Circuit Card Assembly (common to 4010 TTY) |
| CAPACITORS |  |  |  |  |  |
| C9 | 281-0524-00 |  |  |  | 150 pF , Cer, $500 \mathrm{~V}, 20 \%$ |
| C30 | 283-0003-00 |  |  |  | $0.01 \mathrm{uF}, \mathrm{Cer}, 150 \mathrm{~V},+80 \%-20 \%$ |
| C33 | 283-0003-00 |  |  |  | $0.01 \mu \mathrm{~F}$, Cer, $150 \mathrm{~V},+80 \%-20 \%$ |
| C41 | 285-0598-00 |  |  |  | $0.01 \mu \mathrm{~F}, \mathrm{PTM}, 100 \mathrm{~V}, 5 \%$ |
| C48 | 283-0001-00 |  |  |  | $0.005 \mu \mathrm{~F}, \mathrm{Cer}, 500 \mathrm{~V},+100 \%-0 \%$ |
| C50 | 285-0862-00 |  |  |  | $0.001 \mu \mathrm{~F}, \mathrm{PTM}, 100 \mathrm{~V}, 10 \%$ |
| C61 | 283-0003-00 |  |  |  | $0.01 \mu \mathrm{~F}$, Cer, $150 \mathrm{~V},+80 \%-20 \%$ |
| C63 | 290-0512-00 |  |  |  | $22 \mu \mathrm{~F}$, Elect., $15 \mathrm{~V}, 20 \%$ |
| C89 | 283-0000-00 |  |  |  | $0.001 \mu \mathrm{~F}$, Cer, $500 \mathrm{~V},+100 \%-20 \%$ |
| C100 | - 283-0177-00 |  |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C101 | 283-0177-00 |  |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C102 | 283-0177-00 |  |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C103 | 283-0177-00 |  |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C105 | 283-0177-00 |  |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C106 | 283-0177-00 |  |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C107 | 283-0177-00 |  |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C108 | 283-0177-00 |  |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C109 | 283-0177-00 |  |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |


| Ckt. No. | Tektronix <br> Part No. | Serial/ Eff | Model | No. Disc | Description |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DIODES |  |  |  |  |  |  |
| CR5 | 152-0185-00 |  |  |  | Silicon, selected from 1N4152 or 1N3605 |  |
| CR14 | 152-0185-00 |  |  |  | Silicon, selected from 1 N 4152 or 1N3605 |  |
| CR22 | 152-0185-00 |  |  |  | Silicon, selected from 1N4152 or 1N3605 |  |
| CR23 | 152-0185-00 |  |  |  | Silicon, selected from 1 N4152 or 1 N 3605 |  |
| CR28 | 152-0185-00 |  |  |  | Silicon, selected from 1 N4152 or 1N3605 |  |
| CR43 | 152-0185-00 |  |  |  | Silicon, selected from 1N5152 or 1N3605 |  |
| CR67 | 152-0185-00 |  |  |  | Silicon, selected from 1 N 4152 or 1N3605 |  |
| CR68 | 152-0185-00 |  |  |  | Silicon, selected from 1N4152 or 1N3605 |  |
| CR69 | 152-0185-00 |  |  |  | Silicon, selected from 1 N 4152 or 1N3605 |  |
| CR81 | 152-0185-00 |  |  |  | Silicon, selected from 1 N 4152 or 1N3605 |  |
| CR82 | 152-0185-00 |  |  |  | Silicon, selected from 1 N4152 or 1 N3605 |  |
| CR87 | 152-0185-00 |  |  |  | Silicon, selected from 1 N 4152 or 1N3605 |  |
| TRANSISTORS |  |  |  |  |  |  |
| Q1 | 151-0302-00 |  |  |  | Silicon, NPN, replaceable by 2N2222A |  |
| Q3 | 151-0302-00 |  |  |  | Silicon, NPN, replaceable by 2N2222A |  |
| Q7 | 151-0302-00 |  |  |  | Silicon, NPN, replaceable by 2N2222A |  |
| Q9 | 151-0302-00 |  |  |  | Silicon, NPN, replaceable by 2N2222A | 1 |
| Q13 | 151-0302-00 |  |  |  | Silicon, NPN, replaceable by 2N2222A |  |
| Q15 | 151-0188-00 |  |  |  | Silicon, PNP, replaceable by 2 N 3906 |  |
| Q21 | 151-0188-00 |  |  |  | Silicon, PNP, replaceable by 2 N 3906 |  |
| Q23 | 151-0504-00 |  | 7248 |  | Silicon, unijunction, replaceable by 2N4851 |  |
| Q23 | 151-0513-00 | 7249 |  |  | Silicon, unijunction, replaceable by 2N4853 | - |
| Q27 | 151-0513-00 |  |  |  | Silicon, unijunction, replaceable by 2 N4853 |  |
| Q29 | 151-1025-00 |  | 7307 |  | Şilicon, FET, N channel, replaceable by 2N5245 or selected from TIS88 |  |
| Q29 | 151-0302-00 | 7308 |  |  | Silicon, NPN, replaceable by 2 N 2222 A | $\checkmark$ |
| Q33 | 151-1025-00 |  |  |  | Silicon, FET, N channel, replaceable by 2 N 4245 or selected from TIS88 |  |
| Q35 | 151-0188-00 |  |  |  | Silicon, PNP, replaceable by 2 N3906 |  |
| Q55 | 151-0188-00 |  |  |  | Silicon, PNP, replaceable by 2 N3906 | $\checkmark$ |
| RESISTORS |  |  |  |  |  |  |
| R3 | 315-0472-00 |  |  |  | $4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |  |
| R4 | 315-0472-00 |  |  |  | $4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ | L |
| R5 | 315-0104-00 |  |  |  | $100 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |  |
| R7 | 315-0472-00 |  |  |  | $4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |  |
| R10 | 311-1286-00 <br> 311-1287-00 |  | 7248 |  | $50 \mathrm{k} \Omega, \mathrm{Var}$ $100 \mathrm{k} \Omega, \mathrm{Var}$ | $L$ |
| R11 | $311-1287-00$ $315-0302-00$ | 7249 |  |  | $100 \mathrm{k} \Omega, \mathrm{Var}$ $3 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ | - |
| R12 | 315-0102-00 |  |  |  | $1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |  |
| R14 | 315-0472-00 |  |  |  | $4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ | - |
| R15 | 301-0750-00 |  |  |  | $75 \Omega, 1 / 2 \mathrm{~W}, 5 \%$ |  |
| R17 | 301-0221-00 |  |  |  | $220 \Omega, 1 / 2 \mathrm{~W}, 5 \%$ |  |
| R21 | 315-0472-00 |  |  |  | $4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |  |
| R22 | 315-0472-00 |  |  |  | $4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ | $\square$ |
| R23 | 315-0203-00 |  |  |  | $20 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |  |
| R25 | 315-0472-00 |  |  |  | $4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |  |
| R27 | 315-0102-00 |  |  |  | $1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ | - |
| R28 | 315-0472-00 |  |  |  | $4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |  |
| R30 | 315-0472-00 |  |  |  | $4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |  |
| R33 | 315-0472-00 |  |  |  | $4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ $80.6 \mathrm{k}, 1 / 8 \mathrm{~W}, 1 \%$ |  |
| R44 R41 | $\begin{aligned} & 321-0376-00 \\ & 321-0336-00 \end{aligned}$ | 7249 | 7248 |  | $80.6 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ $30.9 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ |  |
| R43 | 315-0471-00 |  |  |  | 470 , $, 1 / 4 \mathrm{~W}, 5 \%$ |  |
| R45 | 315-0101-00 |  |  |  | $100 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |  |

Tektronix Serial/Model No.
Ckt. No.
Part No. Eff
Disc

## Description

RESISTORS (cont)

| R46 | $315-0102-00$ |
| :--- | ---: |
| R48 | $315-0472-00$ |
| R50 | $311-1396-00$ |
| R51 | $315-0243-00$ |
| R53 | $315-0242-00$ |
| R55 | $315-0101-00$ |
| R56 | $315-0102-00$ |

R58
R63
R67
R68
R71
R73
72-00
315-0183-00
315-0511-00
315-0302-00
315-0102-00
315-0220-00
R80
315-0751-00
R81
315-0472-00
R82
R84
R86
315-0203-00
315-0222-00
315-0472-00
315-0563-00
R99
315-0472-00

INTEGRATED CIRCUITS

| U1 | $156-0145-00$ |
| :--- | :--- |
| U7 | $156-0072-00$ |
| U9 | $156-0032-00$ |
| U17 | $156-0039-00$ |
| U19 | $156-0057-00$ |
| U21 | $156-0075-00$ |
| U23 | $156-0039-00$ |
| U25 | $156-0032-00$ |
| U27 | $156-0032-00$ |
| U29 | $156-0030-00$ |
| U31 | $156-0043-00$ |
| U33 | $156-0058-00$ |
| U35 | $156-0150-00$ |

$1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$2 \mathrm{M} \Omega, \mathrm{Var}$
$24 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$2.4 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$100 \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$18 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$510 \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$3 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$22 \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$750 \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$20 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$2.2 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$56 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$
$4.7 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$

Quad 2-input positive nand buffer, replaceable by SN7438N
Single monostable multivibrator-one shot, replaceable by SN74121N
Single $10 \mathrm{MHz} 1-\&-3$-bit binary ripple counter, replaceable by SN7493N
Dual 15 MHz J-K master-slave flip-flop, replaceable by SN7473N
Quad 2-input positive nand gate, replaceable by SN7401N

Single 8-bit data selector/multiplexer, replaceable by SN74151N
Dual 15 MHz J-K master-slave flip-flop, replaceable by SN7473N
Single 10 MHz 1- $\alpha$-3-bit binary ripple counter, replaceable by SN7493N
Single 10 MHz l- $\alpha-3$-bit binary ripple counter, replaceable by SN7493N
Quad 2-input positive nand gate, replaceable by SN7400N
Quad 2-input positive nor gate, replaceable by SN7402N
Hex. inverter, replaceable by SN7404N
Quad 2-input positive nand buffer, replaceable by SN7473N

| Ckt. No. | Tektronix Part No. | Serial/Model No. Eff Disc | Description |
| :---: | :---: | :---: | :---: |
| INTEGRATED CIRCUITS (cont) |  |  |  |
| U37 | 156-0043-00 |  | Quad 2-input positive nor gate, replaceable by SN7402N |
| U39 | 156-0058-00 |  | Hex. inverter, replaceable by SN7404N |
| U40 | 156-0047-00 |  | Triple 3-input positive nand gate, replaceable by SN7410N |
| U41 | 156-0041-00 |  | Dual 15 MHz D-type positive-edge-trigger flip-flop, replaceable by SN7474N |
| U43 | 156-0041-00 |  | Dual 15 MHz D-type positive-edge-trigger flip-flop, replaceable by SN7474N |
| U45 | 156-0041-00 |  | Dual 15 MHz D-type positive-edge-trigger flip-flop, replaceable by SN7474N |
| U47 | 156-0041-00 |  | Dual 15 MHz D-type positive-edge-trigger flip-flop, replaceable by SN7474N |
| U49 | 156-0041-00 |  | Dual 15 MHz D-type positive-edge-trigger flip-flop, replaceable by SN7474N |
| U51 | 156-0041-00 |  | Dual 15 MHz D-type positive-edge-trigger flip-flop, replaceable by SN7474N |
| U53 | 156-0041-00 |  | Dual 15 MHz D-type positive-edge-trigger flip-flop, replaceable by SN7474N |
| U55 | 156-0036-00 |  | Dual 4 -input positive nand buffer, replaceable by SN7440N |
| U57 | 156-0047-00 |  | Triple 3-input positive nand gate, replaceable by SN7410N |
| U59 | 156-0041-00 |  | Dual 15 MHz D-type positive-edge-trigger,flip-flop, replaceable by SN7474N |
| U60 | 156-0034-00 |  | Dual 4 -input positive nand gate, replaceable by SN7420N |
| U61 | 156-0039-00 |  | Dual 15 MHz J-K master-slave flip-flop, replaceable by SN7473N |
| U63 | 156-0030-00 |  | Quad 2-input positive nand gate, replaceable by SN7400N |
| U65 | 156-0047-00 |  | Triple 3-input positive nand gate, replaceable by SN7410N |
| U67 | 156-0145-00 |  | Quad 2-input positive nand buffer, replaceable by SN7438N |
| U69 | 156-0040-00 |  | Dual 2-bit-bistable latch, replaceable by SN7475N |
| U71 | 156-0120-00 |  | Single 4-bit right/left shift register, replaceable by SN7495N |
| U73 | 156-0120-00 |  | Single 4-bit right/left shift register, replaceable by SN7495N |
| U75 | 156-0058-00 |  | Hex. inverter, replaceable by SN7404N |
| U77 | 156-0035-00 |  | Single 8 -input positive nand gate, replaceable by SN7430N |
| U79 | 156-0039-00 |  | Dual 15 MHz J-K master-slave flip-flop, replaceable by SN7473N |
| U80 | 156-0030-00 |  | Quad 2-input positive nand gate, replaceable by SN7400N |
| U81 | 156-0145-00 |  | Quad 2-input positive nand buffer, replaceable by SN7438N |


| Ckt. No. | Tektronix Part No. | Serial/Model  <br> Eff No. <br> Disc  | Description |
| :---: | :---: | :---: | :---: |
| INTEGRATED CIRCUITS (cont) |  |  |  |
| U83 | 156-0174-00 |  | Dual 2- MHz J-K master-slave flip-flop, replaceable by SN74111N |
| U85 | 156-0129-00 |  | Quad 2-input positive and gate, replaceable by SN7408N |
| U87 | 156-0145-00 |  | Quad 2-input positive nand buffer, replaceable by SN7438N |
| U89 | 156-0040-00 |  | Dual 2-bit bistable latch, replaceable by SN7475N |
| U91 | 156-0120-00 |  | Single 4-bit right/left shift register, replaceable by SN7495N |
| U93 | 156-0088-00 |  | Single 8-bit parity generator/checker, replaceable by SN74180N |
| U95 | 156-0043-00 |  | Quad 2-input positive nor gate, replaceable by SN7402N |
| U97 | 156-0145-00 |  | Quad 2-input positive nand buffer, replaceable by SN7438N |
| U99 | 156-0030-00 |  | Quad 2-input positive nand gate, replaceable by SN7400N |

## MECHANICALPARTSLIST

TTY PORT INTERFACE-CONTROL CARD





[^0]:    $1_{\text {Refer to }}$ Electrical Parts List for part number.

[^1]:    ${ }^{2}$ The oscillator must be physically changed to double its frequency; then the INTERFACE CLOCK strap is used only in its X8 position. (C41 changes from. $01 \mu \mathrm{~F}$ to $.0068 \mu \mathrm{~F}$ and R 10 is readjusted to the higher frequency. Observe at TP2 on the Control Card.)

