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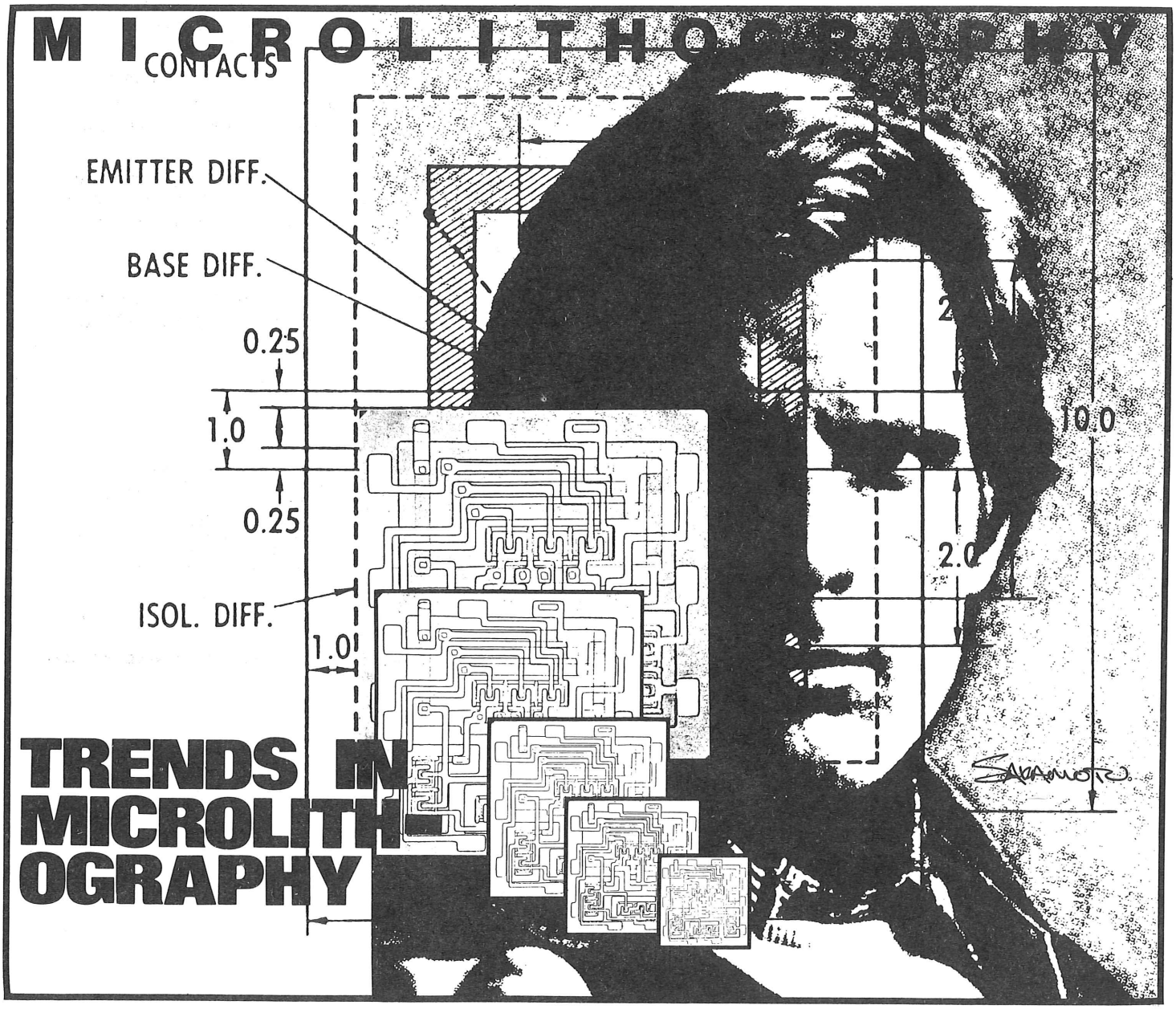


# Trends in Microlithography

*A microlithography primer appears on pages 4 and 5.*

Future trends in component fabrication will be influenced more by marketing directives and economic factors than by what is technically most feasible. This is particularly true for corporations that serve many highly specialized markets.

## Options

Microlithography, which includes the art of mask making as well as wafer fabrication, is an important process in the manufacture of complex semiconductors. Current lithographic processes are illustrated in Figure 1. The table summarizes their advantages and disadvantages.

Although it is likely that the use of electron-beam (E-beam) techniques for mask generation will become fairly routine by 1980, it is not the only option. One may, in certain situations, choose to bypass mask generation entirely and go to E-beam writing directly on wafers. In fact, Texas Instruments has already chosen this course for fabrication of high-density chips as part of their commitment to develop hand-held computers that will sell for $100 or less by 1985.

For those situations in which optical gratings, bubble memories, microwave, surface acoustic wave (SAW), and VLSI (very large scale integration) MOS devices are the major fabrication objectives, then E-beam or X-ray techniques may be indicated, since they promise the best resolution and the highest yield. For the photoprocessing of ROMS, PROMS, CCD, and other MOS (LSI) devices, perhaps an entirely different lithographic method, such as 1:1 projection printing, would be more appropriate. For a bipolar LSI process, which requires generally smaller geometries, one may choose a reduction-step-and-repeat exposure system. And finally, for discrete devices, the use of conventional contact printing could prove to be the most cost effective, as yield and volume problems are less severe than for integrated circuits.

## Trends

The number of components fabricated per chip has doubled each year since the early 60's. Advances in microlithography are a key element, together with circuit innovation, in maintaining this rate of progress. This rate of growth should continue for at least another five years. This means that average die size will gradually increase to about 500 mils square by 1985, and linewidths will approach the submicron range by 1985.

Figure 2 depicts continued growth in component densities and the time-growth intervals at which each new lithographic technology will be required for routine production support.

Because of the trend in instruments toward greater portability and reliability, and more functions, there will be an increased need for customized components, higher density memories, and new component technologies (for example, using GaAs MESFET). These and other needs will require advanced microlithographic techniques.

For information on how these trends may impact Tektronix, call Sal Emmi on extension 5713 or Mel Wright on extension 5308.

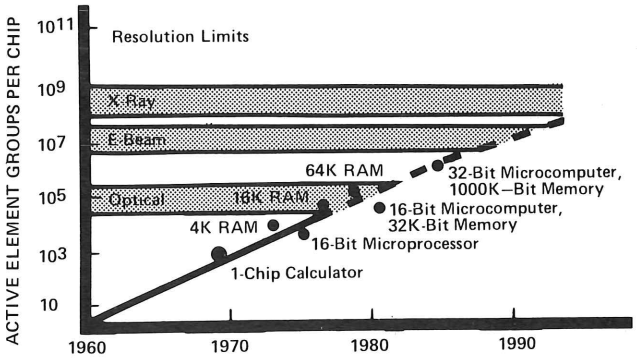
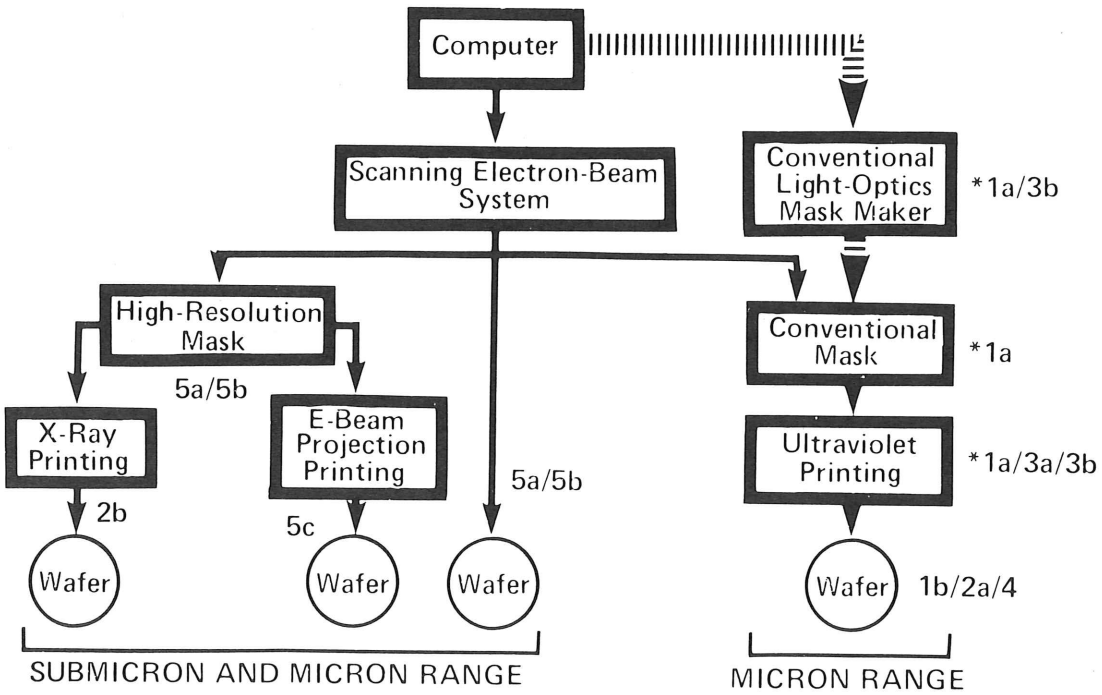



**Figure 2. Chip-density trends.**

The cover dramatizes the trend in microlithography toward greater density of active circuit elements in monolithic circuits. Showing the trend toward diminishing size is a series of integrated circuit dies. In the background is a diagram of the geometry of monolithic integrated circuit transistors.

# Alternative Lithographic Techniques

| Technique | Advantages | Disadvantages |
|---|---|---|
| 1. Contact Printing | | |
| a. Conventional | high throughput | marginally suitable for LSI |
| b. Flexible Mask | better resolution | low throughput |
| 2. Near-Contact Printing | | |
| a. Ultraviolet | low mask wear, high throughput | limited resolution |
| b. X-ray | high resolution, insensitive to defects | not commercially available |
| 3. Optical Projection | | |
| a. Full wafer | improved yields, high throughput | limited resolution |
| b. Step & Repeat | improved yields, improved resolution | lower throughput |
| 4. Reflective Optics | | |
| a. Full wafer | improved yields | limited resolution, long exposure times |
| 5. Electron Beam | | |
| a. Raster Scan (Spot) | high resolution, high yields | low throughput, cost |
| b. Vector Scan (Spot) | high resolution, high yields | low throughput, cost |
| c. Projection | high resolution, high yields, high throughput | cost |




*** Present Tektronix Process**

**Figure 1. Lithographic alternatives.**

# Disc Cleaning Service Offered

On August 1, Industrial Systems Support began a program of inspection of front (2315) and top (5440) disc packs. This cleaning will not cause any loss of data or damage to the disc. It will be performed in your area at a time depending on the usage and environment in which your equipment operates.

This service will reduce damage to discs and to the drives. Cost for this service will be approximately $3 per pack, depending on the number of packs that can be cleaned in a set-up.

For more information, please call Howard Duffy at extension 7091.

# In Print

## PROGRAMMABLE CLOCK SOURCE

Barrie Gilbert (Integrated Circuit Design) wrote an article for the June 7, 1977 issue of **Electronic Design**. The article, "Digitally Programmable Clock Source Built with a D/A and V/F converter," appears on page 118.

At the time he wrote the article, Barrie worked with Analog Devices, Inc. in Massachusetts. For a copy, call the library on ext. 5388.

# Microlithography Primer

Microlithography is the technology of writing microscopic circuit patterns on substrates. It is one of a sequence of techniques in the manufacture of integrated circuits. The series of drawings on the next page provides an overview of that manufacturing sequence.

The EPI (epitaxial) layer grown on the wafer may have a few atoms of an impurity mixed with the silicon to change the electrical characteristics of the layer. This layer is grown by passing the proper mixture of gases at high temperature over the surface.

Next, a thin layer of silicon oxide ($SiO_2$) is laid down over the EPI to prevent impurities from later layers from diffusing through the epi to the wafer.

In the microlithographic stage, "windows" are printed (using either an electron-beam, x-ray, or ultraviolet printing technique) on the surface of the $SiO_2$ layer leaving an image of the circuit pattern. The pattern is then etched down to the EPI layer.

In the diffusion stage, high-temperature gases carrying the dopants (impurities) are passed over and through the windows etched through the oxide. The dopants diffuse through the EPI and then a new protective oxide layer is grown over the wafer. The procedure in steps 2, 3, and 4 may be repeated several times depending on the circuit and process design.

The last layer deposited on the wafer is a very thin film of metal. The metal is etched to form conductors and bonding pads. Finally, the circuit is attached to the circuit package and wires are bonded to the pads for connection to the outside world.

1. EPI

Grow Silicon Layer (EPI) On Wafer

2. Oxidation

Grow Thin Layer Of $SiO_2$ Over Silicon For Protection

3. Microlithography

Etch Circuit Pattern In Oxide

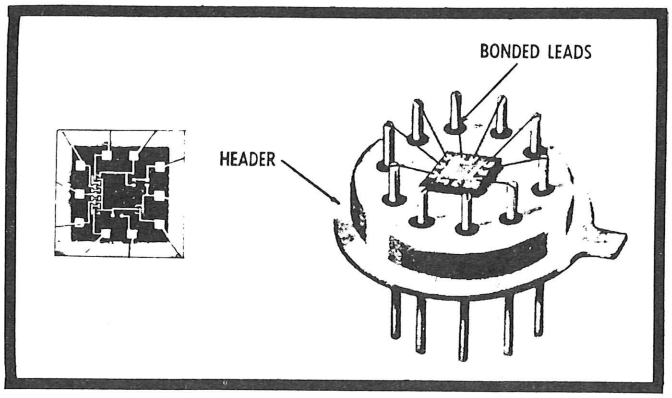
4. Diffusion

Diffuse Dopants Through Windows In Oxide

5. Metal

Contact

Coat Entire Wafer Area With A Thin Metal Layer, Etch Conductors And Bonding Pads. Mount Circuit In Package And Bond The Lead Wires.




**The circuit mounted with connecting leads in place.**

# A GPIB Analyzer

An IEEE 488 (General Purpose Interface Bus, or GPIB) designer can now easily and quickly study GPIB communications with a 7D01 logic analyzer and a modified DF1 display formatter. Interface-dependent and device-dependent messages handshaked across the GPIB can be displayed in a familiar mnemonic format on any 7000 series CRT. In this bus analyzer, a standard 7D01 Logic Analyzer acquires blocks of 256 bus "transactions" and a modified DF-1 Display Formatter displays the data in GPIB format. The bus analyzer can operate in either of two modes.

## DISASSEMBLED DATA

In one mode, the bus analyzer synchronously acquires information using the GPIB data valid (DAV) line as a clock. As many as 256 instructions are stored in the 7D01 and then disassembled and displayed on the DF-1 in IEEE 488 message mnemonics familiar to the GPIB user.

The 7D01 uses 12 of the available 16 lines to monitor ATN, EOI, SRQ, REN, and the 8 data lines. The 8 data lines come in on channels 0-7 with the clock line going to DAV. On the other probe, channel 12 goes to REN, 13 to SRQ, 14 to EOI, and 15 to ATN. Channels 8-11 make up 4 user-definable probes.

## More Information?

Bruce Ableidinger wrote the GPIB disassembler code and Jeff Bradford, who wrote the original DF1 code, helped interface it to the DF1.

If you would like more information on the operation and capabilities of the bus analyzer, call Bruce Ableidinger on ext. 6995 or drop by 39-135.

Contact Dave Lowry (ext. 6758, 39/092) for instructions and materials used to modify the DF-1.

In this mode, the 7D01 has to be in EXTERNAL SAMPLE INTERVAL with the EXTERNAL CLOCK POLARITY set for a high-to-low transition. The internal jumper FULL DISPLAY/FIRST TRIGGER (P617) must be set to FIRST TRIGGER.

## TIMING

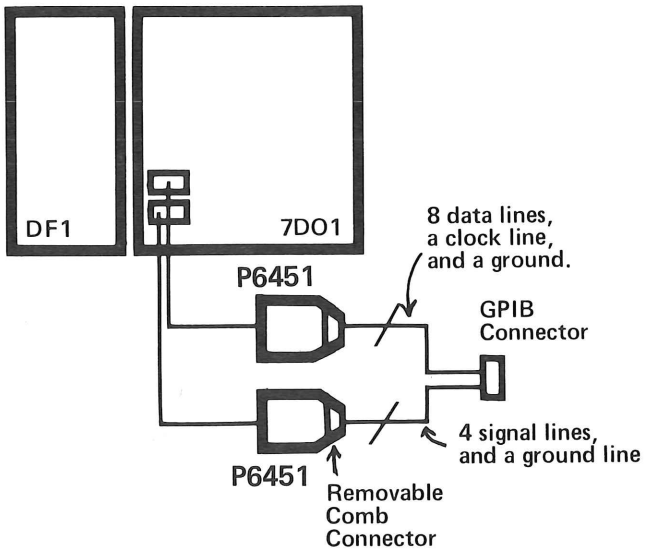
In the second mode, the user assigns 3 of the 4 remaining lines to the three-wire handshake, and then uses the internal clock (at an appropriate sampling rate) to study the timing relation of the three lines.

For example, the designer could set up the word recognizer to trigger the 7D01 on any one of the ATN messages and then study the handshake lines for that message in the timing mode.

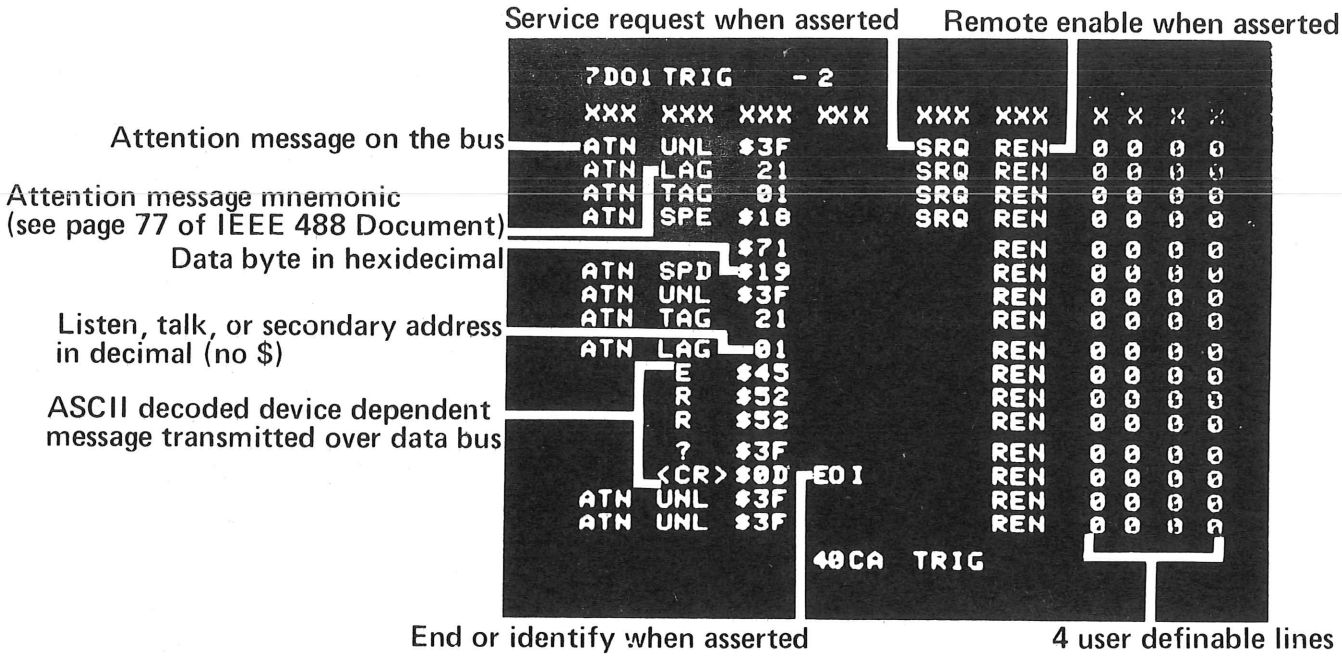
## ADAPTING THE 7D01 AND THE DF-1

The 7D01 needs no modification to work with the DF-1 in GPIB mode because the 7D01 acts only as a synchronous data acquisition unit. The internal DF-1 changes consist of an add-on EC board, several cables and one 2708 EPROM coded to disassemble the GPIB data. The front panel changes are: adding one push button (GPIB option), a backlighting LED, a drive transistor, and a hole punched in the panel.

A comb connector plugs cables from the GPIB connector into the two P6451 probes that plug into the front panel of the 7D01.




**A comb connector plugs cables from the GPIB connector into the two P6451 probes that plug into the front panel of the 7D01.**




**The DF-1 displays disassembled instructions in IEEE 488 message mnemonics familiar to the GPIB user.**

# Cyber Scientific Community Meeting

## FIRST MEETING HELD

The Cyber Scientific Community (CSC) recently held its first meeting. The participants discussed organization and goal setting, and commented on the proposed Tektronix internal user library and other topics of interest to the group.

## LIBRARY

Programs for the library will come primarily from CSC members and other Tektronix programmers. Programs from outside Tek may be included in the library if this proves beneficial. The applications group of the Scientific Computer Center will have primary management responsibility for the library.

## SEMINARS

Many CSC members requested seminars on selected topics. These will be presented in the near future, probably through Education and Training. Announcements of time and place will be made in **Engineering News** and **Tekweek.**

## THE CSC

The CSC's charter is to provide mutual aid through the exchange of ideas and software. Besides the program library, the group will also maintain a documentation library to make sure that all users have easy access to all the software available at Tektronix. Additional activities will be held to meet the needs of the CSC and Tektronix programmers.

Managers who wish representation in the CSC should designate a representative and forward the name to the coordinator of the CSC, Kurt Krueger, Applications Group Leader, at the Scientific Computer Center. Kurt can be reached at delivery station 50-454 or on ext. 5976.

# BJT Parameters

**CAUTION**

*Blind-faith usage of the transistor library is not encouraged.*

That might very well be a cautionary label for the Cyber system transistor library. Like all tools, the library has its own capabilities and limitations. To best use the transistor library, the design engineer should know the limitations of the parameters defined for the library.

A brochure, **BJT Parameter Measurement Techniques**, has recently been published by the Scientific Computer Center to provide the background information for those parameters. Topics discussed include:

- choosing a "typical" device.
- junction capacitances.
- early voltage.
- $I_C$ and $I_B$ versus $V_{BE}$ data measurement.
- dc parameters, $R_B$ and $R_E$.
- collector resistance — $R_C$.
- forward transit time.

For a copy of the brochure, contact Cyber Operations (ext. 5104).

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Maureen Key If you have
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