TEKTRONIX®

P7001

CHECKOUT SOFTWARE

062-1566-31 (Paper Tape)
062-1566-38 (Cassette)

INSTRUCTION MANUAL

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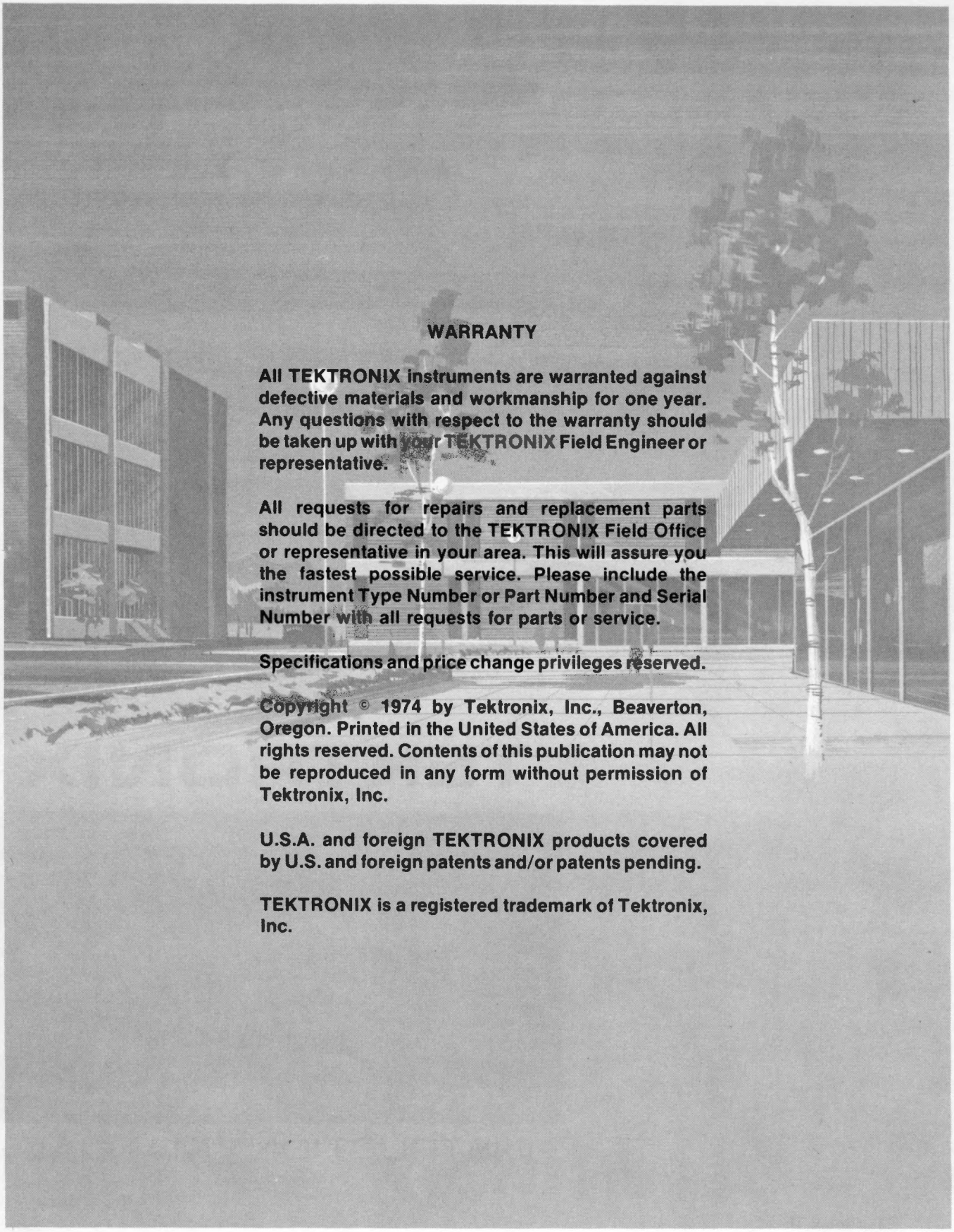
INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97005

070-1612-00



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INTRODUCTION

This manual describes the loading and operation of the P7001 Checkout Software. The software instructs the PDP-11 Controller (minicomputer) to perform various tests and exercises of the P7001 memory, circuitry and interfaces. The software itself is controlled by you, the Digital Processing Oscilloscope (DPO) operator. You request a test, supply parameters if needed (the software will request needed information) and the software does the rest.

In short:

You instruct the software.

The software instructs the controller.

The controller carries out the instructions.

You communicate with the software in a conversational mode via the computer terminal (either an ASR33 Teletype[1], or TEKTRONIX 4010). It works like this:

You ask for a certain test to be made by typing the mnemonic of that test on the terminal.

The controller responds by printing the test name in full and the mnemonic, and asks for any parameters (if needed).

You enter the information requested.

The test is performed.

If errors are found during the test, they will be printed on the terminal with information regarding addresses and data values. Interpretation of error messages is covered in detail in Section II of this manual.

Because of the complexity of the instrument, this software package is not meant to be a complete diagnostic test. It is, however, designed to checkout the basic operating circuits of the DPO and alert you to possible malfunctions associated with the P7001 Processor and its linkage (interface) with the PDP-11 Controller. If a test fails, the errors listed by this software do not necessarily point to the specific problem.

For example, if the Zero Display Generator Test (ZDG) finds a word in the processor's memory that has not been initialized to zero, the fault may not be actually at that word of memory, but could lie in the decoding of the Display Generator Status Word or even a problem in the controller itself. The error merely points to the end result of the malfunction.

[1]**Teletype is a registered trademark of the Teletype Corp.**

To benefit the most from this diagnostic software, note any errors encountered and continue on with the rest of the tests. When completed, go back to each test in error and repeat, looking for a reappearance of the same error. If it cannot be found, and no others are present, it is an indication that the problem was transient and may have been caused by interference in the transmitting of data between the P7001 and the PDP-11.

If the error persists, look for any similarity between it and others found (i.e., a particular word or block of words in memory). This information will aid the technician in troubleshooting the problem.

LOADING THE SOFTWARE

Before any test can be performed, the Checkout Software must be loaded into the controller's memory. The software comes on a roll of paper tape or cassette cartridge. If you have a paper tape system, skip the next paragraph and go to the one entitled Paper Tape Loading.

Cassette Loading. Insert the cartridge containing the Absolute Loader and Checkout Software into the left hand drive of the TA-11 tape drive. Toggle address 173ØØ into the ADDRESS/DATA switches of the controller, place the ENABLE/HALT switch in the HALT position, press START again. The cassette will rewind and then load the controller's memory with Checkout Software. The software is self-starting, and will respond with a listing of tests and options when loading is complete.

Paper Tape Loading. It is assumed here that the Bootstrap and Absolute Loaders are already in the controller's memory. If not, refer to Appendix B; Loading Bootstrap and Absolute Loaders.

The tape reader may be either a Tektronix 4911 Reader/Perforator, or other high-speed paper tape reader, or the paper tape reader on a Teletype terminal. In all cases, position the blank leader (the beginning portion of the tape with only the sprocket holes punched) over the reader sprockets. If you have a 4911, turn the power switch on and set the perforator and reader buttons to off. In the case of a Teletype, set the control lever to START, be sure the punch is off, and turn the LINE/LOCAL control to LINE.

To tell the controller that the Checkout Software tape is ready to be loaded, you must load the proper starting address (a location in the controller's memory) of the Absolute Loader into the controller. (The Absolute Loader is the software that reads in the tape.) The address of the Absolute Loader is $xx75ØØ_8$, where xx designates the highest available memory bank in your particular controller. The value for xx may be found in Table B-2 in Appendix B.

Loading an address into the PDP-11 controller is accomplished with the following switch operations on the controller front panel:

1. Set the ENABLE/HALT switch in the HALT position.

2. Place all ADDRESS/DATA switches down to the "Ø" position.

3. Press START.

4. Enter $xx75ØØ_8$ into the ADDRESS/DATA switches and press LOAD ADRS. This tells the controller where to start execution. (If you are not sure how to set the ADDRESS/DATA switches properly, refer to Appendix B.)

5. Set the ENABLE/HALT switch to the ENABLE position.

The controller is now ready to read in the Checkout Software tape. Is it in the reader? If so, press START on the PDP-11 controller panel and the tape should start moving through the reader. At the end of the tape, the reader will halt and the question "TYPE THE STATUS REGISTER ADDRESS OF THE DPO UNDER TEST", will be printed on the terminal. This signals a successful loading of the software.

ERRORS IN LOADING

If the tape does not move through the reader when START is pressed, check for the following conditions:

1. Was the proper address (xx75ØØ) loaded into the controller?

2. Is the ENABLE/HALT switch in the ENABLE position?

3. Is the reader turned on?

4. If using a Teletype terminal, is the LINE/LOCAL control in the LINE position?

To be sure the controller is in a state ready to accept the software tape, repeat the steps for loading the starting address. If nothing appears wrong, the Absolute Loader or the Bootstrap Loader may have to be reloaded. Refer to Appendix B for loading instruction.

RESTARTING THE SOFTWARE

As mentioned, once the Checkout Software is correctly loaded, it immediately starts execution and asks you for the status register address of the DPO you're testing. At times, you might find it desirable to get back to this initial state, or to the Monitor. (The function of Monitor is covered later.)

Since you already know how to load an address (or you wouldn't be at this point yet), getting to one of the two restarting addresses is easy.

Loading address $ØØØØØØ_8$ gets you to where you would be if you completely reloaded the software tape.

Loading address $ØØ12ØØ_8$ puts you back in the Monitor mode.

Monitor can also be accessed at any time during execution of the Checkout Software by entering a "Control P" command from the terminal. (Control commands are described shortly.)

WHAT YOU NEED (EQUIPMENT)

For the Checkout Software to operate properly, you need something for it to checkout. Besides the tape reader, PDP-11 controller and terminal already discussed, you need a DPO, properly connected. A working DPO consists of at least the following equipment:

1. A P7001 Processor with at least 1K of memory.

2. A D7704 Display Unit (one that functions properly without a P7001 Processor installed).

3. An A7704 Acquisition Unit.
4. Any 7000-Series Amplifier Unit.
5. Any 7000-Series Time Base Unit.

See Fig. 1-1 for orientation to these units.

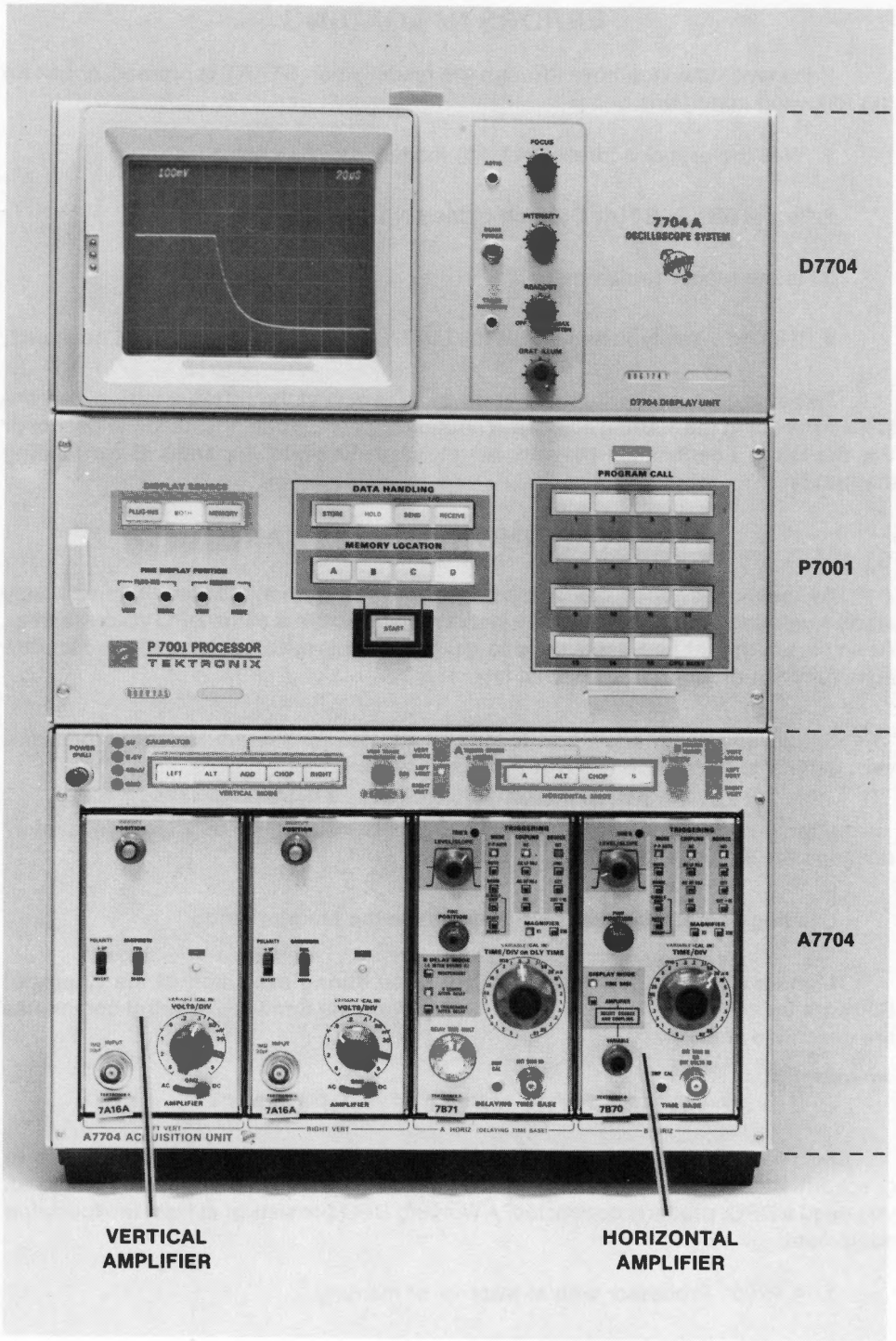


Fig. 1-1. DPO orientation.

Some initial control settings on the DPO must also be set to insure proper operation of the Checkout Software. These settings are:

1. DPO power on.

2. Display Unit READOUT switch turned on with enough intensity to allow you to easily read the display.

3. P7001 DATA HANDLING mode selected to HOLD.

One other switch, the Readout Mode switch located inside the A7704 Acquisition Unit, may have to be set. This is labeled FR/GATED (S 68) and it can be found by removing the bottom right-hand side panel of the A7704. Set the FR/GATED switch (see Fig. 1-2) to the FR position.

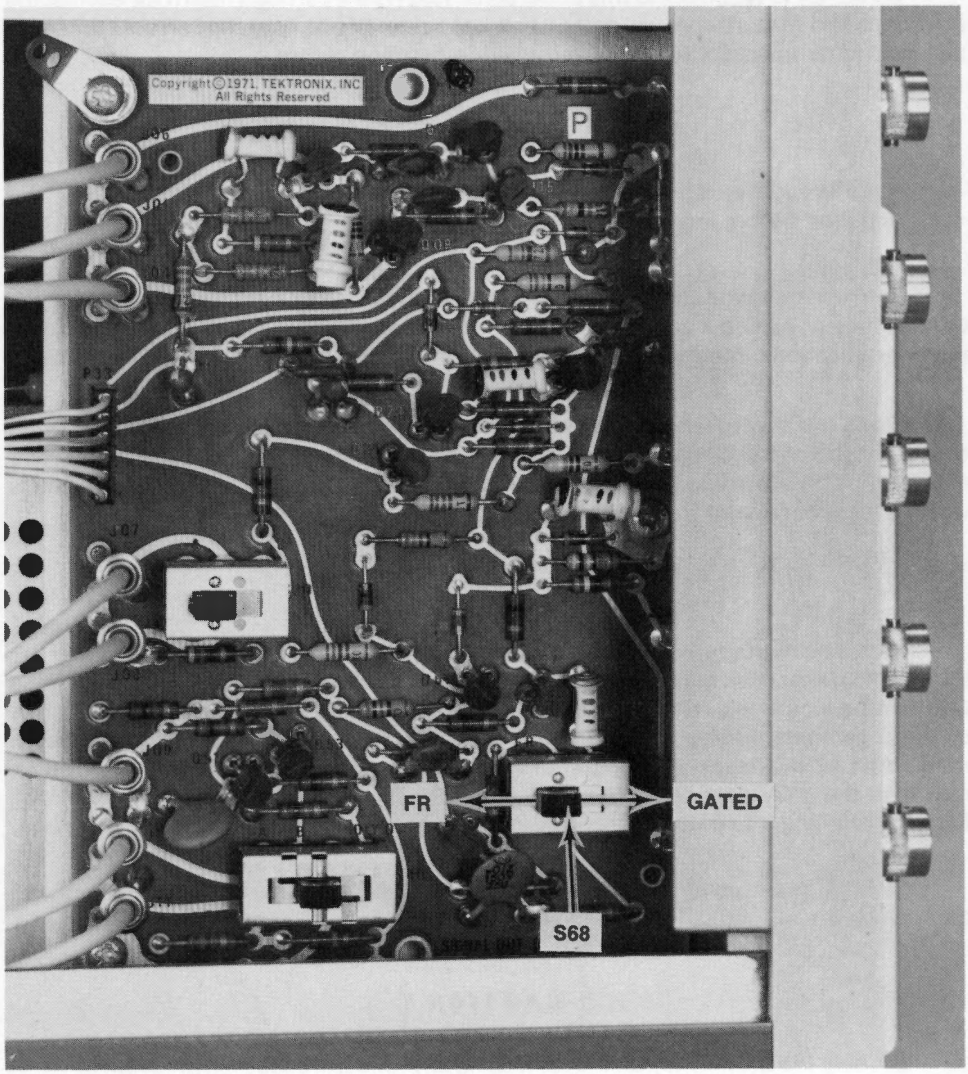


Fig. 1-2. Location of S68.

RUNNING THE CHECKOUT SOFTWARE

With the software loaded and the equipment properly set up and adjusted, you are ready to begin testing the DPO.

Since many DPO's may be on-line at any time, the controller must know which unit to test. The first three questions asked by the controller are used to define a particular DPO. The questions ask for the status register address, the interrupt vector address and the device number of the particular instrument to be tested.

When the DPO is shipped from the factory, the addresses and device number are set as follows:

STATUS REGISTER ADDRESS..... 164ØØØ

INTERRUPT VECTOR ADDRESS..... 374

DEVICE NUMBER..... Ø

If your DPO is still set to this initial state, just type a carriage return for each of the questions and the software will default to these values. If not, type the correct addresses and device number. Follow each entry with a carriage return.

NOTE

If the wrong status register address is entered, software must be completely reloaded before any test can be made.

The next questions concern the processor's memory. Answer by typing a Y for yes or an N for no. Typing a carriage return is not necessary. If you should answer N to all memory questions, the sequence will repeat until the actual configuration is known.

Once the controller knows the size of your processor's memory, a listing of all available tests and options is printed on the terminal. When the listing is completed, two asterisks ("**") are printed. This signals that the software is in the Monitor mode and is waiting for a command from you.

MONITOR

A monitor-structured system is used to allow maximum flexibility in testing the P7001 Processor. You may select and run any or all tests available simply by giving the Monitor the mnemonic for the test desired. The Monitor reads only the three characters of the mnemonic. Follow this entry with a carriage return. Should you misspell the mnemonic for the desired test, Monitor will respond with the message "WHAT?", then return to the Monitor mode. Whenever the word "WHAT?" appears on the terminal, Monitor is telling you that the previous input was unrecognized and must be retyped.

Only alpha-numeric characters (i.e., A-Z, 0-7, octal) and special control commands are allowable input to the Checkout Software. (Spaces are *NOT* allowed.)

CAUTION

Striking the BREAK key on the terminal at any time will cause the program to stop. To restart in this event, you must load address ØØ1200$_8$ (see previous section RESTARTING THE SOFTWARE).

SWITCH OPTIONS

The software includes three options, called SWITCH OPTIONS, that permit you to alter the normal performance of particular tests. They are:

1. Error switch "/E"
   This Error switch suppresses all error messages that would normally appear on the terminal. If this switch is set during the call of test ALL (see description of tests), no error message will be printed for any test.

2. Scope Loop switch "/S"
   This switch will place the test being called in a continuous loop until you interrupt with a Control P command.

3. Repeat and Count Error switch "/R"
   With this option, the selected test will repeat, error messages will be omitted, and the total number of errors found will be printed on the terminal at the termination of each pass through the test.

Switch options may be set either in the Monitor mode or during the execution of a test.

For example, if the software is in the Monitor mode, and you wish to use the test ADR (Address Test) with listing of errors suppressed, you would type on the terminal ADR/E. Spaces are not allowed when inputting test commands. The entire command is followed by a carriage return, and would look like this:

EXAMPLE #1. (Underscored characters are operator typed.)

** ADR/E(CR)

The (CR) is a carriage return and is not visible on the terminal. The Monitor takes no action until you press carriage return. For the rest of this text, *assume that every command is followed by a carriage return.* The two asterisks are printed by the software, indicating it is waiting for a command.

If you had desired to place the test in a Scope Loop, the sequence of characters on the terminal would have looked like this:

EXAMPLE #2.

** ADR/S

In this example, the test ADR would be repeated again and again until interrupted by entering a Control P or Control X command.

Similarly, if you had chosen the Repeat and Count Error switch, the input would look like this:

EXAMPLE #3

** ADR/R

Upon identifying the carrier return, the software would put the Address Test in a loop and suppress all error messages except for an error count which is printed at the end of each pass.

Any combination of the three switch options may be entered following the mnemonic of the desired test.

CONTROL COMMANDS

To cancel a switch option or to enter an option after the test has started, special control commands are used. These are entered via the terminal in the following manner:

1. Press and hold the CTRL (Control) key.

2. While still holding down the Control key, strike the character that corresponds to the command you want.

For example, *to cancel any previously set switch option, hold down on the Control key and type the character "X".* If you had previously entered the Scope Loop option, the program would return to Monitor at the end of the test and "**" would be printed on the terminal.

Suppose you wished to enter a switch option after the test is in progress. You can do this by entering the control command for the desired test at any time before the test is completed.

The following control commands are legal inputs to the Checkout Software: ("c" indicates Control function.)

1. cE
   Sets the Error switch to omit printing of error messages.

2. cS
   Sets the Scope Loop switch to run a test in a continuous loop.

3. cR
   Sets the Repeat and Count Errors switch option. The test in progress will repeat, and the number of errors found will be output at the end of each pass.

4. cX
   Cancels any previously set switch options.

5. cP
   This is the Control P command that will immediately return the program to the monitor mode. The test in progress will be aborted.

Before proceeding with the actual tests, it would be wise to review the function of the control options and switches. Likewise, be sure you understand the operation and location of controls located on the P7001 Processor and the terminal you are using.

TEST COMMANDS

Test commands are calls to the monitor for starting a given test. The commands may be entered only while operating in the Monitor mode (signaled by "***") and only one test command may be issued at any one time. Tests are executed immediately after the carriage return following the test mnemonic.

DEVICE SELECT TEST (DST)

The purpose of the Device Select Test is to verify that the strappable options on the PDP-11 Interface Controller and DPO Interface Controller are set correctly, and that the DPO responds to only one device number. If multiple DPO's are on-line, only the DPO under test should be turned on.

DESCRIPTION:

You are requested to generate a DPO interrupt by pressing one of the Program Call buttons. If the DPO interrupts to any other vector than the one specified during initialization, the error message

DPO INTERRUPTED TO VECTOR x

is displayed, where x is the vector the DPO generated.

Next, a command is sent to the DPO using each device number (0 to 7) in turn. If the DPO replys to a device number other than that specified at software initialization, the error message

DPO DEVICE NUMBER y ANSWERS TO DEVICE NUMBER z

is displayed, where y is the device number specified by you at initialization and z is a device number to which the DPO responded.

If the DPO does not reply to the device number specified at software initialization, the error message

DPO DOES NOT RESPOND TO DEVICE NUMBER y

is displayed on the terminal. If both these errors are displayed, it is likely that the number you entered as the device number is wrong. Check to be sure the number you entered matches the actual strapped value. (See DPO Interface Service manual, Part No. 021-0116-00 for instructions.)

STATUS WORD TEST (STA)

DESCRIPTION:

The STATUS WORD TEST checks each of the status words in the P7001 for correct responses to signals sent out on the common bus. This test is automatic and no operator intervention is required.

ERRORS:

A time-out error will occur if an addressed device status word does not recognize or properly decode a signal sent to it or if the device does not exist in the DPO configuration. If no response is generated within 3.5 μs, the Z-axis card automatically acknowledges the request to free the bus, and sends the caller a signal to tell it the proper device did not answer or was non-existent.

The format of the error message is:

DPO TIMEOUT WHEN REFERENCING THE { FRONT PANEL / DISPLAY GENERATOR / A/D CONVERTER / READOUT } STATUS CARD

SWITCH OPTIONS:

/S will put the test in a Scope Loop.

/E will execute the test and omit any error listing.

/R will put the test in a loop and list only the number of errors found.

Z-AXIS TEST (ZAT)

DESCRIPTION:

The Z-Axis Test exercises the P7001 bus time-out logic, the sweep-complete logic, and the single-shot reset logic. The circuitry exercised by this test is on the P7001 Z-Axis card. Two checks are made in this test. They are:

BUS TIME OUT CHECK. When a P7001 circuit card, memory address, or any internal card status word is addressed to the P7001 and is not recognized (i.e., addressing a non-existent card), the Z-Axis circuitry will answer the addressing device after a given time delay to free the bus. (The bus is considered "Hung" if no device answers.) The Z-Axis circuitry sets the error bit in the front panel status word, then generates an interrupt to the controller.

The bus time-out logic is tested by trying to write into a non-existent address. The P7001 should generate an interrupt after setting the error bit in the Front Panel status word. The controller, after receiving the interrupt, examines the bus-error bit. If the bit is not set, the error message "FAILURE OF BUS TIME-OUT LOGIC" is printed on the terminal. If the bus error bit is set, the test continues immediately to the next step, which is:

SWEEP COMPLETE AND SINGLE-SHOT-RESET LOGIC CHECK. Detection of Sweep Complete is available to the controller by examining bit 2 of the Front Panel Status word. When the sweep is complete, bit 2 is equal to "Ø" (off). Writing a "1" into bit 2 of the Front Panel status word resets the sweep.

The following sequence occurs for the Sweep Complete and Single-Shot-Reset exercise test:

1. Instructions are printed at the terminal, telling you to set the horizontal plug-in to single sweep mode, line trigger, and a sweep rate of .1 millisecond per division. When set up is complete, type "Y".

2. After a 1 second delay (to allow time for the sweep to be completed), the Front Panel status word is examined to see if the sweep complete bit is zero. The error message "FAILURE OF SWEEP COMPLETE LOGIC" is printed if the sweep complete bit is not zero.

3. The single-shot-reset bit is set in the Front Panel status word and examined immediately (prior to next end of sweep) to see if this time the sweep-complete bit is not zero.[1]

   The error message "FAILURE OF SINGLE SHOT RESET" is printed on the terminal if the sweep-complete bit is equal to zero.

EXAMPLE #1.

```
** ZAT
Z AXIS TEST (ZAT)
Ø ERROR(S) OCCURRED FOR BUS TIME-OUT LOGIC
SET HORIZ P.I. FOR SINGLE SWEEP, LINE TRIGGER, & .1MS,
SET LEVEL/SLOPE TRIGGER ADJUST FOR TRIG'D LIGHT,
DONE? (Y=YES, N=NO)
Y
Ø ERROR(S) OCCURRED FOR Z AXIS TEST (ZAT)
```

SWITCH OPTIONS:

/E omits the listing of an error message.

/R If this switch is used when the program is called, only bus time-out logic will be tested, repeatedly. To place the rest of the test in the Repeat and Count Error loop, enter Control R while the test is running.

/S (See /R above.)

There are four tests available for checking out processor memory:

DATA TEST (DAT)

DESCRIPTION:

DATA TEST writes zeros in all bits of a specific P7001 memory address, reads the data and verifies if the data is correct, writes all ones in the same address and reads again to verify that the data is correct.

[1]If you have a Sampling Time Base, the Single-Shot-Reset cannot be tested. An error message will be generated in this case, and can be ignored.

INPUT:

The software will request a specific memory address to be typed on the terminal. Enter the desired address (in octal) and press return. This is the address that will be tested. This test will 1) determine if all data bits are stored correctly, and 2) determine if the I/O Interface decodes all bits correctly.

ERRORS:

In the event of an error, the correct data and the actual data received are output to the terminal for comparison. You may then evaluate the inclusion or exclusion of any bits that are in error. The address chosen (following the software printed instruction) allows selected address testing of the P7001 memory. Addresses are numbered in accordance with the address map description found in Appendix C.

If an error does occur, it is suggested that the test be run again using the Scope Loop switch option. If the error does not appear again after several minutes of testing, you can probably assume that the original error was due to interference and could be ignored. If the error repeats, either the memory location is faulty or an error has occurred in the transmission or decoding of the information.

If no error occurs, a test-completed message is printed and the software returns to Monitor mode.

The following examples show output for both a successfully completed test and what the software would display had an error been found.

EXAMPLE #1. (Underscored characters mean operator typed. You do it.)

```
** DAT
DATA TEST (DAT)
ENTER P7001 MEMORY ADDRESS TO BE TESTED
1200
Ø ERROR(S) OCCURRED FOR DATA TEST (DAT)
```

EXAMPLE #2.

```
** DAT
DATA TEST (DAT)
ENTER P7001 MEMORY ADDRESS TO BE TESTED
1000
ERROR(S) OCCURRED FOR DATA TEST
AT ADDRESS      DATA SHOULD BE      DATA READS
1000            1777                1776
1 ERROR(S) OCCURRED FOR DATA TEST (DAT)
**
```

SWITCH OPTIONS:

/S places the DATA TEST in a continuous loop.

/E omits printing of any error messages.

/R prints only the number of errors found and repeats test.

ADDRESS TEST (ADR)

The second memory test, ADDRESS TEST, is similar to the prevous DATA TEST but has the added capability of testing addresses throughout the entire range of the address map (see Appendix C). The test allows address testing of processor core memory and/or hardware device addresses.

DESCRIPTION:

The purpose of the ADDRESS TEST is to verify proper operation of the P7001 to address its core memory or the hardware device addresses. You may define the limits of the test to any part or all of the processor's range of addresses.

INPUT:

The software will request both the starting and ending addresses to be entered from the terminal. The range is Ø-17777_8. Specific device and memory location may be found on the address map in Appendix C.

You may evaluate any single address or range of addresses by defining the limits of the test. The address test is broken into two parts: CORE MEMORY ADDRESSES and DEVICE ADDRESSES.

CORE MEMORY ADDRESSES:

For Core Memory Addresses, the ADDRESS TEST writes each address as data into all locations of the memory range specified. After reaching the ending address, the memory locations are read to determine if the stored addresses are correct. (For example, address 127_8 should contain the data 00127_8). Core Memory address range is Ø-8888. Since words are 10 bits in length, the two most significant bits of the address are not written as data into the word.

DEVICE ADDRESSES:

Devices are defined as the Front Panel or other installed circuitry in the P7001. The device addresses are broken into blocks, or ranges, and each range is tested according to the function it performs. The ranges and their functions are:

RANGE 1ØØØØ—15577—NONEXISTENT DEVICE ADDRESSES. The ADDRESS TEST in this range checks to see that no device(s) answers to a non-existent device address. This portion of the address test relies on the Z-Axis circuitry to create a bus error and thus an interrupt when attempting to write into a non-existent area. (The bus is a communication link between data sending and receiving circuitry.) Should the controller not receive an interrupt when attempting to write into this range (1ØØØØ—15777), an error message will be sent to the terminal. This test is made for both writing and reading in this range.

Since this test depends on the Z-Axis circuitry, test ZAT should be made prior to this ADDRESS TEST.

RANGE 156ØØ—15777—FRONT PANEL ADDRESSES. The ADDRESS TEST in this range checks to see if the Front Panel status word answers to all Front Panel Device Addresses. The controller writes the number 156ØØ as data into all Front Panel addresses or up to the ending address chosen in the test initialization (the second address you inputted), whichever is less. After the specified ending address has been reached, the Front Panel addresses are read to determine if the data is correct.

RANGE 16ØØØ—16577—DISPLAY GENERATOR READOUT INTERFACE ANALOG TO DIGITAL CONVERTER. The ADDRESS TEST in this range checks to see if the Display Generator, Readout Interface, and Analog to Digital Converter status words cause the proper cards to answer to their associated Device Addresses. The controller writes the number 16ØØØ as data in every word of the range (within the limits of the input variables). After your specified ending address is reached, or the last address in this range is encountered, the controller attempts to read the status words and checks to see if the data is zero.

NOTE

1. The controller cannot read information from the Display Generator or the Readout Interface status words. Therefore, their data should be zero.

2. When the controller attempts to read the Analog-to-Digital Converter status word, the vertical data is sent to the controller. Therefore, the vertical signal must be adjusted to equal zero data. A message requesting vertical signal adjustment to zero signal will be printed on the terminal prior to the testing of this address range. (See Example #3.)

RANGE 166ØØ—16777—I/O INTERFACE. The ADDRESS TEST in this range functions the same as for non-existent Device Addresses. (See Range 1ØØØØ—15777 described at the beginning of the ADDRESS TEST description.)

RANGE 17ØØØ—17777—X-Y DISPLAY MODE X DATA. The ADDRESS TEST in this range checks for proper addressing of the X-Y Display Mode. The controller sets up the Display Generator in the X-Y mode, and then writes each address as data into all locations of the address range specified by your inputs.

NOTE

The MSB (most significant bit) is not written as X-data. This is done to lower the ramp display on the CRT so it is easy to see. After reaching the specified ending address, the controller then attempts to read data from the X-Y addresses. The controller cannot obtain data in this address range. If the data is not equal to zero when read, an error message will be printed.

The ADDRESS TEST may be performed on any range of addresses. Thus any waveform location, readout storage location, device address, or any desired range of addresses may be checked for proper addressing.

ERRORS:

If errors occur, they are brought to your attention in the format shown in Example #1. The error message contains the address in question, what data was expected, and what the controller actually read. Proper evaluation of this information may determine which address bits are incorrect. At the end of the test, the number of errors (if any) are displayed in octal. A study of the number of errors could help pin-point the location of any trouble close to a component in the core memory hardware.

EXAMPLE #1. (Underscored characters are operator input.)

```
** ADR
ENTER STARTING ADDRESS
Ø
ENTER ENDING ADDRESS
7777
ERROR(S) OCCURRED FOR ADDRESS TEST
 AT ADDRESS          DATA SHOULD BE          DATA READS
      2                     2                     4
      4                     4                     2
2 ERROR(S) OCCURRED FOR ADDRESS TEST (ADR)
**
```

EXAMPLE #2.

```
** ADR
ADDRESS TEST (ADR)
ENTER STARTING ADDRESS
1ØØ
ENTER ENDING ADDRESS
4ØØ
Ø ERROR(S) OCCURRED FOR ADDRESS TEST (ADR)
```

EXAMPLE #3.

```
** ADR
ADDRESS TEST (ADR)
ENTER STARTING ADDRESS
Ø
ENTER ENDING ADDRESS
17777
POSITION VERTICAL DC LEVEL 1 DIV BELOW BOTTOM SCREEN
GRATICULE LINE THEN HIT SPACE BAR
Ø ERROR(S) OCCURRED FOR ADDRESS TEST (ADR)
**
```

WORST CASE TEST (WCT)

DESCRIPTION:

In the WORST CASE TEST, the controller generates a worst case bit pattern in all P7001 memory locations, then verifies if memory is functioning correctly by reading the patterns back. The Worst Case bit pattern is generated by writing alternate Ø's and 1's in sequential physical locations of the processor's memory core mat. This is considered the worst case pattern and is used to determine how an individual memory core affects its physically adjacent core locations.

ERRORS:

Errors encountered in this test are not listed in a numerical address sequence, but in a physical sequence from one end of memory to the other. The address at which each error occurred, the value of what the data should be, and the value of what the data actually reads are printed on the terminal.

EXAMPLE #1. (Underscored characters are operator typed.)

```
** WCT
WORST CASE TEST (WCT)
ERROR(S) OCCURRED FOR WORST CASE TEST (WCT)
 AT ADDRESS          DATA SHOULD BE          DATA READS
      Ø                    Ø                    1776
     2Ø                  1777                   1ØØØ
2 ERROR(S) OCCURRED FOR WORST CASE TEST
**
```

EXAMPLE #2.

```
** WCT
WORST CASE TEST (WCT)
Ø ERROR(S) OCCURRED FOR WORST CASE TEST (WCT)
```

SWITCH OPTIONS:

/S places the WORST CASE TEST in a continuous loop. This allows checking of signals on the memory cards containing IC's and transistors. Do not attempt to check signals on the memory mat card by attaching probes, because core damage may result.

/E omits the listing of an error message.

/R suppresses error listing, places WCT in a continuous loop and prints number of errors found after each pass through the test.

MEMORY PATTERN TEST (MPT)

DESCRIPTION:

This test is valid only if semi-conductor memory is installed in the P7001. It is similar to the WORST CASE TEST in that bit patterns are written into memory and then re-read to determine accuracy.

The controller first sets every word of memory to zero, then sets one bit "on" in each word. Memory is then examined to see if the bit was indeed set. It then zeros memory and sets the second bit of each word "on" and tests as before. This process is repeated for all ten bits of each word.

The second part of the test sets all bits "on" in each word and then zeros one bit of each word and checks for the proper value. Then, all bits are turned on again and another bit of each word is turned "off". The cycle continues until all ten bits have been tested.

This test assumes 4K of memory. With less than 4K of memory, the MEMORY PATTERN TEST will "wraparound" the memory, checking some locations as many as four times. For example, if you have 1K of memory, and an error is found at location 200_8, the following output might appear on the terminal.

AT ADDRESS	DATA SHOULD BE	DATA READS
200	40	2040
2200	40	2040
4200	40	2040
6200	40	2040

Location 200_8 is the actual address in error, but because the test made four passes through memory, the same error was found four times. The address was incremented by 2000_8 (1K decimal) with each pass.

If 2K memory is used, the error would be found twice. With 3K the error would be found once or twice, depending on whether the word in question is located in high or low memory.

SWITCH OPTIONS:

/S places the Memory Pattern Test in a continuous loop.

/E will suppress the listing of any errors found.

/R will put the test in a loop and output the number of errors found after each pass.

ZERO DISPLAY GENERATOR TEST (ZDG)

DESCRIPTION:

When a STORE/START command is given, the Display Generator initializes all of the chosen core memory waveform locations to zero. (For example, if you pressed STORE, A, START on the processor's front panel, the Display Generator would zero out memory locations $0\text{-}0777_8$ in the processor, as these locations correspond to the storage area for waveform A.) This test checks to see if the Display Generator really does zero out all of the stated memory locations by sending a status word to "Store A, B, C, D". Memory is then examined for zeros in all memory locations. Errors which may be present are displayed on the terminal for each incorrect address.

EXAMPLE #1. (Underscored characters are operator typed.)

```
** ZDG
ZERO DISPLAY GEN TEST (ZDG)
ERROR(S) OCCURRED FOR ZERO DISPLAY GEN TEST (ZDG)
 AT ADDRESS          DATA SHOULD BE          DATA READS
      0                    0                    1777
     100                   0                     1
2 ERROR(S) OCCURRED FOR ZERO DISPLAY GEN TEST (ZDG)
**
```

EXAMPLE #2.

```
** ZDG
ZERO DISPLAY GEN TEST (ZDG)
Ø ERROR(S) OCCURRED FOR ZERO DISPLAY GEN TEST (ZDG)
**
```

SWITCH OPTIONS:

/E will suppress any error listing.

/S will place the test in a scope loop.

/R will repeat the test and print the number of errors found after each pass.

There are four sets of computer generated data points that can be used to check the Display Generator operation. Each data point set produces a distinct DPO CRT waveform; the X-Y Display Waveform, the Calibrate Waveform, X-Y Intensity and the Display Generator Accuracy Test.

X-Y DISPLAY WAVEFORM (XYD)

The purposes of the X-Y Display pattern are:

a. To check correct operation of the Display Generator in the X-Y mode.

b. To check the Display Generator horizontal compensation.

c. To check both the vertical and horizontal digital to analog conversion gain when using the X-Y mode.

The X-Y Display pattern (see Fig. 2-1) is generated by the controller in the following sequence:

a. The Display Generator is sent a status word placing it in the X-Y mode.

b. X-Y coordinate data is sent to the Display Generator directly from the computer.

c. The Display Generator draws vectors on the CRT between successive coordinates as they are received. The user may discontinue the X-Y display by striking the space bar. (The displayed data points are not stored in the processor's memory upon completion of the test.)

Horizontal compensation may be made to eliminate overshoot or undershoot. Overshooting may be detected at points A, B, and C of the X-Y display pattern (shown in Fig. 2-1). For adjustment procedures, see Display Generator Instruction Manual, Part No. 070-1608-00.

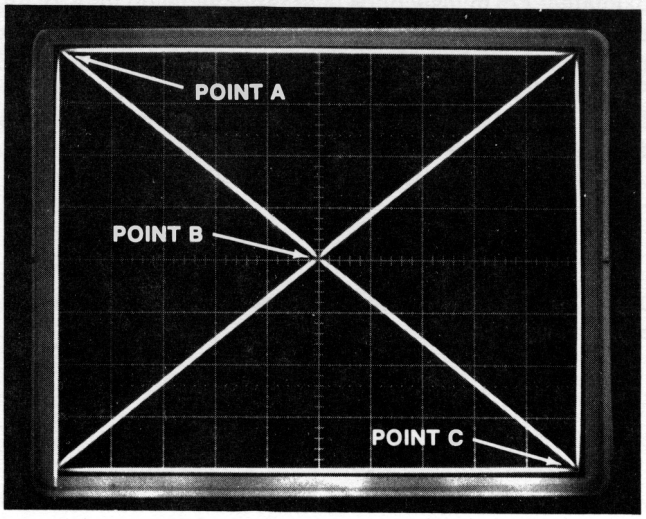


Fig. 2-1. X-Y Display pattern.

SWITCH OPTIONS:

There is no meaningful result from the use of any switch option with this test.

NOTE

This test is used in calibration procedures encompassing the entire system. Do not attempt to make calibration adjustments using only front panel controls. If calibration procedures are called for, be sure the DPO is properly warmed up (at least 20 minutes).

CALIBRATE WAVEFORM (CAL)

DESCRIPTION:

This second waveform display has four purposes:

a. Check for correct operation of the Display Generator in the Y-T mode. (Y-T displays amplitude (Y) against time (T).)

b. Check for correct zero logic operation of the Display Generator.

c. Check vertical compensation of the Display Generator.

d. Check the Display Generator vertical and horizontal gain and positions.

The CALIBRATE WAVEFORM display is generated in the Y-T mode in the following sequence:

a. The Display Generator is sent a status word to store zeros into memory location A.

b. Approximately 125 milliseconds later (after allowing time for the memory to be cleared), the controller stores the CALIBRATE WAVEFORM coordinates in memory location A. The first two divisions of the CALIBRATE WAVEFORM (see Fig. 2-2a) have successive address coordinates stored, causing segments 1 and 2 to be displayed at a bright intensity. The remianing segments have coordinates stored only for addresses which are proportional to approximately one centimeter increments, resulting in a dimmer display.

c. The Display Generator now pulls the waveform from Memory Location A and displays it on the CRT.

You may stop the display by striking the space bar. The waveform will be left in Memory Location A.

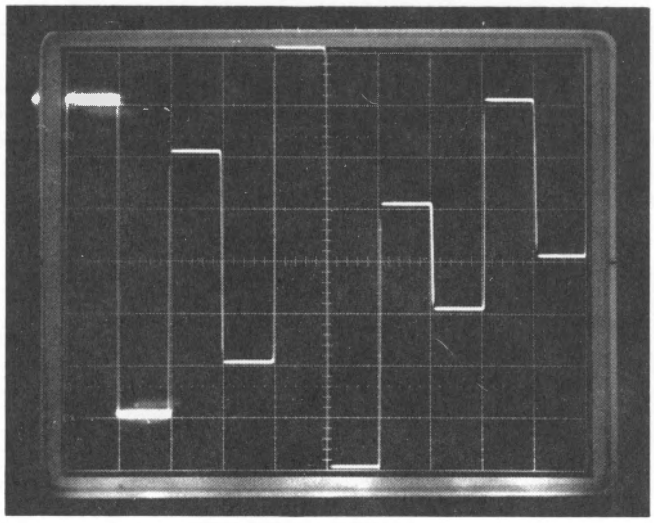
Segments 1 and 2 of the display should have a square transition at points A and B (see Fig. 2-2a). Any spikes, rounding, or ringing on the waveform can be corrected by adjustment of the vertical compensation potentiometer, located on the Display Generator circuit card. (See Display Generator Instruction Manual, Part No. 070-1608-00). If the compensation is incorrect, a damped ringing or rounding off effect appears because of the large number of points in segments 1 and 2, while there are only two points in all the other segments.

The Display Generator includes logic to ignore zeros in memory during the Y-T mode of operation. If a memory address has a value of zero (nothing stored in that address), the Display Generator does not draw a vector on the CRT for that address. If the Display Generator zero logic is not functioning properly, the CALIBRATE WAVEFORM will appear as in Fig. 2-2b.

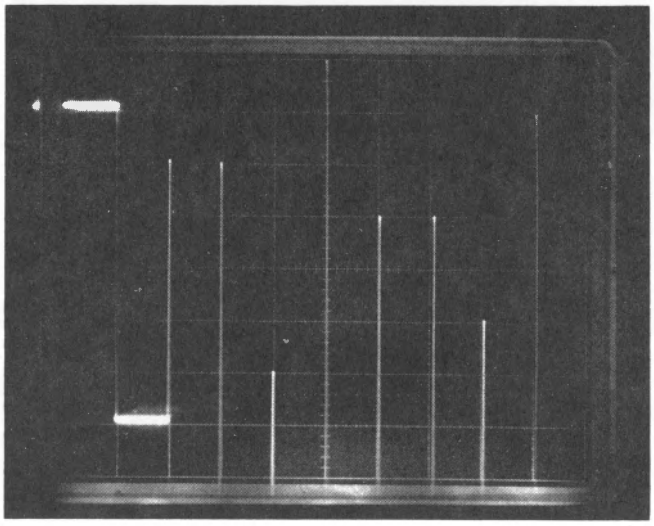
If the Display Generator is functioning properly, the horizontal and vertical components of the waveform will lie on graticule lines of the CRT. Gain and position adjustment controls located on the Display Generator card are used to correctly position the display.

SWITCH OPTION:

There is no meaningful result from the use of any switch option with this test.



A. Display Generator correctly working.



B. Display Generator improperly working.

Fig. 2-2. Calibrated waveforms.

X-Y INTENSITY TEST (XYI)

This routine tests the three intensity levels of the DPO CRT (dim, normal, and bright) in the X-Y mode. The software generates three chevrons (inverted "V's"), the outermost being of bright intensity, the middle normal, and the innermost dim. Figure 2-3 shows the correct display. It may be necessary to turn up the D7704 intensity control to see the innermost display. Hitting the space bar terminates the test.

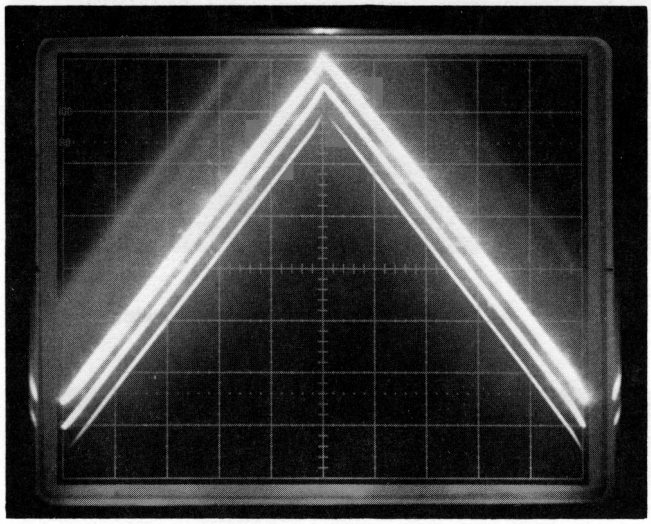


Fig. 2-3. X-Y Intensity Test waveform.

DISPLAY GENERATOR ACCURACY TEST WAVEFORM (DGA)

This test is performed in the Y-T mode. A horizontal pattern is displayed on the DPO CRT, with vertical vectors drawn every centimeter. If these vertical lines are absent, it is an indication of a possible bit error in the display generator. See Figure 2-4 for correct display. Striking the space bar will terminate this test.

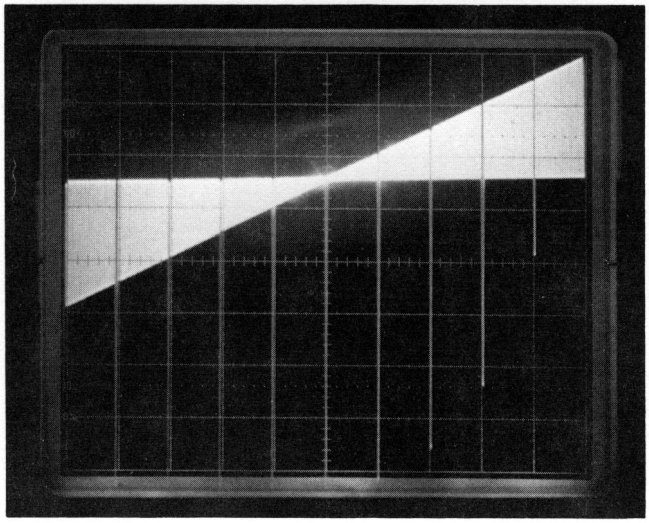


Fig. 2-4. Display Generator Accuracy Test waveform.

TRANSFER ROUTINE (XFR)

DESCRIPTION:

The TRANSFER ROUTINE checks proper transfer of data from one Memory Location (either A, B, C, or D) to any other memory location in the P7001.

EXAMPLE #1. (Underscored characters are operator typed.)

```
** XFR
TRANSFER OF MEMORY LOCATION DATA (XFR)
PRESS SEND, THE DESIRED MEMORY LOCATION, THEN START
(the routine waits here until START has been pressed on the DPO front panel)
PRESS RECEIVE, THE DESIRED MEMORY LOCATION, THEN START
(again, the routine waits until the operation has been performed)
TO EXIT FROM TEST HIT SPACE BAR
**
```

If, for example, the Calibration waveform created during the CAL test was still in Memory Location A, it could be sent to location B by first pressing SEND, A, and START on the DPO Front Panel when the message PRESS SEND, THE DESIRED MEMORY LOCATION, THEN START appears on the terminal. This action sends the data in A to the controller for temporary storage before the receive sequence starts. When completed, the next message, PRESS RECEIVE, THE DESIRED MEMORY LOCATION, THEN START will be printed on the terminal. By following the instructions, the contents of memory location A will be transferred to whichever memory location you specified. The original (sending) memory location will remain the same.

SWITCH OPTIONS:

/S will allow you to perform several store operations with either one or more waveforms.

ANALOG-TO-DIGITAL CONVERTER TEST (A2D)

The ANALOG TO DIGITAL CONVERTER TEST checks correct response of the A-D converter to changes at its input.

DESCRIPTION:

The A-D converter is that part of the P7001 that digitizes input waveforms from the plug-ins and stores them in the processor's memory. Vertical amplitude becomes data that is stored in a memory location corresponding to the horizontal divisions on the CRT. This test determines if the input signal is digitized correctly by comparing real-time input with known values.

INPUT:

Operator interaction is required to vertically position the trace to several dc levels. These levels will be digitized and compared with software generated data. A tolerance factor of ±2.5% (a total of 5% full scale) is automatically set by software if you do not request another value when calling up the test. You can select any tolerance from 0 to 9% by following the test command with a hyphen "-" and an integer (0 through 9).

EXAMPLE #1. (Underscored characters are operator typed.)

** A2D-5

The above example requests a ±5% level of tolerance in determining correctness of the A-D converter output. If the tolerance option is not chosen, the tolerance will default to ±2.5%.

The sequence of events of the A-D test is:

1. The P7001 is put into the STORE mode.

2. The software instructs you to position the trace on the bottom CRT graticule line and center it.

3. Information from memory is checked to be sure it is in tolerance with the nominal value for each trace dc level.

4. Repeated instructions are printed asking you to raise the level of the trace one horizontal division. You signal the controller that you have completed the operation by entering a "Y" on the terminal.

ERRORS:

Errors that are detected are printed on the terminal and consist of the address in the processor that is in question, what data should be there and what the controller actually reads. If the dc trace is placed in the wrong vertical position, errors will occur for every tested address.

EXAMPLE #1. (Underscored characters are operator typed.)

```
** A2D
ANALOG TO DIGITAL CONVERTER TEST (A2D)
INSTALL HORIZ PLUG IN(S): SET TRIG SOURCE(S) TO EXT; SET SWEEP
TO .1MS
INSTALL VERTICAL PLUG IN INTO VERT COMPARTMENT ONLY
SET VERT GAIN TO .5V/DIV
CENTER HORIZ SWEEP POSITION(S) TO EXTEND OUTSIDE THE
GRATICULE 1Ø DIV LIMITS
POSITION VERTICAL DC LEVEL TO BOTTOM SCREEN GRATICULE LINE
DONE? (Y=YES, N=NO) (NOTE: Controller waits here until you respond.)
Y
RAISE VERTICAL DC LEVEL +1 DIV DONE? (Y=YES, N=NO)
Y
RAISE VERTICAL DC LEVEL +1 DIV DONE? (Y=YES, N=NO)
.
.  (this sequence repeated 8 times)
.
RAISE VERTICAL DC LEVEL +1 DIV DONE? (Y=YES, N=NO)
Y
Ø ERROR(S) OCCURRED FOR ANALOG TO DIGITAL CONVERTER TEST
(A2D)
**
```

Had errors been detected during the test, they would be displayed in the following manner:

EXAMPLE #2.

```
ERROR(S) OCCURRED FOR ANALOG TO DIGITAL CONVERTER TEST
(A2D)
 AT ADDRESS          DATA SHOULD BE          DATA READS
      Ø                    146                    Ø
      1                    146                    Ø
2 ERROR(S) OCCURRED FOR ANALOG TO DIGITAL CONVERTER TEST
(A2D)
```

At least two plug-ins are needed to perform this test, a Time Base and an amplifier. These instruments should be installed in the far right and far left plug-in compartments of the A7704 Acquisition Unit respectively. With no input to either plug-in, center the dc trace signal so that the left and right edge are just outside the left and right boundary lines of the graticule. The vertical position of the trace must be exactly on the bottom graticule line. Be sure the Triggering Mode is in the Auto position.

SWITCH OPTIONS:

/E will omit the printing of any errors encountered.

/S will place this test in a continuous loop.

/R will place the test in a loop and output only the number of errors (if any) at the end of each pass.

Three Readout Interface exercise tests, "READOUT TEST", "SCALE FACTOR STORE TEST" and "READOUT 'ROM' TEST" are used to verify proper operation of the Readout Interface circuitry and to verify proper storage of scale factor data (usually obtained from the acquisition plug-in units or controller generated data).

READOUT TEST (ROT)

DESCRIPTION:

The READOUT TEST checks the Readout Interface in the DPO by displaying patterns and words on the CRT screen, and asking you to visually check the resultant display. The step-by-step procedure is described below:

Part A. This section checks time slot and column data (see 7704A Oscilloscope Service System Manual (Part No. 070-1260-00) for description of special terms used in association with Tektronix P7001 readout systems).

1. Message "0123456789" is written in Channel 0 in all fields and all waveform locations.

2. The command "HOLD A,B,C,D" sets the Readout Interface Card status word. (you see only waveform A.)

3. You respond with yes or no (Y=YES, N=NO) if the correct message is in the upper left of the DPO CRT.

   a. If YES—after typing Y, the software advances to Part B.
      If NO—after typing N, you are asked if there are any characters in the display.

b. If NO—after typing N, the message "READOUT NOT FUNCTIONING" will be printed.
If YES—after typing Y, you are asked if characters are in upper left of CRT (Channel 0 only).

c. If NO—after typing N, the message "CHANNEL ERROR(S) OCCURRED FOR READOUT TEST (ROT) INCOMPLETE" will be printed.
If YES—after typing Y, you are asked if the characters are all numbers.

d. If NO—after typing N, the message "ROW ERROR OCCURRED TEST INCOMPLETE" is printed on the terminal.
If YES—after typing Y, the message "TIMESLOT ERROR OR COLUMN ERROR OCCURRED TEST INCOMPLETE" is printed.

Part B. Check proper row data and channel addresses.

1. The following message is written in all fields and all waveform buffers of the P7001 memory:

Chan. 0	Chan. 1	Chan. 2	Chan. 3
Chan. 4	Chan. 5	Chan. 6	?JMP ERROR

   You see only waveform A.

NOTE

"?" is an instruction that the P7001 Readout Interface circuitry translates as a command to jump out of channel 7, and not to display the words "JMP ERROR" that are stored for readout use. If the jump instruction "?" did not get decoded by the Readout Interface Card, the DPO CRT will show the words "JMP ERROR" in the Channel 7 location.

2. The status word "HOLD A,B,C,D" is sent to the Readout Interface Card, and the CRT displays the following message out of the scale factor area associated with Memory Location A.

CHAN. 0	CHAN. 1	CHAN. 2	CHAN. 3
CHAN. 4	CHAN. 5	CHAN. 6	

3. You are asked if the message is correct.

   a. If YES—after typing Y, the software goes immediately to Part C.
   If NO—after typing N, you are asked if the words "JMP ERROR" appear.

   b. If YES—after typing Y, the message "ROW ERROR OCCURRED TEST INCOMPLETE" is printed on the terminal and the test halts.
   If NO—after typing N, the question "ARE CHANNEL #'S IN PROPER SEQUENCE? is printed on the terminal.

   c. If YES—after typing Y, the message "ROW ERROR OCCURRED TEST INCOMPLETE" is printed on the terminal.
   If NO—after typing N, the message "CHANNEL ERROR OCCURRED TEST INCOMPLETE" is printed on the terminal.

Part C. Checks the field and Memory Location scale factors.

1. Identifying messages are written in each readout Memory Location. The message: "FIELD x, WAVEFORM y" is filed in each field of each Memory Location, where x is the field number (Ø-3) and y is the Memory Location (A-D).

2. Status words are sent in sequence to the Readout Interface Card as follows:

   DISPLAY FIELD 0, WAVEFORM A
   DISPLAY FIELD 1, WAVEFORM A
   DISPLAY FIELD 2, WAVEFORM A
   DISPLAY FIELD 3, WAVEFORM A

3. You are asked if the proper message is displayed (for each message).
   If NO—after typing N, the message "FIELD ERROR OCCURRED" is printed on the terminal. The software then fetches the next message.
   If YES—after typing Y, the software continues to the next message until all messages have been displayed. When finished, the controller sets the Readout Status Word to accomplish:

   Display A,B,C,D (should see "FIELD 0 WAVEFORM A")
   Display B,C,D (should see "FIELD 0 WAVEFORM B")
   Display C,D (should see "FIELD 0 WAVEFORM C")
   Display D (should see "FIELD 0 WAVEFORM D")
   The P7001 always displays the memory location alphabetically nearest A.

4. You are asked if the proper message is displayed for each message.
   If NO—after typing N, the message "WAVEFORM ERROR" will be printed on the terminal. The software then goes to the next message.
   If YES—after typing Y, the software continues to the next message until the routine is complete.

EXAMPLE #1. (Underscored characters are operator typed.)

```
** ROT
READOUT TEST (ROT)
IS MESSAGE IN UPPER LEFT OF CRT "Ø123456789" (Y=YES, N=NO)
Y
ARE THE FOLLOWING MESSAGES DISPLAYED?
    CHAN. Ø     CHAN. 1     CHAN. 2     CHAN. 3
    CHAN. 4     CHAN. 5     CHAN. 6
(Y=YES, N=NO)
Y
DOES THE MESSAGE "FIELD Ø WAVEFORM A" APPEAR? (Y=YES, N=NO)
Y
DOES THE MESSAGE "FIELD 1 WAVEFORM A" APPEAR? (Y=YES, N=NO)
Y
DOES THE MESSAGE "FIELD 2 WAVEFORM A" APPEAR? (Y=YES, N=NO)
Y
DOES THE MESSAGE "FIELD 3 WAVEFORM A" APPEAR? (Y=YES, N=NO)
Y
DOES THE MESSAGE "FIELD Ø WAVEFORM A" APPEAR? (Y=YES, N=NO)
Y
DOES THE MESSAGE "FIELD Ø WAVEFORM B" APPEAR? (Y=YES, N=NO)
Y
```

```
DOES THE MESSAGE "FIELD Ø WAVEFORM C" APPEAR? (Y=YES, N=NO)
Y
DOES THE MESSAGE "FIELD Ø WAVEFORM D" APPEAR? (Y=YES, N=NO)
Y
READOUT TEST (ROT) COMPLETE
**
```

EXAMPLE #2.

```
** ROT
READOUT TEST (ROT)
IS MESSAGE IN UPPER LEFT OF CRT "Ø123456789" (Y=YES, N=NO)
Y
ARE THE FOLLOWING MESSAGES DISPLAYED?
     CHAN. Ø     CHAN. 1     CHAN. 2     CHAN. 3
     CHAN. 4     CHAN. 5     CHAN. 6
(Y=YES, N=NO)
N
DOES THE MESSAGE "JMP ERROR" APPEAR? (Y=YES, N=NO)
Y
ROW ERROR(S) OCCURRED FOR READOUT TEST (ROT)
TEST INCOMPLETE
**
```

SCALE FACTOR STORE TEST (SFS)

DESCRIPTION:

The Scale Factor Store Test routine makes various tests of the Readout Interface circuitry by storing particular Scale Factor patterns in Field 0 of the P7001 memory. This test must be made with all plug-ins removed from the Acquisition Unit. The following table is a summary of tests that are made.

TABLE 2-1

Test #	Put into Memory	Sent to R/O Interface	Check for A B C D	Error Code A B C D
1	All 8's	H A B C D	8 8 8 8	1 2 3 4
2	All 8's	S A B C D	* * * *	5 5 5 5
3	All 8's	S A	* 8 8 8	6 2 3 4
4	All 8's	S B	8 * 8 8	1 6 3 4
5	All 8's	S C	8 8 * 8	1 2 6 4
6	All 8's	S D	8 8 8 *	1 2 3 6
7	All 8's	S B D	8 * 8 *	1 6 3 6
8	All 8's	S A C	* 8 * 8	6 2 6 4
9	All 8's	S	8 8 8 8	1 2 3 4

NOTE: H—Hold
S—Store
A—Memory Location A
B—Memory Location B
C—Memory Location C
D—Memory Location D
**—Expect skips in Time Slots 1, 2 & 3 and expect spaces in Time Slots 4 through 10.*

Any errors are written on the terminal along with the correct data for each occurrence. The following table describes error codes:

Code #	Description
1	Illegal Store A.
2	Illegal Store B.
3	Illegal Store C.
4	Illegal Store D.
5	Wrong Data Stored.
6	Scale Factor stored at wrong time or the selected Scale Factor was not stored correctly.

The procedure for each test is as follows:

1. You are instructed to remove all plug-ins from the Acquisition Unit.

2. An ASCII 8 character is stored in all of Field Ø memory.

3. A status word for each test is sent to the Readout Interface (see Table 2-1 for the status word sent for each test).

4. A check for each test is made to ensure the correct operation was performed (see Table 2-1 for operation performed).

5. All tests are performed sequentially. The next step commences as soon as the first is done.

NOTE: "A" refers to the Acquisition Unit.

EXAMPLE #1.

```
** SFS
REMOVE ALL PLUG-INS FROM "A" UNIT FOR READOUT SCALE FACTOR
STORE TEST (SFS) THEN HIT SPACE BAR
ERROR(S) OCCURRED FOR READOUT SCALE FACTOR STORE TEST
(SFS)
SEE ERROR CODE 5
 AT ADDRESS          DATA SHOULD BE          DATA READS
    4Ø6Ø                   4Ø                     42
    4Ø62                   177                    2Ø
2 ERROR(S) OCCURRED FOR SCALE FACTOR STORE TEST (SFS)
**
```

SWITCH OPTIONS:

/S will place the SFS test in a continuous loop, printing error messages if they are found.

/E will suppress the listing of error messages.

/R will place the test in a loop and print a count of errors found at the termination of each pass.

READOUT "ROM" TEST (RRT)

The readout (Read Only Memory) test exercises the Readout Interface for all combinations of ASCII characters. Four messages are generated by this test (one in each scale factor area corresponding to Memory Location A, B, C, and D).

The message placed in Memory Location A scale factor area is all the characters that the Readout Interface Card can encode (all visual characters). Fig. 2-5 is a photo of the correct display.

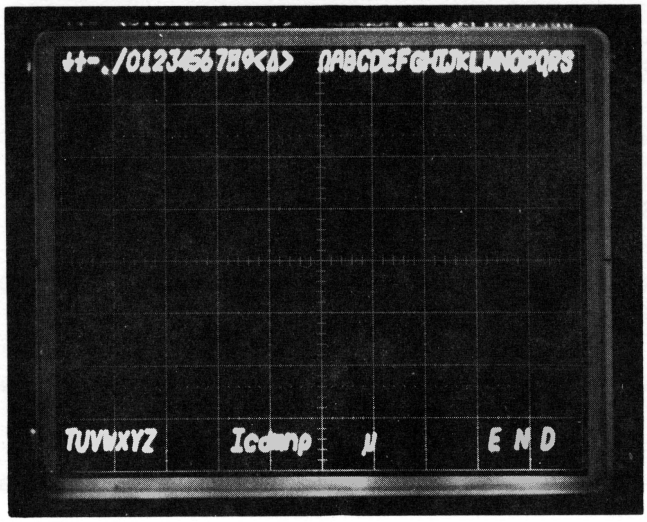


Fig. 2-5. Message in Memory Location A.

In Memory Location B, a message with the inclusion of a decimal point logic is displayed. In this test, the decimal point will always be positioned to the right one extra place for each word. The message in channel #7 of Memory Location B checks for the correct display of an ASCII decimal point in all ten Time Slot locations. See Fig. 2-6 for the proper message.

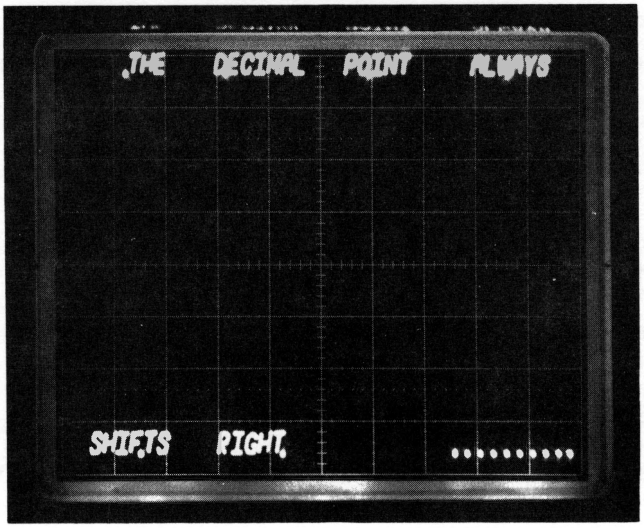


Fig. 2-6. Message in Memory Location B.

The message in Memory Location C scale factor area checks out the zeros logic of the readout system and the jump instruction. The message "CORRECT" should appear in five channel locations (Ø through 4). In channel #5, the message "JMP ERROR" is stored preceded by a "word jump instruction". If the word jump instruction is not executed, the message "JMP ERROR" will be displayed (see Fig. 2-7).

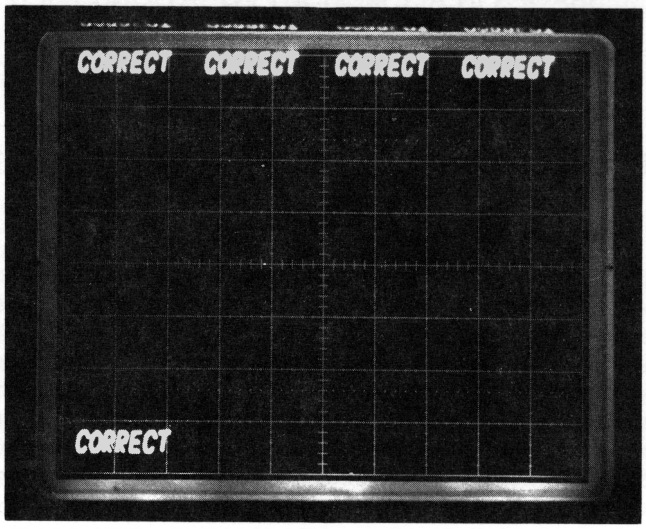


Fig. 2-7. Message in Memory Location C.

The message in Memory Location D scale factor checks out all legal skip instructions. The skip instructions are programmed throughout the message, such that if the skips are executed properly, the readable portion of the message will not be distorted. Fig. 2-8 shows the correct format.

These messages will exercise all possible combinations of the Readout Interface ROM chip. (A subset of the ASCII character set.)

The software will instruct you to observe each of the four memory locations to check for errors. Striking the space bar will terminate the test.

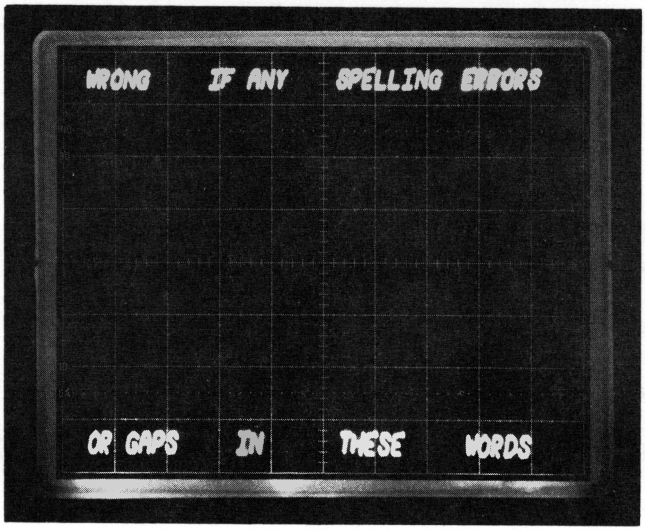


Fig. 2-8. Message in Memory Location D.

EXAMPLE #1. (Underscored characters are operator typed.)

```
** RRT
READOUT ROM TEST (RRT)
MESSAGE COMPLETE
CHECK ALL MESSAGES IN ALL MEMORY LOCATIONS THEN HIT SPACE
BAR
**
```

MULTIPLE MEMORY LOCATION STORE TEST (MMS)

DESCRIPTION:

The MULTIPLE MEMORY LOCATION STORE TEST checks the DPO for all proper combinations of multiple inputs and the correct storage into memory locations. A dc level is accepted from plug-in units in the DPO Acquisition Unit. A tolerance of ±5% (total 10% full scale) is accepted as correct. All combinations of legal input are made according to the type of plug-ins available. You respond to questions regarding the type of plug-ins in your particular system. Should you have two time bases, an instruction is printed to position the vertical trace separation so that the two sweeps are vertically coincident (on top of each other), and to center the horizontal position controls so the ends of both sweeps are outside the graticule 10 division limits.

In brief, this test checks for proper storage of all combinations of legal input signals while using the various mainframe horizontal and vertical modes of operation.

ERRORS:

If errors are found, the software will display the address at which the error was found, what the data should be and what the data really is.

SWITCH OPTIONS:

/S will place the test in a continous loop, printing error messages if they are found.

/E will suppress the listing of error messages.

/R will place the test in a loop and print a count of errors found at the termination of each pass.

EXAMPLE #1. (Underscored characters are operator typed.)

```
** MMS
MULTIPLE MEMORY LOCATION STORE TEST (MMS)
DO YOU HAVE SAMPLER PLUG-IN(S)? (Y=YES, N=NO)
N
DO YOU HAVE A DUAL VERTICAL PLUG-IN? (Y=YES, N=NO)
N
DO YOU HAVE TWO TIME BASE PLUG-INS? (Y=YES, N=NO)
N
INSTALL HORIZ PLUG-IN(S), SET TRIG SOURCE(S) TO EXT; SET SWEEP TO
.1 MS
INSTALL VERTICAL PLUG-IN INTO LEFT VERT COMPARTMENT ONLY
SET VERT GAIN TO .5 V/DIV
SET MAINFRAME HORIZ MODE TO B
```

```
SET MAINFRAME VERTICAL MODE TO CHOP
POSITION VERTICAL TRACE 1 CM ABOVE BOTTOM SCREEN LEVEL
DONE? (Y=YES, N=NO)
Y
Ø ERROR(S) OCCURRED FOR MULTIPLE MEMORY LOCATION STORE
TEST (MMS)
SET MAINFRAME VERTICAL MODE TO ALT
POSITION VERTICAL TRACE 1 CM ABOVE BOTTOM SCREEN LEVEL
DONE? (Y=YES, N=NO)
Y
Ø ERROR(S) OCCURRED FOR MULTIPLE MEMORY LOCATION STORE
TEST (MMS)
INSTALL VERTICAL PLUG-IN INTO RIGHT VERT COMPARTMENT ONLY
SET VERT GAIN TO .5 V/DIV
SET MAINFRAME HORIZ MODE TO B
SET MAINFRAME VERTICAL MODE TO CHOP
POSITION VERTICAL TRACE 1 CM ABOVE BOTTOM SCREEN LEVEL
DONE? (Y=YES, N=NO)
Y
Ø ERROR(S) OCCURRED FOR MULTIPLE MEMORY LOCATION STORE
TEST (MMS)
SET MAINFRAME VERTICAL MODE TO ALT
POSITION VERTICAL TRACE 1 CM ABOVE BOTTOM SCREEN LEVEL
DONE? (Y=YES, N=NO)
Y
Ø ERROR(S) OCCURRED FOR MULTIPLE MEMORY LOCATION STORE
TEST (MMS)
MULTIPLE MEMORY LOCATION STORE TEST (MMS) COMPLETE
```

WRITES MESSAGE FROM TERMINAL ONTO CRT (WRI)

DESCRIPTION.

This routine allows you to visually inspect the readout on the DPO CRT for proper input and display of text. Characters typed on the terminal will appear on the CRT.

The set of characters displayable on the CRT readout is a subset of the full ASCII code character set. The characters allowed are the digits 0-9, all upper case letters except O, the lower case letters c, d, m, p, u and the six symbols

/ . + − < >

There are three additional non-ASCII characters available for outputttting on the CRT. To enter these characters, refer to the table below:

ASCII Character	Readout Character
!	↓
=	Δ
@	Ω

Although lower case letters can be displayed by the Readout circuitry, only upper case letters and special characters may be input for this test.

After 40 characters have been entered, an automatic carriage return and line feed is forced on the terminal to match the CRT's space limits. Text entered past the 80 character limit of the scale factor area is inserted into memory, but it does not appear on the DPO CRT. The test is automatically terminated when the maximum input is reached (177_8) for the scale factor storage area.

Control P will terminate this test at any time.

ERRORS:

Errors, if present, may be found by either visually comparing your typed input with what is displayed on the CRT, or by running the PRINTS SCALE FACTOR MESSAGE ON TERMINAL test (PSF).

EXAMPLE #1. (Underscored characters are operator typed.)

```
** WRI
WRITES MESSAGES FROM TERMINAL ONTO CRT (WRI)
PRESS THE DESIRED MEMORY LOCATION
NOTE: CONTROL SHIFT P (NULL) TERMINATES THIS TEST
ENTER TEXT
TEKTRONIX HOPES THAT YOUR NEW DPO SYSTEM AIDS IN KEEPING
YOUR GEAR ON THE AIR . . .
THIS LAST LINE IS NOT PRINTED ON THE DPO CRT . . .
MESSAGE COMPLETE
**
```

PRINTS SCALE FACTOR MESSAGE ON TERMINAL (PSF)

DESCRIPTION:

This test prints the message from a P7001 Memory Location scale factor area onto the terminal. The software instructs you to press the desired Memory Location button, and information in that scale factor area is transferred to the terminal. After 40 characters have been output, the software forces an automatic carriage return and line feed enabling the printed output to align with the CRT display.

The entire 127 characters stored in the scale factor area are printed, 80 of which are visible on the CRT.

Certain codes may be in a scale factor location which will not appear on the CRT. Examples of special characters and a brief description of the function they perform in the Acquisition Unit Readout circuit are listed below.

ASCII Code in Scale Factor Location	CRT Readout	Comments
:	Non-printing	Will be found in first time slot for scale factor plug-in units.
;	Non-printing	May be found in first time slot for some digital plug-in units.
$ % & ' (	Decimal point commands (loc. 3, 4, 5, 6, 7).	May be found in any time slot to represent the location where decimal point will be displayed on DPO CRT.
?	Display jumps to next channel	Display jumps past remaining time slots to next channel.
e f g h	Modifies text that is displayed. *Inserted by software only. Terminal prints them upper case.*	These commands are used in time slot #1 to provide zero's adding and prefix shifting for scale factor readouts.
b	CRT displays "I"	
Control Char.	Non-printing	

NOTE

These codes may be subject to special interpretation by other software routines.

EXAMPLE #1. (Underscored characters are operator typed.)

```
** PSF
PRINTS SCALE FACTOR MESSAGE ON TERMINAL (PSF)
DEPRESS DESIRED MEMORY LOCATION
TEKTRONIX HOPES THAT YOUR NEW DPO SYSTEM AIDS IN KEEPING
YOUR GEAR ON THE AIR . . .
THIS LAST LINE IS NOT PRINTED ON THE DPO CRT . . .
MESSAGE COMPLETE
**
```

FRONT PANEL INTERRUPT TEST (FPT)

DESCRIPTION:

The Front Panel Interrupt Test verifies that all Front Panel pushbuttons generate the correct interrupt.

The sequence of the test is:

1. Each Front Panel button is lighted (except Program Call buttons 1-15) in turn by the controller.

2. After the lamp is turned on, you will be instructed to press the button that is lighted.

3. This generates an interrupt which the controller will recognize.

4. The Front Panel status is evaluated to see if the button lighted is the same as the button that was pressed.

STARTING OPTIONS:

When entering the Front Panel Interrupt test from monitor, you can select any starting point by following the test command with a hyphen ("-") and the name of the desired starting button in either the Data Handling, Memory Location or Program Call areas of the Front Panel.

The names of the Memory Location buttons are recognized by entering A, B, C, or D.

The Data Handling buttons are recognized by entering STORE, SEND, or RECEIVE. (HOLD is not included in this test.)

The program Call buttons are entered as C1 through C15.

SWITCH OPTIONS:

/S will cause the software to repeat the same button test after an interrupt has occurred.

/E suppresses any error output.

/R will repeat the button test and output only an error count, (Ø or 1 in this test).

Errors that occur are printed and compared to what the Front Panel status should have been and what it actually was.

The software instructions printed on the terminal are self-explanatory.

POWER FAIL MEMORY TEST (PFM)

DESCRIPTION:

This test is valid only if core memory is available in the P7001 Processor.

The software writes all "1's" into the processory memory, and instructs you to turn off the power to the DPO. When the power off interrupt has been decoded by the software, a message to turn the DPO on again is printed on the terminal. Memory is then checked to see if the original pattern of 1's was retained.

LISTING OF CALLS (LIS)

This routine prints on the terminal the name and mnemonic of each test available. See Appendix A for the complete listing of names and mnemonics for tests. The listing also contains notes to identify the special control and switch option functions.

RUNS ALL TESTS (ALL)

While not a test itself, this routine allows you to run every test through the use of only one test command. Tests are run in the sequence shown with the LIS command. This is considered to be the best sequence of tests.

STARTING OPTIONS:

When entering the ALL test from Monitor, you can select any starting test by following the test command with a hyphen ("-") and the mnemonic of the desired starting test. This will permit you to begin the ALL test at any point in the normal sequence. Tests before the starting point will be skipped.

APPENDIX A

LISTING OF CALLS AND MNEMONICS

**LIS

THE FOLLOWING ARE TESTS THAT MAY BE CALLED WHEN IN MONITOR BY TYPING ITS (MNEMONIC)

DEVICE SELECT TEST (DST)

STATUS WORD CHECK (STA)

Z AXIS TEST (ZAT)

DATA TEST (DAT)

ADDRESS TEST (ADR)

WORST CASE TEST (WCT)

MEMORY PATTERN TEST (MPT)

POWER FAIL MEMORY TEST (PFM)

ZERO DISPLAY GEN TEST (PFM)

DISPLAY GENERATOR ACCURACY TEST WAVEFORM (DGA)

X-Y DISPLAY PATTERN (XYD)

CALIBRATION PATTERN (CAL)

TRANSFER OF MEMORY LOCATION DATA (XFR)

X-Y INTENSITY TEST (XYI)

ANALOG TO DIGITAL CONVERTER TEST (A2D)

READOUT TEST (ROT)

READOUT SCALE FACTOR STORE TEST (SFS)

READOUT ROM TEST (RRT)

MULTIPLE MEMORY LOCATION STORE TEST (MMS)

WRITES MESSAGE FROM TERMINAL ONTO CRT (WRI)

PRINTS SCALE FACTOR MESSAGE ON TERMINAL (PSF)

FRONT PANEL INTERRUPT TEST (FPT)

LISTING OF CALLS (LIS)

RUNS ALL TEST (ALL)

NOTE: THE FOLLOWING ARE SPECIAL CONTROL CHARAS

↑P ABORTS THE EXISTING PROGRAM AND RETURNS TO MONITOR

↑E OMITS ERROR MESSAGES SWITCH

↑S SCOPE LOOP SWITCH — REPEATS TEST INDEFINITELY

↑X CLEARS ALL PREVIOUS SPECIFIED SWITCHES

↑R REPEATS TEST AND COUNTS ERRORS ONLY

NOTE: THE FOLLOWING ARE SWITCH OPTIONS

/E OMITS ERROR MESSAGES

/S PLACES ROUTINE IN A SCOPE LOOP

/R REPEATS TEST AND COUNTS ERRORS ONLY

APPENDIX B

LOADING BOOTSTRAP AND ABSOLUTE LOADERS

Bootstrap Loading

The Bootstrap Loader consists of machine-language instructions that direct the computer to accept from paper tape and place in core a limited amount of bootstrap formatted data. In short, Bootstrap is the minicomputer's first lesson in paper-tape readers and paper tape. Since it is a first lesson, it follows that Bootstrap itself must be loaded through a medium other than paper tape. This first medium of communication is the PDP-11 front-panel toggle switches.

Preliminary Information on Bootstrap

Toggling the Bootstrap Loader into the PDP-11 minicomputer is accomplished by using the following front-panel switches: ADDRESS/DATA (these switches are numbered Ø to 15 or 17, depending upon which member of the PDP-11 family is in use), LOAD ADRS (loads addresses from ADDRESS/DATA switches), and DEP (deposits data from ADDRESS/DATA switches into the presently addressed location). Before toggling in the Bootstrap Loader, make sure that the ENABLE/HALT switch is placed down to the HALT position. Next, place all ADDRESS/DATA switches in the down position. With the preceding accomplished, ENABLE/HALT to HALT and all ADDRESS/DATA switches in the down or "Ø" position, press down fully on the START switch and then release it. These manipulations of the PDP-11 front-panel switches will ensure minicomputer receptiveness of the Bootstrap Loader.

The first step in toggling in Bootstrap is to place the beginning address into the switch register. This address and subsequent Bootstrap Loader addresses will consist of six octal digits, the two most significant digits being used to designate the highest available memory bank. The octal addresses for the Bootstrap Loader are contained within Table B-1. The two most significant digits required for designating the highest available memory bank are contained within Table B-2. To see how the first address for a 16K memory is set into the switch register, refer to Figure B-1.

TABLE B-1

Bootstrap Loader

Octal Address	Octal Instruction
xx7744[1]	Ø16ØØ1
xx7746	ØØØØ26
xx775Ø	Ø127Ø2
xx7752	ØØØ352
xx7754	ØØ5211
xx7756	1Ø5711
xx756Ø	1ØØ376
xx7762	116162
xx7764	ØØØØØ2
xx7766	xx74ØØ
xx777Ø	ØØ5267
xx7772	177756
xx7774	ØØØ765
xx7776	[2]

[1] See Table B-2 for value of xx

[2] 177560 for TTY or Tektronix 4911 Reader/Perforator, or 177550 for a high-speed paper-tape reader

TABLE B-2

Memory Bank Designations

Memory Bank	Memory Size	Value of xx
Ø	4K	Ø1
1	8K	Ø3
2	12K	Ø5
3	16K	Ø7
4	2ØK	11
5	24K	13
6	28K	15

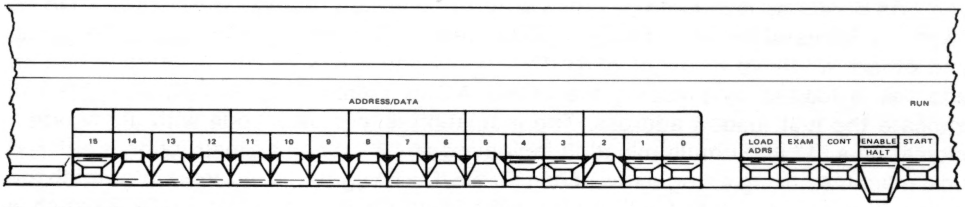
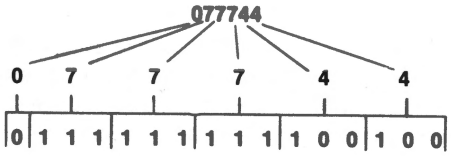


Fig. B-1. Switch positions for entering the first Bootstrap address into PDP-11 with 16 K of memory.

In toggling addresses or instructions into the PDP-11, the octal information contained within Tables B-1 and B-2 is mentally converted to binary code (1's and Ø's). This binary code is then entered into the PDP-11 switch register via the ADDRESS/DATA toggle switches by placing each switch in the position corresponding to the required binary code — switch up corresponds to a binary "1" and switch down corresponds to a binary "Ø". To understand the relationship between octal information and its corresponding binary code representation in the PDP-11 toggle switches, compare the switch positions in Figure B-1 with their binary/octal conversion in Figure B-2.



A. Octal to binary conversion of first Bootstrap address for PDP-11 with 16K of memory.

octal digit	three bit binary code weights:	4	2	1
0		0	0	0
1		0	0	1
2		0	1	0
3		0	1	1
4		1	0	0
5		1	0	1
6		1	1	0
7		1	1	1

B. Table for converting octal to three bit binary code.

Fig. B-2. Binary/Octal Conversion table.

Toggling in Bootstrap

Once the binary code for the first Bootstrap address, xx7744, has been placed into the ADDRESS/DATA switches, press the LOAD ADRS switch down, and then release it. Next, place into the ADDRESS/DATA switches the instruction from Table B-1, Ø16700, that corresponds to the just loaded address, xx7744. With this instruction in the ADDRESS/DATA switches, push up fully on the DEP switch and then release it. Upon release of the DEP switch, the instruction will be deposited in memory. To load the second instruction, ØØØØ26, place its binary representation into the ADDRESS/DATA switches and lift the DEP switch. When the DEP switch is lifted, the first address, xx7744, will be incremented by two, thus bringing up the second address, xx7746. Releasing the DEP switch will deposit the second instruction into the second address. Load the third instruction and continue loading instructions in the sequence of Table B-1 by placing the binary code for the instruction into the ADDRESS/DATA switches and then lifting and releasing the DEP switch.

NOTE

Lifting the DEP switch causes the minicomputer to automatically increment the address only when the preceding operation was a DEPosit. When the preceding operation was something other than DEPosit, such as LOAD ADRS or EXAM, lifting the DEP switch will not increment the address. In all cases, release of the DEP switch causes the contents of the ADDRESS/DATA switches to be placed in memory.

As Bootstrap is toggled in, note the front-panel lights above the ADDRESS/DATA switches. Some of the PDP-11 family will have a single row of ADDRESS/DATA lights, and others will have a row of ADDRESS lights and a row of DATA lights. When an address is loaded by pressing the LOAD ADRS switch, the front-panel lights will indicate the just loaded address. The indication is in binary code with illumination indicating a "1" and nonillumination indicating an "Ø". When an instruction is entered on a machine having a single row of ADDRESS/DATA lights, the address into which the instruction is being loaded will appear in the front-panel lights while the DEP switch is up; when the DEP switch is released, the just entered instruction will be displayed. On machines having two sets of lights, an ADDRESS row and a DATA row, activation of the DEP switch will cause the affected address and the deposited instruction to be displayed by their respective indicator lights.

After Bootstrap is toggled in, it is a good idea to go back and examine the contents of each memory location for correctness. This examination is initiated by first ensuring that the ENABLE/HALT switch is in the HALT position. Next, place the first address, xx7744, into the ADDRESS/DATA switches and press LOAD ADRS. For machines having a single row of ADDRESS/DATA lights, after pressing LOAD ADRS, press and release the EXAM switch. The instruction residing in the first location will be displayed in the ADDRESS/DATA lights. Pressing and holding the EXAM switch will cause the next address to be displayed; and upon release of the EXAM switch, the contents of that location will be displayed.

For those machines having separate ADDRESS and DATA lights, make sure that the ENABLE/HALT switch is in HALT. Place xx7744 into the ADDRESS/DATA switches and press LOAD ADRS. Press EXAM — the address, xx7744, and the instruction will appear in their respective displays. To examine the next location and its contents, operate the EXAM switch again and so on until all locations have been examined.

NOTE

Pressing the EXAM switch causes the minicomputer to automatically increment the address only when the preceding operation was an EXAMine. When the preceding operation was something other than EXAMine, such as LOAD ADRS or DEP, pressing the EXAM switch will not increment the address. In all cases, release of the EXAM switch will cause the contents of the EXAMined address to be displayed.

In the event that an examined location's contents are incorrect, load that address into the minicomputer and place the correct instruction into the ADDRESS/DATA switches. Next, lift the DEP switch to deposit the correct instruction in memory.

In summary, the Bootstrap Loader is entered by:

1. Place the ENABLE/HALT switch to the HALT position.
2. Place all ADDRESS/DATA switches down to the "Ø" position.
3. Press START on the PDP-11. (Steps 1 through 3 are in initialization procedure.)
4. Place the first address, xx7744, into the ADDRESS/DATA switches. The xx is chosen from Table B-2 to designate the highest available memory bank.
5. Press LOAD ADRS.

6. Place the first instruction, Ø67Ø1, into the ADDRESS/DATA switches and lift up on the DEP switch.

7. Place each subsequent instruction from Table B-1 into the ADDRESS/DATA switches and load each by lifting the DEP switch.

8. Once all instructions have been loaded, use the EXAM switch to inspect all Bootstrap Loader addresses for correct contents.

Absolute Loader

Once the Bootstrap Loader has been toggled in, the Absolute Loader may be read into the PDP-11 with a paper-tape reader. To be compatible with the Bootstrap Loader, the Absolute Loader is punched in bootstrap format.

The Absolute Loader paper tape begins with a blank leader that is followed by several feet of special bootstrap leader. This special bootstrap leader, as opposed to the normally blank leader of absolute binary tapes, is punched with ASCII code 351 (see Figure B-3). The instructions that follow this special leader make up a systems program that, once in core, will allow the PDP-11 to accept paper tape punched in asbolute binary format. The trailer that follows these instructions is blank except for the reader sprocket holes.

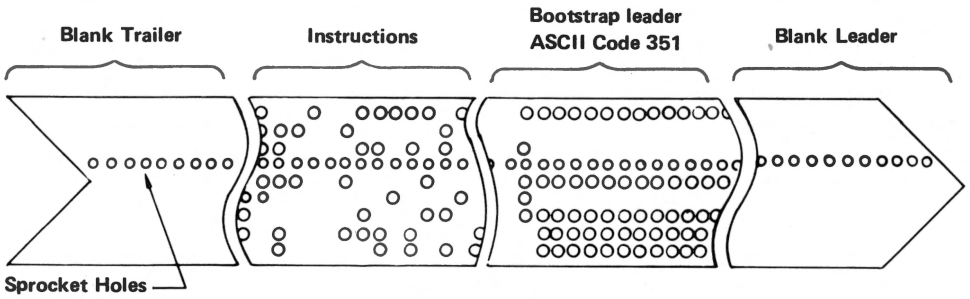


Fig. B-3. Absolute Loader paper tape.

To read the Absolute Loader into the PDP-11:

1. Place the ENABLE/HALT switch in the HALT position.

2. Place all ADDRESS/DATA switches down to the "Ø" position.

3. Press START on the PDP-11. (Steps 1 through 3 are an initialization procedure.)

4. Place xx7744 into the ADDRESS/DATA switches and press LOAD ADRS. The value of xx designates the highest available memory bank and may be found in Table B-2.

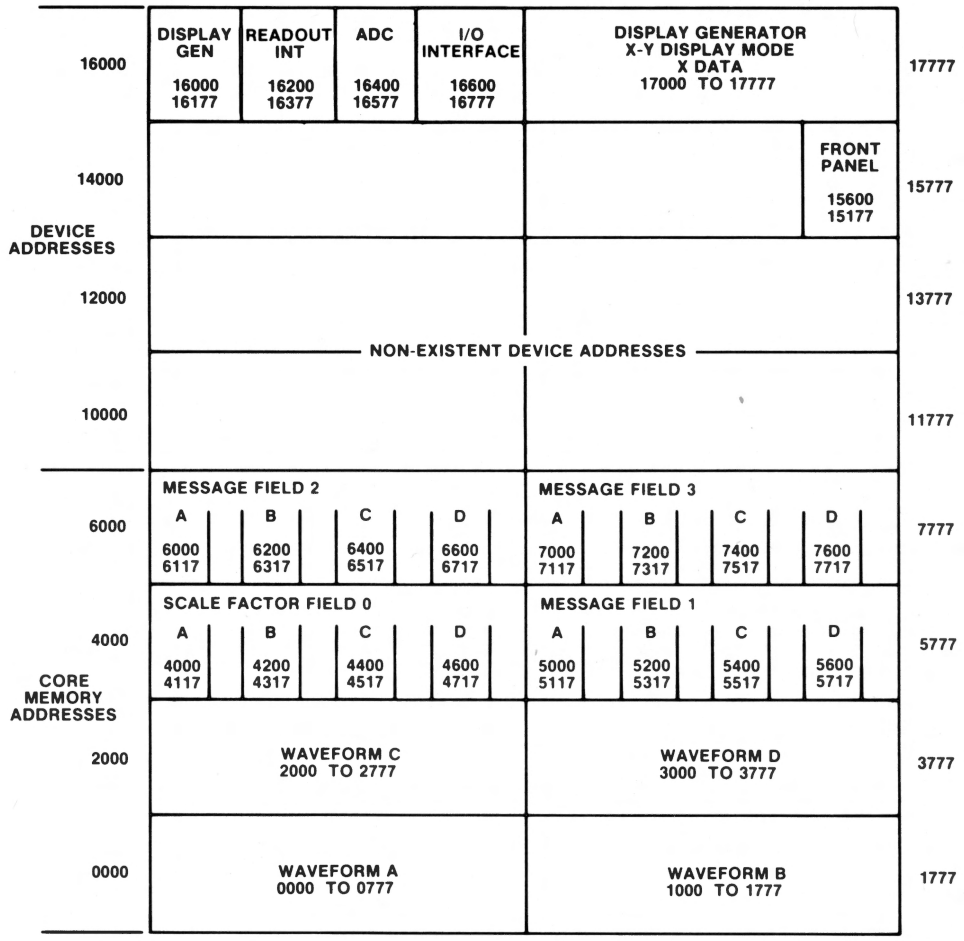
5. According to the instruction manual for the reader in use, place the Absolute Loader tape into the paper-tape reader. Make sure that the reader's feed sprocket engages the paper tape and that the ASCII 351 leader resides over the reader sensors.

6. Place the ENABLE/HALT switch in the ENABLE position.

7. Press START on the PDP-11. The tape should move through the reader and stop at the blank trailer. Correct loading is indicated by xx75ØØ (xx7476 for PDP-11/15 or PDP-11/20) appearing in the address lights. If the tape does not pass through the reader after pressing START, EXAMine the Bootstrap Loader to make sure that it is correctly entered and then repeat the procedure for entering the Absolute Loader.

APPENDIX C

P7001 ADDRESS MAP



All Addresses are in Base 8

MANUAL CHANGE INFORMATION

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