Tektronix®

PM112

PERSONALITY MODULE FOR THE MULTIBUS

INSTRUCTION MANUAL

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PM112
PERSONALITY MODULE FOR THE MULTIBUS

INSTRUCTION MANUAL

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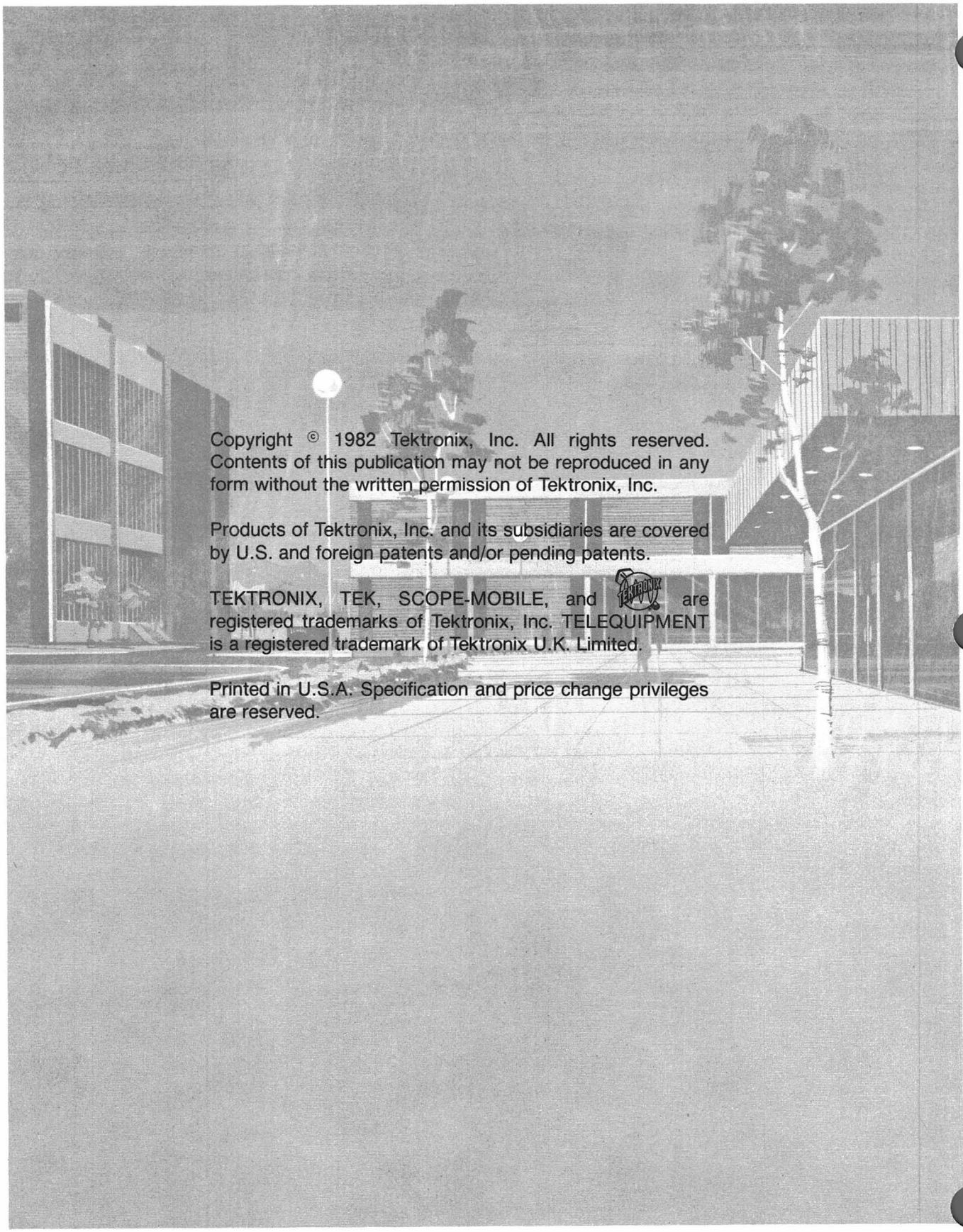

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WARNING

The following service instructions are for qualified personnel only. To avoid personal injury, do not perform any servicing other than that contained in operating instructions unless you are qualified to do so.

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OPERATOR'S SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and service personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or to other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Grounding the Product

This product is grounded through the grounding conductor of the logic analyzer power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting the product input or output terminals. This protective ground connection is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective ground connection, all accessible conductive parts can render an electric shock.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been certified for such operation.

Do Not Operate Without Shield

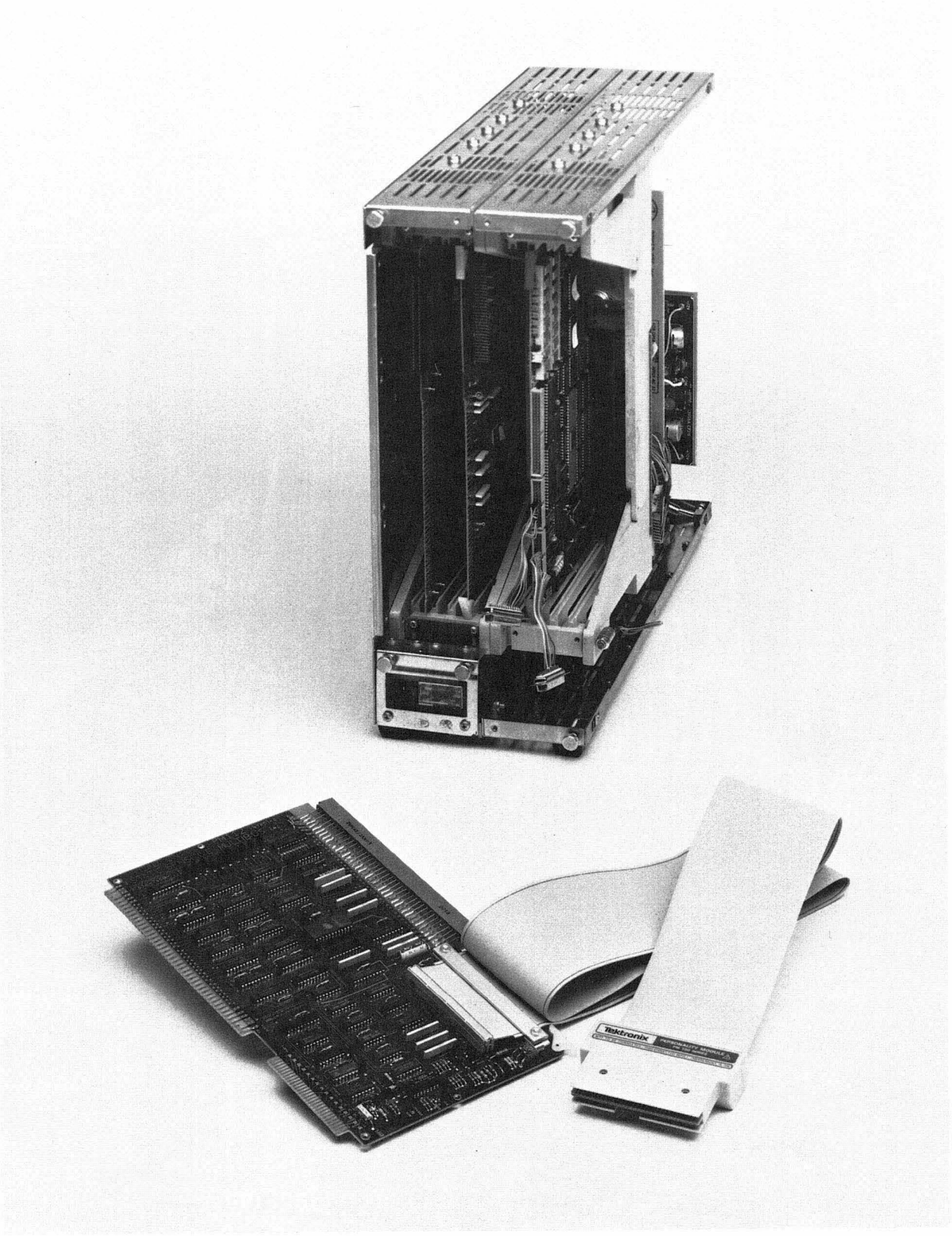
To avoid instrument damage, do not operate this product without its insulating shield installed.

Disconnect Power Before Servicing

Disconnect power before removing insulating shield, soldering, or replacing components.

Conductive Jewelry

Do not wear conductive jewelry while servicing the PM 112.



PM 112 Personality Module
(shown with a Multibus-type cardcage)

INTRODUCTION

ABOUT THIS MANUAL

Overview

This manual describes operation and servicing of the PM 112 Personality Module.

The operator's portion provides an overview of the PM 112, connection instructions, operation information, and specifications.

The service portion is located after the colored divider. It contains maintenance information, circuit descriptions, performance check procedures, diagnostic and service procedures, schematics, and parts lists. The service portion of this manual is intended to be used only by qualified service personnel.

At the rear of the manual is a signal glossary. It gives a brief description of signals going to and from the PM 112. After the signal glossary you will find a tab divider, behind which manual change information may be placed.

Conventions Used In This Manual

The following is a list of conventions used throughout this manual:

- Unless distinctions are relevant to operation of the PM 112, any version of Intel's Multibus specification, including the IEEE P796 Proposed Microcomputer System Bus Standard (proposed October, 1980), will be referred to as a Multibus specification or a Multibus system under test (SUT). (Multibus is a registered trademark of the Intel Corporation.) Where mentioned, the IEEE version of the Multibus will be referred to as the IEEE P796 bus.

- All of the simulated 7D02 displays in this manual depict a 7D02 equipped with the Timing Option. The Timing Option causes TIMING WR=X to appear in the word recognizer displays, allows a choice between a MAIN or TIMING trigger in the trigger displays, and causes MAIN to appear following ACQMEM in the bottom inverse video portion of the acquisition memory display.

  The 7D02 need not be equipped with the Timing Option for use

with the PM 112. Operation instructions for the Timing Option are provided in the 7D02 Operator's Manual.

- In the text an (H) or (L) following a signal name indicates that the signal is asserted in the (high) or in the (low) electrical state.

- On the circuit diagrams a bar ($\overline{\ }$) over a signal name or portion of a signal name indicates that the signal is asserted in the low electrical state.

  The PM 112 shares many of the 7D02 logic analyzer's line names. Therefore, on a PM 112 circuit diagram, the absence of a bar over a line name does not necessarily mean that the signal carried is asserted in the high electrical state.

- On the logic analyzer's display screen and in this manual's simulated screen displays, a slash (/) preceding a field name or portion of a field name indicates that a 0 placed in this field will specify the active condition. For example, placing a 0 in the R/W field will specify that a Write operation be the active condition. (Note that it is possible to invert the active condition for a field, using bus inversion in the Format mode. Doing this will not change the appearance of the field's name on the display.)

- Slashes (/) are also used to denote an active low signal on circuit board mnemonic labels, and are used in the text when referring to board labels.

Other References

The Tektronix 7D02 Logic Analyzer (with Expansion Option) supports the PM 112. You will need to be familiar with the following documentation:

- 7D02 Logic Analyzer Operators Manual (070-2918-00)

- 7D02 Logic Analyzer Service Manual (070-2919-00)

You should also have access to and be familiar with all literature supporting the system under test, including microprocessor documentation, and documentation for the version of bus specification used.

INTRODUCTION TO THE PM 112

The PM 112 Personality Module is designed to facilitate logic analysis of systems based on Intel Multibus and IEEE P796 bus specifications. This is achieved in the following ways:

- The PM 112 connects the logic analyzer to a Multibus system under test (SUT). It plugs into the SUT's backplane in the same manner as any other Multibus-compatible circuit board, and gives the logic analyzer access to all address, data, status, and clock lines. Rather than acting as a bus master or slave, the PM 112 acquires information on the bus as a passive listener. Because the PM 112 monitors only the bus, it does not directly monitor microprocessor operations, and does not follow such on-board functions as local memory programs.

- Hardware in the personality module isolates, buffers, latches, and in some cases encodes information from the SUT bus. The information is organized in a format which is standard to the logic analyzer. Together the PM 112 and the logic analyzer generate a state clock which is used to strobe information from the PM 112 to the logic analyzer's acquisition memory.

- If all the slots in the backplane are in use, the PM 112 can act as an extender for the P1 bus connector.

- Firmware in the personality module personalizes the logic analyzer's display for use with Multibus SUTs, and allows the logic analyzer to disassemble bus commands into descriptive command mnemonics. Because the Multibus specification can be used with a variety of microprocessors, no disassembly of specific microprocessor mnemonics is performed.

NOTE

For use with the PM 112, the 7D02 Logic Analyzer should be equipped with the Expansion Option (Option 03).

Jumper Wires (Optional Accessory)

You may require jumper wires for connecting the user-defined control (UDC) lines to various bus signals not accessed by UDC jumper straps. In particular, jumper wires are necessary for connecting UDC lines to the upper four address lines (ADR14(L)-ADR17(L)(HEX)) in Multibus systems using 24-bit addressing. A set of ten 40 cm Individual Connector wires (with female square-pin connectors at one end and Pomona Grabbers at the other) can be ordered as an optional accessory (part number 012-0670-00).

OPERATION INSTRUCTIONS

CONNECTING THE PM 112

CAUTION

Always switch the logic analyzer mainframe power off before connecting the personality module. Always switch off system-under-test (SUT) power before inserting the personality module into the SUT backplane. Failure to take these precautions may cause permanent damage to the logic analyzer, the personality module, and the system under test.

CONNECTING THE PM 112 TO THE LOGIC ANALYZER

1. Switch OFF logic analyzer mainframe power.
2. Insert the PM 112's logic analyzer plug, label side up, into the logic analyzer's front panel receptacle.

NOTE

For use with the PM 112, the 7D02 Logic Analyzer should be equipped with the Expansion Option (Option 03).

CONNECTING THE PM 112 TO THE SYSTEM UNDER TEST (SUT)

WARNING

Dangerous voltages may be present within your SUT. Before disassembling the SUT and/or connecting the PM 112, consult documentation supporting the SUT for safety and servicing information. Be sure to perform work as directed, or if required, have the work performed by qualified service personnel.

1. Switch off power to the SUT and the logic analyzer.
2. Ground yourself to drain static electricity.
3. Check to be sure that the jumper strap on jumper W3085 (located on the edge of the PM 112 circuit board near the ribbon cable) is placed in the NORM (rather than the TEST) position. If you do install the PM 112 configured in the self-test mode, the acquisition display DATA values will

appear as all zeros on the display screen. This serves as a reminder to move the jumper to the NORM position.

4. If your SUT uses parallel bus priority resolution, you will want to place the strap on jumper W3015 (shown in Figure 2-6) in the PAR position; if serial bus priority resolution is used place this strap in the SER position.

5. At this point you may wish to re-configure the user-defined control (UDC) lines. These lines enable the user to monitor a variety of signals, including the upper four address lines of later bus specifications that use 24-bit addressing. Refer to USING UDC LINES in this section.

6. Insert the personality module circuit board into a free slot in the SUT's backplane, with the PM 112's components facing the same direction as those of the SUT's.

CAUTION

When inserting or removing the PM 112, take care to avoid touching components on neighboring circuit boards; electrical and/or physical damage can occur to both the PM 112 and the system under test.

If all slots in the backplane are being used or if the remaining slots are inaccessible, the PM 112's extender socket may be used. Remove one of the SUT's circuit boards that does not require access to the P2 bus connector (the PM 112's extender carries only P1 signals), and insert the PM 112 in its place. Then insert the displaced circuit board into the PM 112's extender socket.

CAUTION

A short-circuit on the PM 112 extender's power runs can cause damage to the SUT and to the PM 112. To prevent damage, be sure that no conductive materials contact the P1 extender's socket assembly. Refer to Specifications section for extender power run current limits.

7. Switch on logic analyzer mainframe power, and power up your system under test.

DISCONNECTING THE PM 112

1. Be sure that power to both the logic analyzer and to the SUT is switched off when disconnecting the PM 112 from the SUT and/or the logic analyzer.

2. Ground yourself to drain static electricity.

3. Use the white plastic ejector tab (at the ribbon cable corner of the PM 112) to remove the circuit board from the SUT backplane. Avoid contacting components of neighboring circuit boards while removing the PM 112.

STORING AND TRANSPORTING THE PM 112

The PM 112 should be stored and transported in its carrying case using the original packing materials. The carrying case is designed to protect the module from static electricity and physical impact. Keep the personality module in a clean area where the temperature remains between -62 and +85 degrees centigrade, and where humidity does not exceed 95% (non-condensing). Do not flex the PM 112's ribbon cable at temperatures below -15 degrees centigrade.

USING THE PM 112

The 7D02 Operator's Manual provides general operating information for use with all PM 100 Series personality modules. However, the 7D02 will operate slightly differently with each personality module. This subsection is devoted specifically to operating the 7D02 with the PM 112 Personality Module.

The 7D02 screen displays of the word recognizer, acquired data, clock qualifiers, and FORMAT mode all contain elements that are specific to the PM 112, and are discussed in the following subsections.

WORD RECOGNIZER DISPLAY

The word recognizer can be used to specify recognition of a reference point (trigger event) in the SUT's program for general data acquisition and storage. It can also be used for data qualification, specifying that all information stored in the acquisition memory conforms to parameters selected in the word recognizer. Refer to the 7D02 Operator's Manual for detailed programming information.

When the PM 112 is attached to the 7D02, the 7D02 WD RECOGNIZER key will produce the display shown in Figure 2-1.

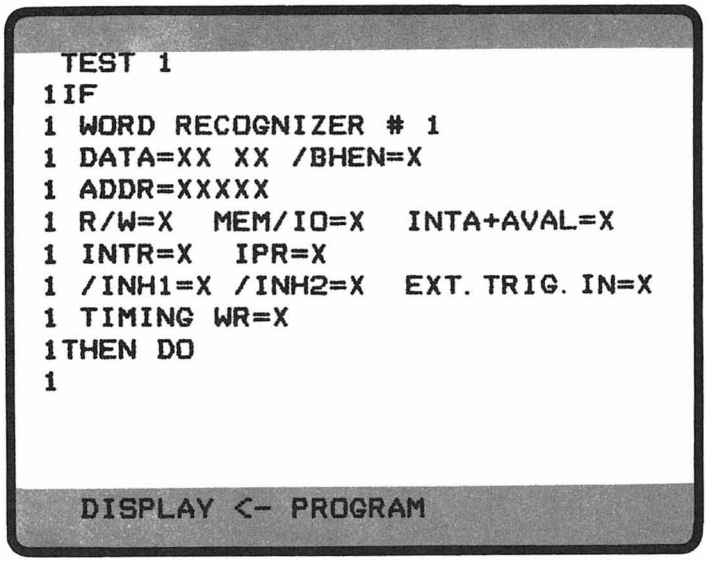


Figure 2-1. 7D02/PM 112 word recognizer display. This display shows the default radices of the address, data and IPR field values (hexadecimal, hexadecimal, and octal, respectively). You can change these radices, as well as invert any word recognizer field value, in the 7D02's FORMAT mode.

A 1 or a 0 should always be entered in the INTA+AVAL field. If you leave this field don't cared (Xed) the word recognizer will not distinguish I/O operations from Bus Available/Interrupt Acknowledge cycles, nor will it distinguish memory transfers from invalid cycles. These cycle relationships are defined in Table 2-1.

Word Recognizer Fields

The following paragraphs describe elements in the 7D02 word recognizer display that are specific to the PM 112:

DATA--These are actually two separate fields representing recognition values for the high and low bytes of the data bus. While the signals on the data bus are active low, they are firmware-inverted to appear active high on the display. They are normally displayed in hexadecimal radix unless changed in FORMAT mode. FORMAT mode BUS INVERSION also allows you to specify DATA recognition values in their active low form.

During 8-bit cycles (or any time BHEN(L)=1), the high byte of the DATA field specifies recognition values on the eight user-defined control (UDC) lines. Normally BHEN(L)=1 on 8-

bit data transfers, but you can force BHEN(L) to appear permanently high to the PM 112 by moving a jumper strap (see Monitoring UDC Lines on All Cycles, in this section under USING UDC LINES). Moving this jumper will cause the high DATA byte to specify UDC recognition values on all cycles.

NOTE

When you change the word recognizer DATA field's radix to octal, remember that this field is split into two separate bytes. The most significant octal digit in each of the fields represents only two bits and therefore has a maximum value of 3. For example, to specify recognition of the 16 bit octal word 177777 (all binary 1s), you must enter the value 377 377 (again all binary 1s) in the two DATA fields.

Because the acquisition memory display's DATA field is not split on 16 bit cycles, the number will there be represented as 177777.

/BHEN--When this Multibus signal is asserted (low), it indicates that the high byte on the data bus is enabled (a 16-bit data transfer is taking place). Therefore, when you enter a 0 in the word recognizer /BHEN field, you specify that the value in the upper half of the word recognizer DATA field is expected on the upper data bus. Entering a 1 specifies that the value in the upper half of the DATA field is expected on the UDC lines.

ADDR--This is a 20-bit address field. You can change its radix and/or invert its values in FORMAT mode. The default is hexadecimal radix, with bus signals inverted to appear active high on the display. If you are testing a system using 24-bit addressing, you may wish to monitor the upper four address bits ADR14(L)-ADR17(L)(HEX) with user-defined control (UDC) lines. Refer to USING UDC LINES in this section of the manual.

R/W--By entering a 1 in this field of the display, you specify recognition of a Read operation. Entering a 0 specifies a Write operation.

MEM/IO--By entering a 1 in this field, you specify recognition of a data transfer to/from memory. Entering a 0 specifies an I/O operation.

INTA+AVAL--By entering a 1 in this field you specify that the event recognized be either an Interrupt Acknowledge, or

a cycle on which the bus is Available (i.e., BUSY(L) is not asserted - either the bus is not in use or a Bus Exchange is taking place). A 0 specifies that the recognized event is not to be any of those above.

Table 2-1 summarizes the types of cycles that can be specified using the R/W, MEM/IO and INTA+AVAL fields of the word recognizer.

NOTE

A 1 or 0 should always be specified in the INTA+AVAL field. If you leave this field don't cared (Xed), the word recognizer will not distinguish I/O operations from Bus Available/Interrupt Acknowledge cycles, nor will it distinguish memory transfers from invalid cycles. These relationships are defined in Table 2-1.

INTR--By entering a 1 in this field of the word recognizer display you specify recognition of a cycle on which at least one Interrupt Request is pending. 0 specifies that no requests be pending. (This line is active low on the bus, but is inverted by PM 112 firmware to appear active high on the display.)

IPR--You can specify recognition of an interrupt's priority from zero to seven in this field (zero is the highest priority interrupt). Only the highest priority interrupt request can be seen by the PM 112 on a given cycle. For example, if interrupts of priority 2 and 4 are both pending, only priority 2 can be recognized. When INTR=0, IPR will always have the value 7 (lowest priority). Bits in this field may be individually don't-cared (Xed) if the binary radix is selected. For example, you could use this method to define the event to be recognized as an interrupt of priority higher than 4 (i.e., 0, 1, 2, or 3) by specifying IPR=0XX.

/INH1--By entering a 0 in this field you specify recognition of cycles on which RAM is inhibited (when ROM or memory-mapped I/O is being addressed).

/INH2--By entering a 0 in this field you specify recognition of a cycle on which ROM and memory mapped I/O are inhibited (when RAM is being addressed).

Table 2-1
DISTINGUISHING CYCLE TYPES

INTA+AVAL[1]	MEM/IO	R/W	Cycle Type	Acquisition Memory Display Mnemonic
0	0	0	I/O Write	IOW
0	0	1	I/O Read	IOR
0	1	0	Memory Write	MWT
0	1	1	Memory Read	MRD
1	0	0	Bus Available[2]	AVL
1	0	1	Interrupt Acknowledge	INA
1	1	0	Invalid[3]	***
1	1	1	Invalid[3]	***

[1] A 1 or 0 should be specified in the INTA+AVAL field, or the word recognizer will not distinguish I/O operations from Bus Available/Interrupt Acknowledge cycles, nor will it distinguish memory transfers from Invalid cycles.

[2] BUSY not asserted. Indicates either bus is not in use or Bus Exchange.

[3] Should not occur with properly operating PM 112, logic analyzer, and SUT. See note [1] .

TRIGGER DISPLAY (CLOCK QUALIFICATION)

The only two aspects of the 7D02 trigger display specific to the PM 112 are clock qualification and use of the System Under Test Halt feature. Figure 2-2 shows the 7D02/PM 112 Trigger Menu. Refer to the 7D02 Operator's Manual for general information on trigger use.

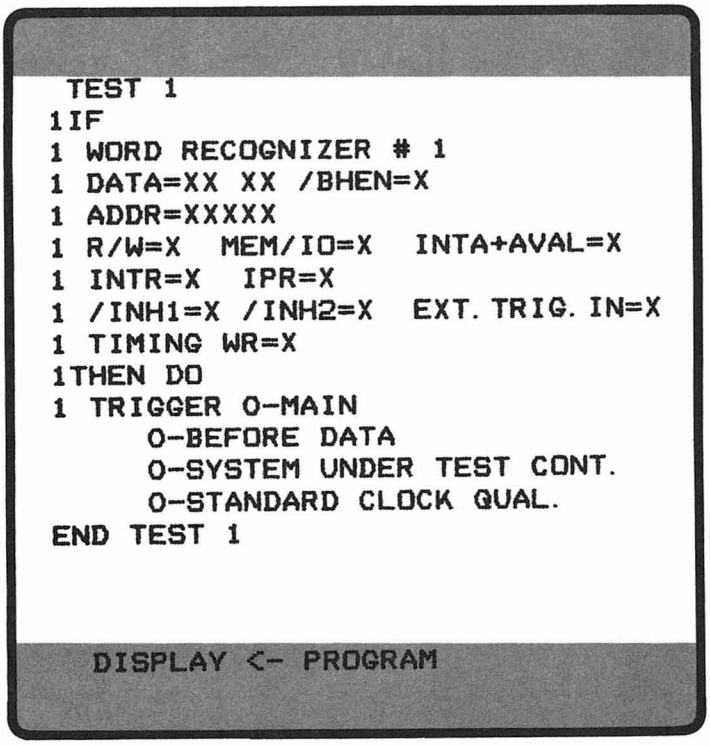


Figure 2-2. 7D02/PM 112 trigger display. This display shows the trigger display following the word recognizer. Clock qualification and the SYSTEM UNDER TEST CONT. (HALT) feature are the only items of the trigger display that are specific to the PM 112 (see text).

This display shows one of the most basic programs possible for data acquisition. To call up this program, press the TRIGGER button after the 7D02 has powered up.

System Under Test Halt

The HALT SUT(L) signal is accessed in the trigger menu by moving the cursor to the SYSTEM UNDER TEST CONT. field. The menu will expand to offer:

```
0-SYSTEM UNDER TEST CONT.
  0 SYSTEM UNDER TEST CONT.
  1 SYSTEM UNDER TEST HALT
```

If you enter a 1 in this field, HALT SUT(L) will be asserted after data acquisition is completed. The line carrying this signal terminates at a square pin on the PM 112 circuit board marked /HALT SUT (see Figure 2-3). If you wish to use this feature, you must connect HALT SUT(L) by wire to an appropriate SUT line. When connecting, be sure to avoid electrical contention with existing Halt line inputs to the microprocessor. Refer to Specifications section for electrical information.

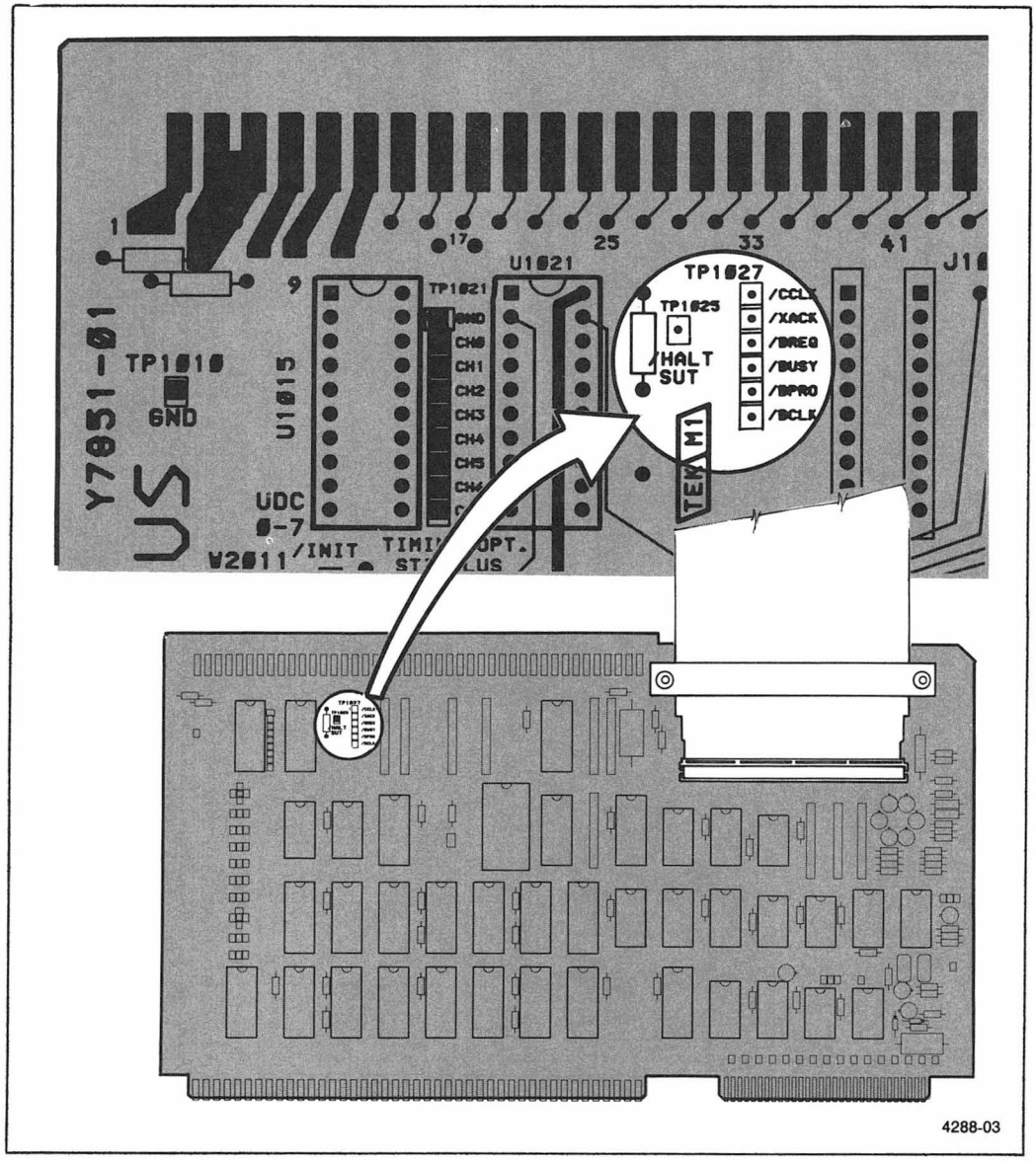


Figure 2-3. /HALT SUT Pin. The signal HALT SUT(L) will go low after data acquisition is complete, if you have selected this option in the trigger display. HALT SUT(L) terminates at this pin. To use the signal, you must connect it to an appropriate SUT line (see accompanying text, and electrical information in Specifications).

Clock Qualification

Clock qualification qualifies not only the nature of the trigger condition, but also the nature of all subsequent cycles of data that are stored.

Standard Clock Qualification. The PM 112 provides powerup default values for clock qualification (shown in trigger display as STANDARD CLOCK QUAL.) that are appropriate for most Multibus SUT users. Default clock qualification causes data to be acquired on the falling edge of every PM 112 clock signal, which is derived from the falling edge of XACK(L) ORed with the rising edge of BUSY(L). (Refer to the circuit diagrams and Theory of Operation for more information on clock generation.)

User Clock Qualification. You can select non-default values for the PM 112's clock qualification lines C9-C4. This causes the PM 112 clock signal to be qualified by the specified state of one or more of the Multibus signals carried on these lines.

NOTE

Deleting the trigger command from the 7D02 program will not remove user clock qualification values. Clock qualification can only be returned to default by replacing 0 in the STANDARD CLOCK QUAL. field, or by switching the logic analyzer mainframe OFF for five seconds, then back ON.

You access user clock qualification by moving the cursor to the trigger menu's STANDARD CLOCK QUAL. field. The menu will expand as follows:

```
0-STANDARD CLOCK QUAL.
  0 STANDARD CLOCK QUAL.
  1 USER CLOCK QUAL.
```

Entering a 1 in this field further expands the menu with EDGE OF CLOCK and ANDED CLOCKS selection fields:

```
1-USER CLOCK QUAL.
1-FALLING EDGE OF CLOCK
  0 RISING EDGE OF CLOCK
  1 FALLING EDGE OF CLOCK
C9-C4 (ANDED CLOCKS)=XXXXXX
```

(Note the default values. These are the values that are restored whenever you place 0 in the USER CLOCK QUAL. field.) You can choose the clock's falling edge by entering a 1 or by simply moving the cursor to the next field (falling edge is the default value).

By entering a 0 in the FALLING EDGE OF CLOCK field you can select the rising edge of the PM 112 clock. This is not recommended, as the PM 112 operates correctly only when using the falling edge of its clock signal.

C9-C4 are PM 112 control lines that carry Multibus signals, and can be used as clock qualifiers. Entering a 1 or 0 in one or more of these fields (C9 at left to C4 at right) causes the 7D02 to qualify (store) data on clocks occurring when the selected control lines are in their specified states. For example, if you specified C9 (the leftmost bit in the field) equal to 1, and C4 (the rightmost bit) equal to 0, then only those clocks on which C9 (BUSY(H)) = 1 and C4 (INH1(L)) = 0 would be qualified and stored.

The following paragraphs describe the clock qualifier signals carried on lines C9-C4:

C9 BUSY(H) This is the Multibus Bus Busy signal (inverted). BUSY(H)=0 indicates that no master is using the bus, or that an exchange of bus masters is taking place. By qualifying on C9=1, you can eliminate storage of cycles on which no master is using the bus.

C8 ACLO(H) In the Intel bus specification, this is the Multibus AC line voltage Low signal. In the IEEE specification this line is reserved; if you are testing this type of system, leave C8 don't cared (Xed).

C7 LOCK(L) A bus master generating LOCK(L)=0 prevents another processor from accessing the memory during read-modify-write operations. (In some early versions of the bus, this is the Advanced Acknowledge line, AACK(L). A master that detects AACK(L)=0 may eliminate some wait states.)

C6 CBRQ(L) This is the Multibus Common Bus Request signal. CBRQ(L)=1 indicates to the Bus Master that no other master is requesting the bus. Qualifying on C6=0 will cause the logic analyzer to sample only on those cycles on which the bus is being requested by multiple bus masters.

C5 INH2(L) This is the Multibus Inhibit ROM signal. It prevents ROM memory addresses from responding to the address on the bus, thereby enabling auxiliary (shadow) ROMs to override ROM memory and share address space. Qualifying on C5=1 will cause only the normal ROM accesses to be sampled.

C4 INH1(L) This is the Multibus Inhibit RAM signal. It prevents RAM memory devices from responding to the address on the address bus, enabling ROM or memory-mapped I/O devices to override RAM memory. Qualifying on C4=1 will cause only the normal RAM accesses to be sampled.

DISPLAYING ACQUIRED DATA

The PM 112 does not decode specific microprocessor mnemonics. The menu offering a choice of absolute or mnemonic display of data, located below the data display in inverse video, has no effect when the PM 112 is used with an Expansion Option-equipped 7D02.

NOTE

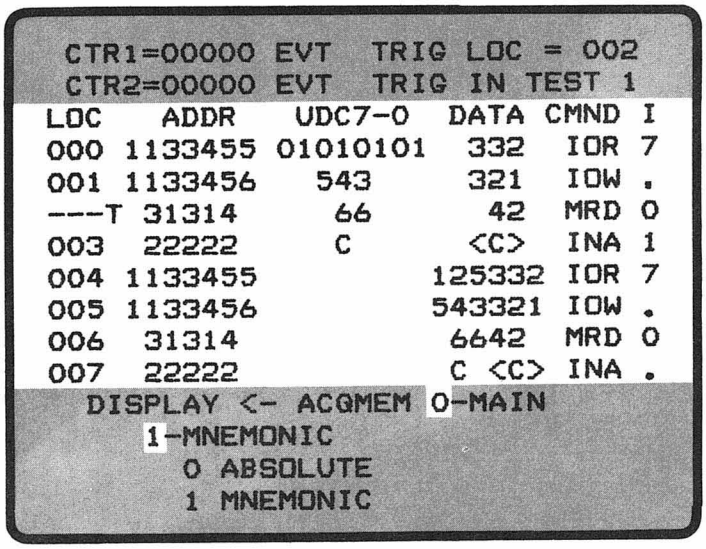
If the your 7D02 is not equipped with the required Expansion Option (Option 03), a special error display will occur when you attempt to display acquired data in the default mnemonic mode. This display notifies you that the Expansion Option is required. It also lists the PM 112 functions that are invalid without the expansion option: the upper eight data/UDC lines, the PM 112's upper four address lines (A19-A16), the interrupt request and encoded interrupt priority lines. If you use the PM 112 without the Expansion Option, the invalid word recognizer fields are ignored by the 7D02, but do not disappear from the screen.

If you wish to proceed with limited capabilities, the error display is exited by selecting "0 ABSOLUTE" in the menu at the display's bottom. Acquired data can then be displayed by the 7D02, but all values in the above-mentioned fields will be invalid.

When you use the default radices for the data display, each word (bus cycle) of data requires one line on the 7D02's screen. When you select binary radix for display of the address bus and/or data bus values, or if you select ASCII for display of the address bus value, then the display uses a three-line format for each word of data.

One-Line Data Display Format

Each word (bus cycle) of acquired data will appear on a single line when the address bus is being displayed in octal or hex radices and the data bus is being displayed in a non-binary radix. Figure 2-4 shows the one-line display format.



4288-04

Figure 2-4. Hypothetical one-line data display. This display shows how varying radix selections affect the formatting of fields in a one-line display. (In actual use the radices would not change from line to line of the display.) Line (LOC) 000 demonstrates octal radices for the address and data buses, and binary for the UDC lines. Line 001 demonstrates octal radices for all three fields. Line 002 is the trigger location (denoted by ---T) and demonstrates hexadecimal radix for all three fields. Line 003 demonstrates the address bus in hexadecimal, and the UDC lines and data bus fields in ASCII.

Lines 000-003 all show data on 8-bit (BHEN(L)=1) operations.

Lines 004-007 show the same information on 16-bit (BHEN(L)=0) operations. Note that the UDC field is empty and that an additional eight high-order bits appear in the data bus field.

The mnemonic/absolute menu at bottom has no effect on the data display when the PM 112 is used with an Expansion Option-equipped 7D02. (See the discussion of special Expansion Option conditions at the beginning of DISPLAYING ACQUIRED DATA.)

The following paragraphs describe the heading and contents of each column in the one-line format data display:

LOC — This column contains the acquisition memory location (000-255) of the word (bus cycle) of data displayed on each line. The oldest word of data is in location 000, the newest in location 255. The location of the trigger word is denoted by "---T" in place of the location number.

ADDR — This column contains the address bus value. The values of all 20 address lines are shown regardless of validity. For instance, all 20 address lines are shown on I/O cycles, even though only A15-A0 have meaningful information on these cycles.

(If you are testing a Multibus system having 24 address lines and wish to monitor ADR14(L)-ADR17(L)(HEX), the most significant four bits, you will need to use UDC lines. Refer to USING UDC LINES later in this section.)

UDC7-0 — This column contains the value of the eight user-defined control lines. UDC7 is located furthest left in the column, UDC0 furthest right. This field will be blank on 16-bit data-transfer cycles, unless BHEN(L) is forced to appear permanently low by using the 8/16 jumper strap (refer to USING UDC LINES later in this section).

DATA — This column contains the data bus value. Only the low byte is present on 8-bit cycles.

CMND — This column contains mnemonics identifying the type of cycle (the Multibus command that was being executed). The mnemonics are derived by encoding several of the Multibus command lines (as defined in Table 2-1). The identified cycle types are:

IOW	=	I/O Write
IOR	=	I/O Read
MWT	=	Memory Write
MRD	=	Memory Read
AVL	=	Bus Available (BUSY not asserted -- either bus not in use or Bus Exchange)
INA	=	Interrupt Acknowledge
***	=	Invalid (should not occur with correctly operating PM 112 and SUT)

I — This column contains interrupt request information. A number (0-7) in this column indicates the highest priority interrupt active on the cycle (0 is the highest possible priority). If no interrupt is pending, a "." will appear in this column.

Three-Line Data Display Format

Each data word (bus cycle) will require three display lines when binary radix has been selected for display of either the data or the address bus, or when ASCII radix has been selected for display of the address bus.

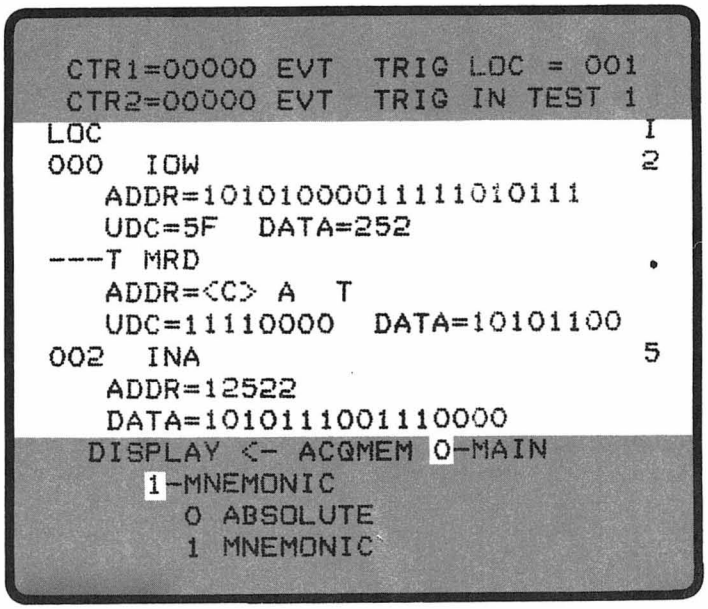


Figure 2-5. Hypothetical three-line data display. This display shows how varying radix selections affect the formatting of fields in a three-line format data display. (In actual use the radices would not change from line to line of the display). Line 000 (LOC) shows an 8-bit data operation; the address bus is in binary, the UDC lines are in hexadecimal, and the data bus is in octal. Line 001 is a trigger word (denoted by ---T), also an 8-bit operation, with the address in ASCII, and both the data bus and the UDC lines shown in binary. Line 002 shows a 16-bit operation with the address in hexadecimal and the data bus in binary.

The mnemonic/absolute menu at bottom has no effect on the data display when the PM 112 is used with an Expansion Option-equipped 7D02. (See the discussion of special Expansion Option conditions at the beginning of DISPLAYING ACQUIRED DATA.)

The three-line format data display's LOC and I column headings have the same meanings as those described previously in the One-Line Data Display Format subsection.

The format for a word of data on a 16-bit cycle (BHEN(L)=0) is as follows:

```
lll  ccc                          i
   ADDR=bbbbbbbbbbbbbbbbbbb
   DATA=bbbbbbbbbbbbbbbb
```

On an eight-bit cycle (when BHEN(L)=1) the format is:

```
lll  ccc                          i
   ADDR=bbbbbbbbbbbbbbbbbbb
   UDC=bbbbbbbb  DATA=bbbbbbbb
```

The fields "lll," "ccc," and "i" represent memory location, cycle type, and interrupt priority, respectively. These fields have the same functions as described previously for the one-line format data display. Each b above represents one binary digit. If binary radix is not selected for one of the fields, that field will be shorter.

FORMAT MODE

The PM 112 personalizes elements of the 7D02's FORMAT mode display. These elements appear when choosing non-default radices for fields in the word recognizer and data display, and also when inverting buses (making active low lines appear active high and vice versa).

Press the Format key on the 7D02 front panel to enter or exit the the Format mode.

Note that when a signal labeled with a slash is inverted in the FORMAT mode, the appearance of the signal's label will not change on any of the displays.

MANUAL CLOCK SWITCH

The PM 112 has a push-button manual clock switch. This switch is located on the circuit board corner next to the 64-conductor ribbon cable.

The manual clock switch generates an acquisition strobe for the 7D02, in place of a strobe generated by the default PM 112 clock. (The default clock is derived from the falling edge of XACK(L) ORed with the rising edge of BUSY(L) -- for details refer to Theory of Operation.) The manual clock signal is asynchronous, and will give a snapshot of whatever is on the bus during the acquisition strobe. Each snapshot is stored as a data word (bus cycle) by the 7D02.

You might want to use the manual clock for instance, when the 7D02 is running, does not trigger, and displays the message NO CLOCK in the upper left corner of the display screen. XACK(L) and/or BUSY(L) may be stuck high or low, or not present at all (bus inactive).

To use the manual clock, follow these directions:

1. Obtain the 7D02 program shown in Figure 2-2 by turning the 7D02 mainframe power off for five seconds, back on, and then push the TRIGGER button. This program, with all field values in the default condition, will allow the 7D02 to trigger regardless of the state of the bus.

2. Push the 7D02's START/STOP button.

3. Push the manual clock switch. The message SLOW CLOCK will take the place of NO CLOCK on the screen dislay. Push the switch at least two more times.

4. Push the START/STOP button to display the acquired data.

PARALLEL AND SERIAL BUS PRIORITY RESOLUTION

The PM 112 has a three-pin jumper to accommodate both parallel and serial bus priority resolution schemes. This jumper, labeled SER PAR, is shown in Figure 2-6. If your SUT uses parallel priority resolution, place this jumper strap in the PAR position. For SUTs using serial priority resolution systems, place the strap in the SER position.

USING UDC LINES

The user-defined control lines allow a variety of Multibus signals to be monitored and to be used for word recognition. The signals are selected with the use of jumper straps (included with the PM 112) and/or jumper wires. (Jumper wires with grabber tips are recommended, and are available from Tektronix as an optional accessory. Refer to the Introduction section for their part number.) The PM 112 data lines 15-8 effectively become UDC lines 7-0 whenever the SUT performs 8-bit operations (as indicated by BHEN(L)=1).

WARNING

Switch off power to both the logic analyzer and the SUT before moving jumper straps, attaching jumper wires, or inserting/removing the PM 112. Voltages present within the SUT may be lethal. Damage to the SUT, the PM 112, and the logic analyzer may result if work is performed with power on.

Monitoring UDC Lines on All Cycles

The PM 112 perceives an 8-bit operation as occurring whenever BHEN(L)=1. To force BHEN(L)=1 on all cycles, as seen by the PM 112, move the strap on jumper W3011, labeled 8/16 8, to the 8 position. Moving this jumper strap has no effect on operation of the SUT, but it does prevent the logic analyzer from monitoring the upper eight bits of the data bus. The most significant 8 bits in the word recognizer DATA field will now specify UDC recognition values at all times. The 8/16 8 jumper is located with the other UDC jumpers, as shown in Figure 2-6.

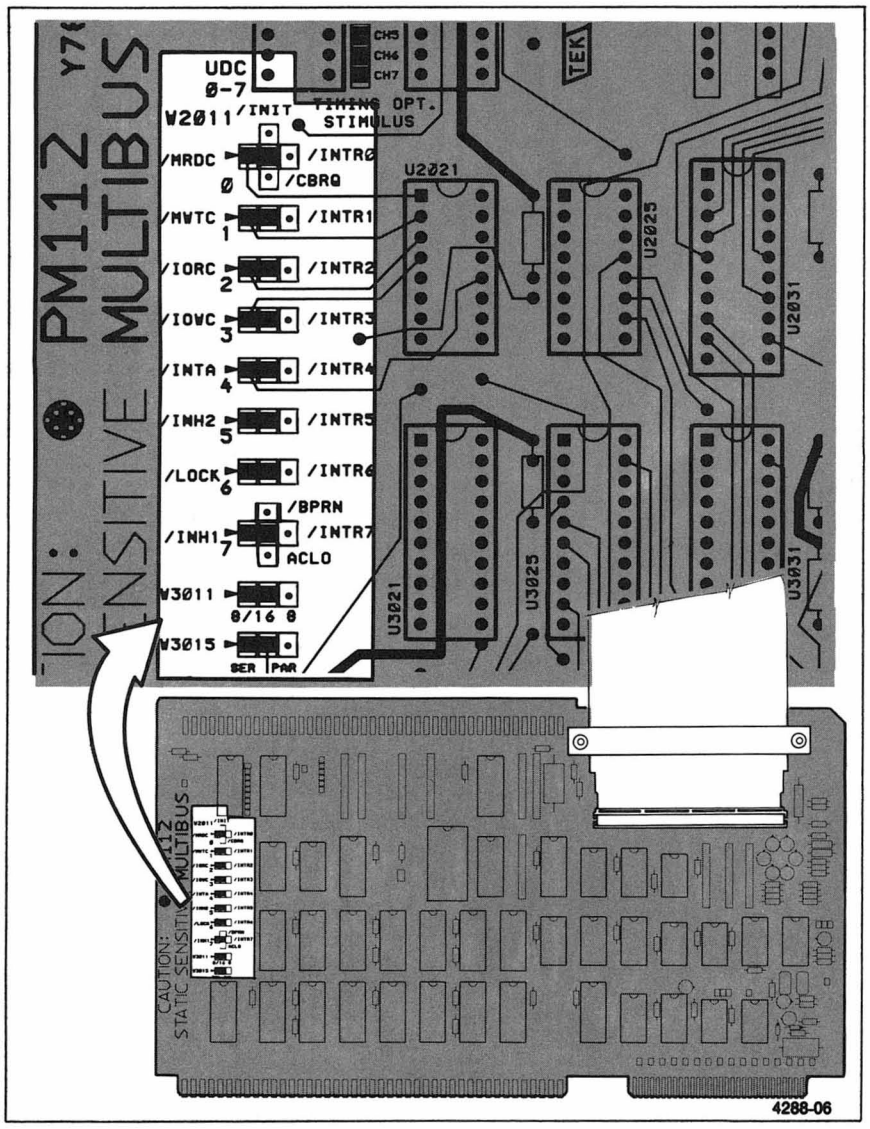


Figure 2-6. UDC jumper pins and straps. The large numeral next to each jumper indicates the UDC line number. Signals accessible by jumper strap are labeled next to the required strap position. In this illustration the straps are shown in their default positions. Jumpers for UDC7 and UDC0 have four possible strap positions; UDC6-1 have two possible positions. The 8 8/16 jumper (near bottom of row) allows UDC lines to be monitored on both 8 and 16-bit cycles when in the 8 position.

Note the SER PAR jumper at bottom of the row; place the jumper strap in the SER position if your SUT uses serial bus priority resolution, or in the PAR position if parallel priority resolution is used.

Default UDC Line Assignments

Each UDC line is assigned to its default signal when its jumper strap is placed on the leftmost pair of pins, also indicated by tick marks, as shown in Figure 2-5. Table 2-2 is a listing of signals that can be accessed by jumper strap at each UDC jumper.

NOTE

Jumper straps must be in default positions, indicated by tick marks, for the PM 112 to pass self-test.

Optional UDC Line Assignments

By moving the UDC jumper straps to positions other than default, or by removing jumper straps and using jumper wires (connected to the center pins of UDC jumpers) several other Multibus signal lines can be accessed.

Jumper Strap Selected Signals. Each UDC line has either three pins in a row (UDC lines 6-1), or five pins arranged in a cross (UDC7 and UDC0). The three-pin arrangement has two possible jumper strap positions, and the five-pin arrangement has four. Signal names are labeled on the circuit board next to the UDC jumper strap position required, as shown in Figure 2-6. Table 2-2 is a listing of signals that can be accessed by jumper strap at each UDC jumper.

Table 2-2
DEFAULT AND OPTIONAL UDC JUMPER STRAP POSITIONS

UDC Line	Default	Optional
UDC0	MRDC(L)	INTR0(L), CBRQ(L), INIT(L)
UDC1	MWTC(L)	INTR1(L)
UDC2	IORC(L)	INTR2(L)
UDC3	IOWC(L)	INTR3(L)
UDC4	INTA(L)	INTR4(L)
UDC5	INH2(L)	INTR5(L)
UDC6	LOCK(L)*	INTR6(L)
UDC7	INH1(L)	INTR7(L), ACLO(H), BPRN(L)

*AACK(L) in early bus specification versions.

Jumper Wire Selected Signals. The PM 112 provides test point pins for several Multibus signals that can be connected to the UDC jumpers by jumper wires. These test point pins are shown in Figure 2-7. You can also connect UDC lines to TTL level signals in the SUT.

NOTE

At the UDC jumpers, any signals selected by jumper wires have an extra delay of approximately 2 ns. This is subtracted from hold time and added to setup time.

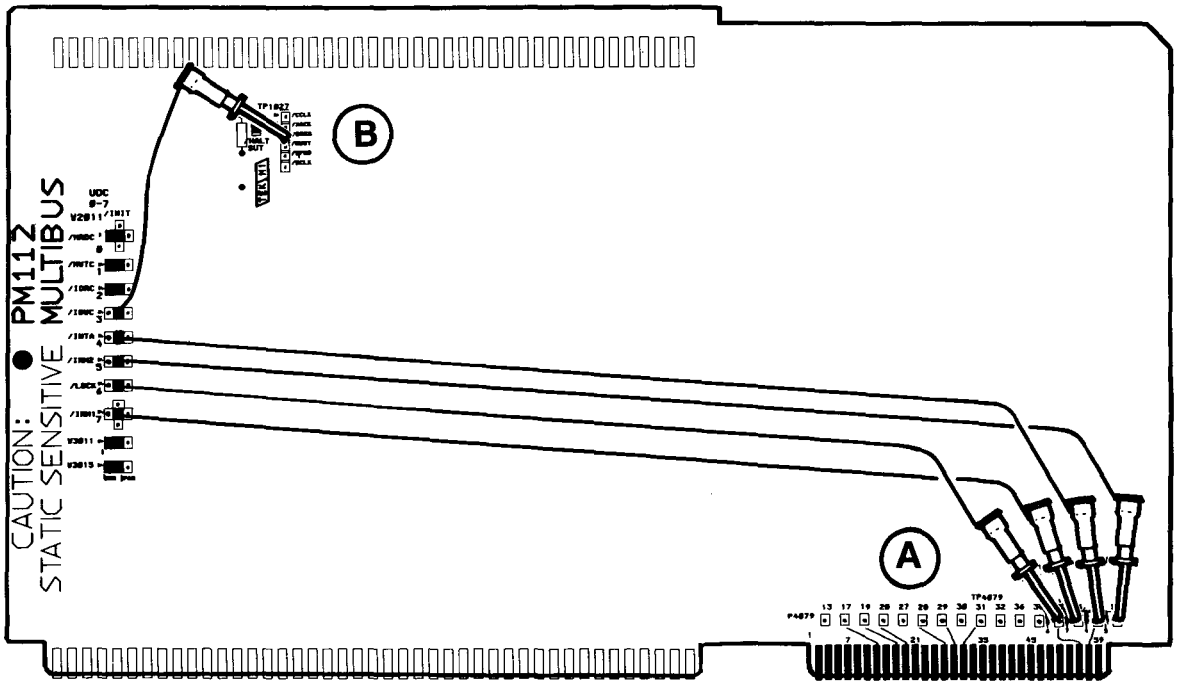


Figure 2-7. Test points accessible by UDC jumper wires. This illustration shows (A) jumper wires connecting the most significant four Multibus address lines (ADR14(L)-ADR17(L)(HEX) of a 24-bit address system), found at Test Point 4079, to UDC lines 4, 5, 6, and 7, and (B) a jumper wire connecting BREQ(L), found at Test Point 1027, to UDC3. Table 2-3 provides a listing of the signals that can be selected by UDC jumper wires.

To connect a signal to a UDC line, remove the jumper strap on the desired UDC line's jumper and connect a jumper wire to the center pin, as shown in Figure 2-6. Connect the other end of the lead to the selected signal's test point pin (or to a convenient connection point for a TTL signal that is within the SUT).

The PM 112 provides test point pins for the signals listed in Table 2-3.

Table 2-3
SIGNALS ACCESSIBLE BY UDC JUMPER WIRES

Test Point Pin	Signal
TP1027-1	CCLK(L)
" "-2	XACK(L)
-3	BREQ(L)
" "-4	BUSY(L)
-5	BPRO(L)
" "-6	BCLK(L)
TP4079-13	PFSR(L)*
" "-17	PFSN(L)*
-19	PFIN(L)*
" "-20	MPRO(L)*
-27	PAR1(L)*
" "-28	HALT(L)*
-29	PAR2(L)*
" "-30	WAIT(L)*
-31	PLC(H)*
" "-32	ALE(H)*
-36	BD RESET(L)*
" "-38	AUX RESET(L)*
TP4079-55	ADR16(L)*
" "-56	ADR17(L)*
-57	ADR14(L)*
" "-58	ADR15(L)*

*Consult SUT documentation -- these signals carried on Multibus P2 connector with same pin number. May be reserved and/or not bussed on some bus versions.

PM 112 SPECIFICATIONS

Overview

This section of the manual provides specifications tables of the following categories:

TABLE	TABLE NUMBER
GENERAL CHARACTERISTICS	3-1
CONTROL LINE USAGE	3-2
ELECTRICAL	3-3
MECHANICAL	3-4
ENVIRONMENTAL	3-5
LOGIC ANALYZER CABLE	3-6

Listings in Performance Requirements columns are specifications of the instrument that may be verified. If verification of these listed specifications is required for customer incoming inspection or other purposes, procedures and test equipment are described in the Performance Check section of this manual.

Listings in Supplemental Information columns are either explanatory notes or performance characteristics for which no limits are specified. They are not tested in the Performance Check section of this manual.

Safety Certification

The PM 112 complies with the requirements of U.L. 1244, IEC 348, and CSA 556B.

Table 3-1
PM 112 GENERAL CHARACTERISTICS

CHARACTERISTIC	DESCRIPTION
Channels Stored and Displayed	
Max. Number of Channels	44
Address Lines	20 ADR0(L)-ADR13(L)(HEX) 24 (using user-defined control lines)
Data Lines 7-0	8 DAT0(L)-DAT7(L)(HEX)
Data Lines 15-8, UDC Lines 7-0	8 DAT8(L)-DATF(L)(HEX) When the upper 8 bits of the data bus are not used, the lines are stored as UDC7-UDC0 (user-defined control).
Interrupt Priority	3 INT0(L)-INT7(L) (encoded on A22-A20)
Interrupt Request	1 INTR(L) (carried on A23)
Command Lines	4 MWTC(L), MRDC(L), IOWC(L), IORC(L), INTA(L), BUSY(H) (encoded onto C2-C0) BHEN(L) (carried on C3)

Table 3-2
PM 112 CONTROL LINE USAGE

SIGNAL	CONTROL LINE	STORED	WORD RECOGNIZER	CLOCK QUALIFIER
MWTC(L), MRDC(L), IOWC(L), IORC(L), INTA(L), BUSY(H) — encoded onto	C2-C0	X	X	X
BHEN(L)	C3	X	X	X
INH1(L)	C4		X	X
INH2(L)	C5		X	X
CBRQ(L)	C6			X
LOCK(L)	C7			X
ACLO(H)	C8			X
BUSY(H)	C9			X

Table 3-3
ELECTRICAL SPECIFICATIONS

CHARACTERISTIC	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
PM 112 SPECIFICATIONS		
All Signal Inputs		TTL Compatible
V_{iH}	2.0 V min	
V_{iL}	0.6 V max	
V_{max}		5.5 V
V_{min}		-0.5 V
I_{iH} max		20 uA @ 2.7 V
I_{iL} max		200 uA @ 0.4 V
I_{in} @ V max		100 uA
Hysteresis		0.2 V min
Threshold		+1.4 V nominal
Minimum Signal Pulse Widths		50 ns
Input Capacitance		35 pF typical, 60 pF max

Table 3-3 (cont.)
ELECTRICAL SPECIFICATIONS

CHARACTERISTIC	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
SYSTEM SPECIFICATIONS (with 7D02)		
Clock		
Clock Propagation Delay XACK(L) to CLK (at 7D02)		50 ns min 63 ns max
Clock Period	200 ns min.	
Clock Pulse Width	50 ns min.	
Setup and Hold Measurements made with respect to the falling edge of XACK(L), except as denoted by "*" - measured with respect to the rising edge of BUSY(L).		
Data Lines		
Setup Time	0 ns	
Hold Time	35 ns	
Address Lines		
Setup Time		-5 ns
Hold Time		55 ns
UDC Lines		
Setup Time		-5 ns
Hold Time		55 ns (at the UDC jumpers, a signal selected using jumper straps or jumper wires has approximately 2 ns delay. This is subtracted from hold time and added to setup time.)

Table 3-3 (cont.)
ELECTRICAL SPECIFICATIONS

CHARACTERISTIC	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Commands (MRDC(L), MWTC(L), IORC(L), IOWC(L) and INTA(L))		
Setup Time	0 ns	
Hold Time	35 ns	30 ns typical
Interrupt Lines (INT0-INT7)		
Setup Time		50 ns
Hold Time		45 ns
INH1(L) and INH2(L) (as Word Recognizer inputs)		
Setup Time		10 ns
Hold Time		50 ns
BHEN(L)		
Setup Time		-5 ns
Hold Time		55 ns
Clock Qualification INH1(L), INH2(L), LOCK(L), ACLO(H)		
Setup Time		30 ns
Hold Time		35 ns
CBRQ(L)		
Setup Time		25 ns*
Hold Time		35 ns*
Timing Option		
Setup Time	-5 ns	-5 ns*
Hold Time	50 ns	65 ns*

*Measured with respect to the rising edge of BUSY(L)

Table 3-3 (cont.)
ELECTRICAL SPECIFICATIONS

CHARACTERISTIC	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
HALT SUT(L)		
Delay		Two qualified State Clocks plus 58 ns max. after 7D02 completes data acquisition
Output Drive		
V_{oL}		0.5 V @ -5 mA max
V_{oH}		2.4 V @ 0.5 mA max
Self-Test Clock Accuracy	20 MHz $\pm$ 5%	
P1 Extender Run Current Limits		
+5 V MB (pins 3, 4, 5, 6)		7.5 A max
+12 V MB (pins 7, 8)		4.3 A max
Reserved (pins 9,10)		4.3 A max
Reserved (pins 77, 78)		4.3 A max
-12 V MB (pins 79,80)		4.3 A max
+5 V MB (pins 81, 82, 83, 84)		7.5 A max
Power Dissipation		3.3 W max. (without self-test)

Table 3-4
MECHANICAL SPECIFICATIONS

CHARACTERISTIC	DESCRIPTION
Size	12" by 6.75" 30.5 cm by 17.15 cm (conforms to Intel Multibus and IEEE P796 specifications)
Weight	1 lb. 9 oz. .71 kg
Cable Length (logic analyzer to personality module)	4 ft. $\pm$ 1.0 ft. 122 cm $\pm$ 2.5 cm

Table 3-5
ENVIRONMENTAL SPECIFICATIONS

CHARACTERISTIC	DESCRIPTION
Temperature	
Operating	-15°C to +55°C
Non-operating	-62°C to +85°C
Relative Humidity	95 to 97% non-condensing
Altitude	
Operating	15,000 ft. (4.5 km)
Non-operating	50,000 ft. (15 km)

Table 3-6
LOGIC ANALYZER CABLE SPECIFICATIONS

PM 112 J1075 PIN	SIGNAL	DESCRIPTION
1	GROUND	GROUND
2	CLK	Differential ECL level; high=-0.8 V, low=-1.7 V
3	CLK(L)	Differentially terminated into 124 ohms; ECL level
4	GND	GROUND
5	AI0	*
6	AI1	*
7	AI2	*
8	AI3	*
9	AI4	*
10	AI5	*
11	AI6	*
12	AI7	*
13	AI8	*
14	AI9	*
15	AI10	*
16	AI11	*
17	AI12	*
18	AI13	*
19	AI14	*
20	AI15	*
21	AI16	*
22	AI17	*
23	AI18	*
24	AI19	*
25	AI20 (IPR)	*
26	AI21 (IPR)	*
27	AI22 (IPR)	*
28	AI23 (INTR)	*
29	DI0	*
30	DI1	*
31	DI2	*
32	DI3	*
33	DI4	*
34	DI5	*
35	DI6	*
36	DI7	*

*STTL output back terminated into 68 ohms.

Table 3-6 (cont.)
LOGIC ANALYZER CABLE SPECIFICATIONS

PM 112 J1075 PIN	SIGNAL	DESCRIPTION
37	DI8, UDC0	*
38	DI9, UDC1	*
39	DI10, UDC2	*
40	DI11, UDC3	*
41	DI12, UDC4	*
42	DI13, UDC5	*
43	DI14, UDC6	*
44	DI15, UDC7	*
45	+5 V	+5 V supply
	Commands encoded;	
46	INTA(L), BUSY(H),	CI0, *
47	MRDC(L), MWTC(L),	CI1, *
48	IORC(L), IOWC(L)	CI2, *
49	BHEN(L)	CI3, *
50	INH1(L)	CI4, *
51	INH2(L)	CI5, *
52	CBRQ(L)	CI6, *
53	LOCK(L)	CI7, *
54	ACLO(H)	CI8, *
55	BUSY(H)	CI9, *
56	+5 V	+5 V supply
57	+5 V	+5 V supply
58	+15 V	+15 V supply
59	-15 V	-15 V supply
60	GND	GROUND
61	HALT SUT(L)	1/2 LSTTL input load
62	LOOK(H)	3 LSTTL input loads
63	SELP(L)	3 LSTTL input loads
64	GND	GROUND

*STTL output back terminated into 68 ohms.

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

SERVICE SAFETY SUMMARY

For Qualified Service Personnel Only

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or to other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Grounding the Product

This product is grounded through the grounding conductor of the logic analyzer power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective ground connection, all accessible conductive parts can render an electric shock.

Do Not Operate Without Shield

To avoid instrument damage, do not operate this product without its insulating shield installed.

Disconnect Power Before Servicing

Disconnect power before removing insulating shield, soldering, or replacing components.

Conductive Jewelry

Do not wear conductive jewelry while servicing the PM 112.

SECTION 4
THEORY OF OPERATION

OVERVIEW

The primary function of a personality module is to collect data from a system under test (SUT) and transfer this data to the logic analyzer in a format that the analyzer and the user can easily interpret.

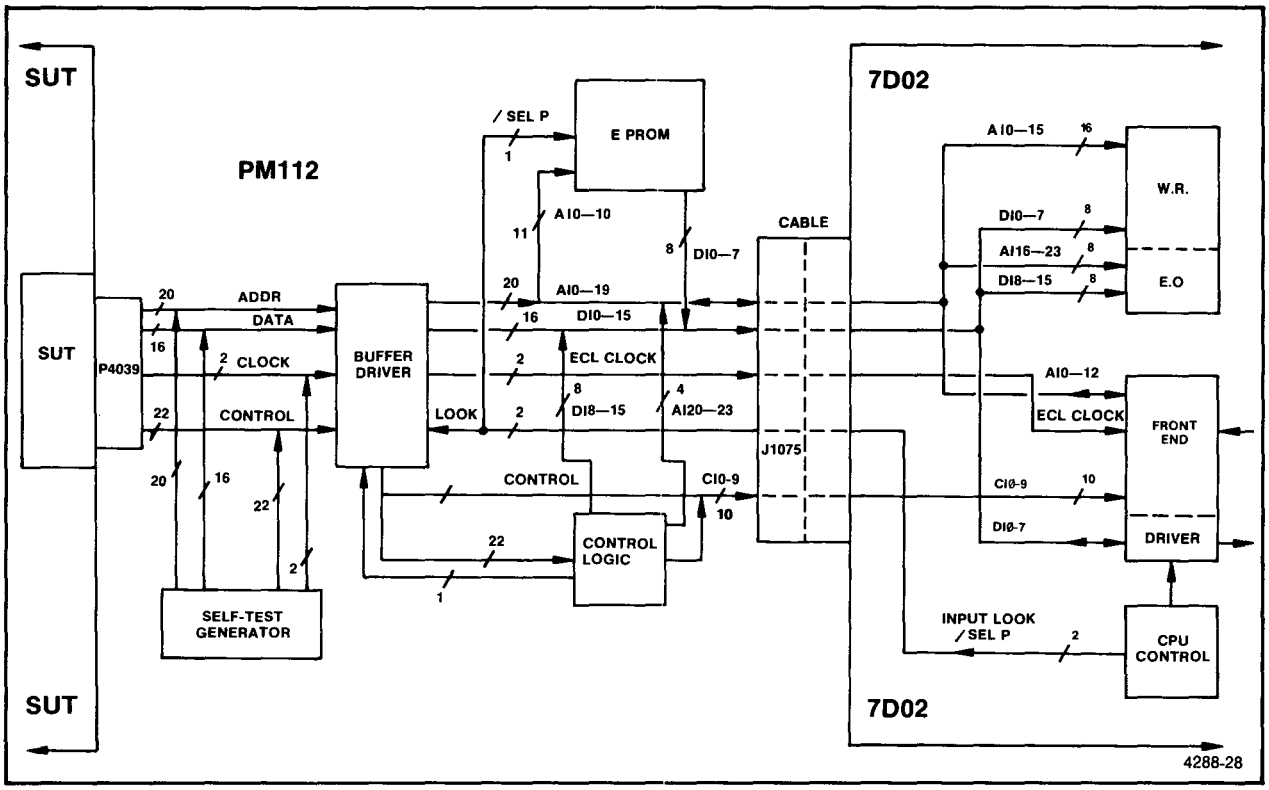


Figure 4-1. Block diagram of Multibus-SUT/PM 112/7D02 system.

The PM 112 Personality Module performs its function in the following ways:

- The PM 112 connects the logic analyzer to a Multibus SUT. It plugs into the SUT's card-cage in the same manner as any other Multibus-compatible circuit board (or acts as a P1 extender if all the backplane's slots are in use). Unlike other PM 100 Series personality modules, the PM 112 does not directly monitor a microprocessor in the system under test. Instead, it gives the logic analyzer access to all address,

data, command, status, and clock lines carried on the SUT bus.

- Circuitry in the PM 112 works together with logic analyzer circuitry to generate the state clock. The state clock strobes information from the PM 112 into the logic analyzer's acquisition memory.

- The PM 112 transfers data from the SUT to the logic analyzer in a standard format. The PM 112 also contains firmware that allows the logic analyzer to disassemble the states of the Multibus command lines into descriptive command mnemonics.

- Because the Multibus is a general-purpose bus specification that may be used with a variety of microprocessors, the PM 112 does not disassemble data into the opcode mnemonics of a particular microprocessor.

- In the self-test mode, the PM 112 self-test circuitry generates a predefined set of simulated Multibus signals. These signals are fed into the PM 112 acquisition circuitry and may be used to test both the PM 112 and the logic analyzer.

SIGNAL-NAMING CONVENTIONS

- In the text an (H) or (L) following a signal name indicates that the signal is asserted in the high or in the low electrical state.

- On the circuit diagrams and block diagram, a bar ($\overline{\ }$) over a signal name or portion of a signal name indicates that the signal is asserted in the low electrical state.

  The PM 112 shares many of the logic analyzer's line names. Therefore the absence of a bar over a PM 112 line name does not necessarily mean the signal carried is asserted in the high electrical state.

- On the 7D02's display screen and in this manual's simulated screen displays, a slash (/) preceding a field name or portion of a field name indicates that a 0 placed in this field specifies the active low condition. For example, placing a 0 in the word recognizer R/W field specifies that a Write operation is the active low condition. (Note that it is possible to invert the active condition for a field by entering Format mode and specifying bus inversion. Doing this will not change the appearance of the field's name on the display.)

- Slashes (/) are also used to denote an active low signal on circuit board mnemonic labels, and are used in the text when referring to board labels.

GENERAL INFORMATION

- All buffers are of hysteresis type, minimizing susceptibility to noise on the SUT bus lines.
- The PM 112's P4039 connector is equivalent to the Multibus P1 connector.
- The PM 112's P4079 connector is equivalent to the Multibus P2 connector.

DETAILED CIRCUIT DESCRIPTION

ACQUISITION CIRCUITRY ◇1

Command and Miscellaneous Buffers

Various Multibus signals are buffered by U4021 and U4025A. Some signals are output to the UDC jumpers (W2011-7 through W2011-0), others are carried on control lines to the 7D02, and still others are input to the command encoder.

Command Encoder

The command encoder encodes the four Multibus commands (MRDC(L), MWTC(L), IORC(L), and IOWC(L)), and the INTA(L) and BUSY(H) signals into codes representing the six valid Multibus cycle types: Memory Read, Memory Write, I/O Read, I/O Write, Interrupt Acknowledge, and Bus Available (BUSY(L) not asserted). Because the six signals are mutually exclusive, they can be encoded onto only 3 lines. Codes are carried to the logic analyzer on lines CI2-CI0.

Interrupt Encoder and Buffers

The seven Multibus Interrupt lines, INTR0(L)-INTR7(L), are buffered by U4031 and then priority encoded by U2025. The code output by U2025 identifies the highest priority interrupt line currently asserted. However, U2025 cannot distinguish between 1) only the lowest priority input, INTR7(L), asserted and 2) no interrupts asserted. The enable output (EO) of U2025 is high whenever at least one input is low (asserted), and indicates that at least one interrupt is active. The EO signal is inverted by U2031G and carried to the 7D02 on AI23. The three outputs of U2025 are buffered by U3021, and then carried on AI22-AI20 to the 7D02.

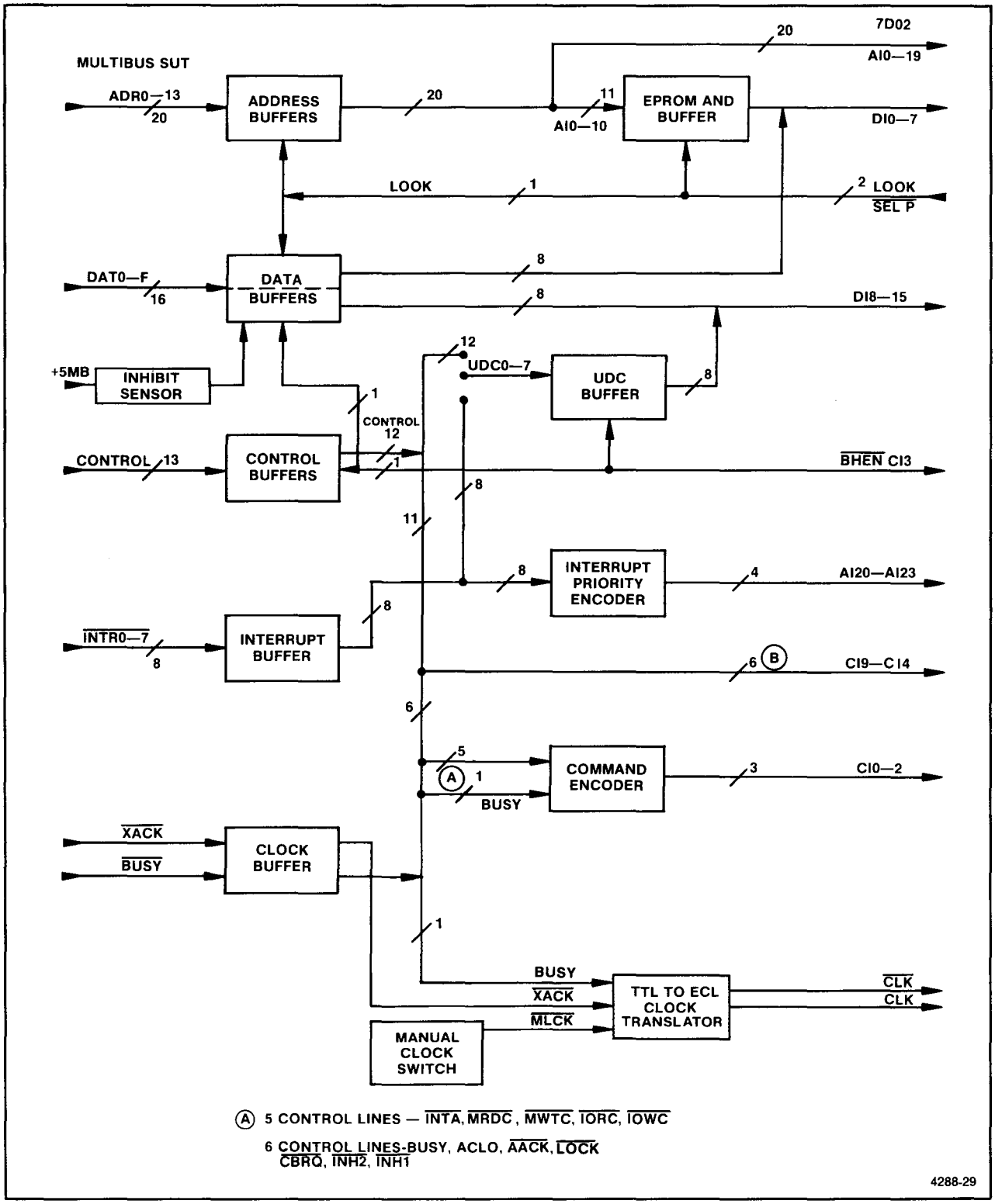


Figure 4-2. Block diagram of PM 112 acquisition circuitry.

HALT SUT(L) Buffer

The 7D02 HALT PUT(L) signal (equal to PM 112 HALT SUT(L)) is buffered by U1015E and terminates at TP1025. This signal can be connected by the user, if desired, to an appropriate line in the SUT. HALT SUT(L) will go low when data acquisition is completed by the 7D02, if specified by the user in the 7D02 trigger display.

UDC Jumpers and Buffer

The user-defined control (UDC) lines can access a variety of lines from the Multibus SUT; 20 different signals are available (8 simultaneously) using jumper straps on UDC jumpers W2011-7 through W2011-0. The user can access still other signals with jumper wires attached to the UDC jumpers' middle pins. UDC signals are inverted and buffered by U1021. The Multibus signal BHEN(L) is inverted by U2031A and enables U1021. (U1021 is enabled during 8-bit SUT cycles, or whenever the user places jumper W3011 in the "8" position.) UDC signals are then carried to the logic analyzer on DI15-DI8. (On the 7D02's display screen, the UDC signals are reinverted to appear active in the same state as the original SUT signal appeared.)

Clock Generation

The PM 112 derives its clock signal (CLK) from the Multibus signals XACK(L) and BUSY(L), or from the PM 112 signal MCLK(L). The falling edge of XACK(L) is logically ORed with the rising edge of of BUSY(L). The resulting output is XORed with MCLK(L) (the manual clock switch's output). Implementation of these functions is discussed under the following Manual Clock Switch and TTL-to-ECL Clock Translator headings. Figure 4-5 shows the timing relationships between XACK(L), BUSY(L), and MCLK(L). Figures 4-3 and 4-4 show the timing relationship of Multibus data read and write commands, respectively, to XACK(L).

Manual Clock Switch

The manual clock switch provides an asynchronous clock to the 7D02. For each push of the button, the result is acquisition of a snapshot of the SUT's bus. Gates U4079B and C are cross-coupled, forming a debouncing latch for the switch's output (MCLK(L)). Minimum pulse duration is approximately 50 ns.

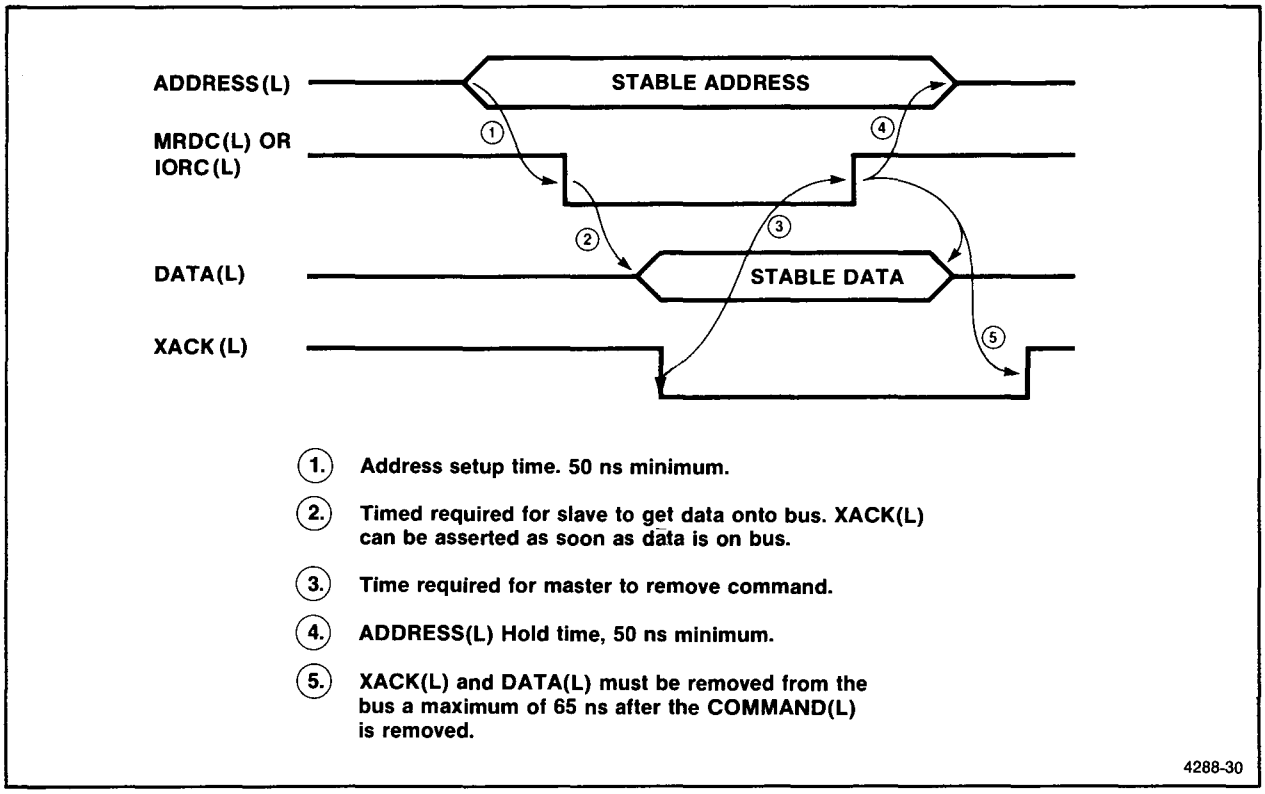


Figure 4-3. Multibus SUT memory and I/O read timing. This diagram shows how XACK(L), the Multibus Transfer Acknowledge signal, relates to Multibus read timing. The PM 112 uses XACK(L) for clock generation.

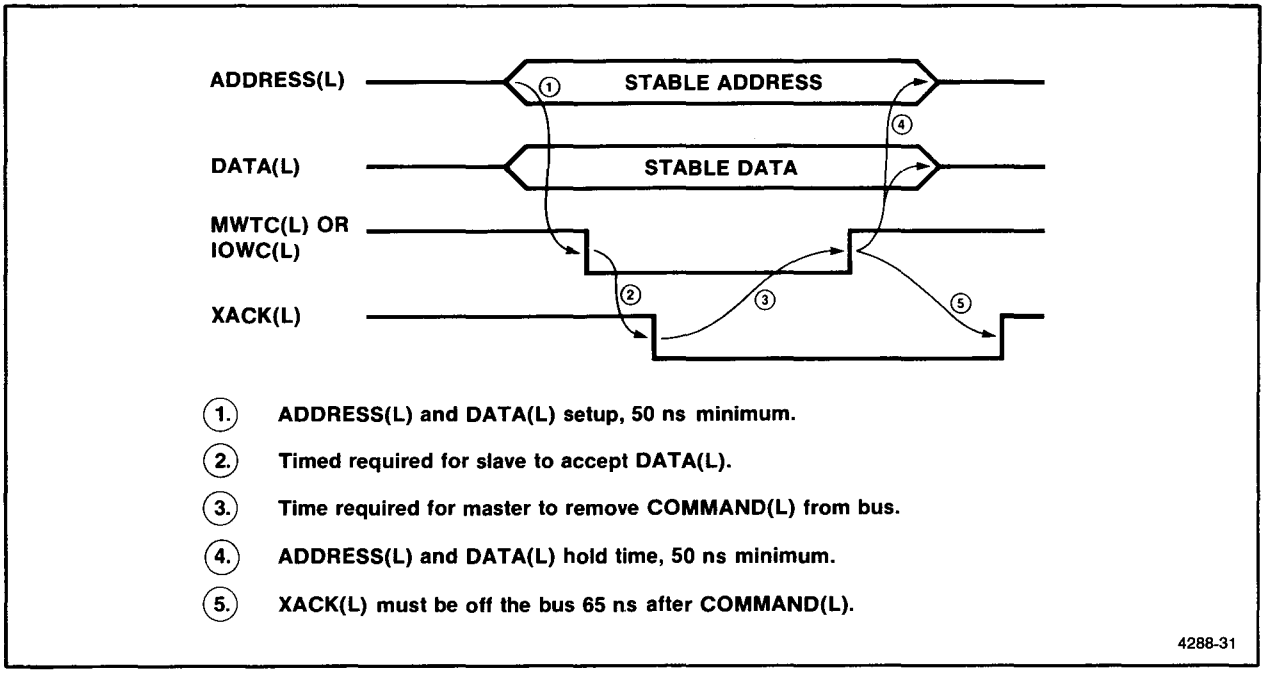


Figure 4-4. Multibus SUT memory and I/O write timing.

TTL-to-ECL Clock Translator

The TTL-to-ECL clock translator serves three functions:

1. to delay the signals used for clock generation, in order to optimize setup and hold relationships between the CLK signal and data;

2. to form a signal from XACK(L) logically ORed with BUSY(H), then to logically XOR this signal with the manual clock switch debouncer output, MCLK(L); and

3. to generate differential ECL clock signals (CLK(L) and CLK(H)) for the 7D02 from three TTL inputs (XACK(L), BUSY(H), and MCLK(L)). The clock signals cause data acquired by the PM 112 to be strobed into the 7D02.

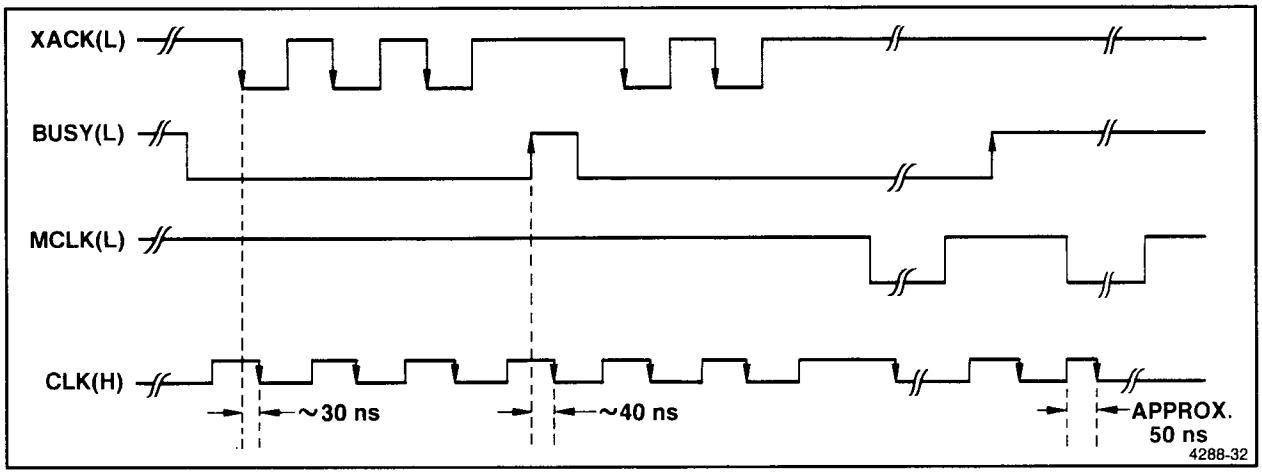


Figure 4-5. PM 112 Clock Generation.

DL3081 performs the first function, delaying XACK(L) and BUSY(H) by 30 ns.

The second two functions are implemented as follows. Q2086 and R1083 form a 19 mA current source, which feeds the differential comparator. Q2083 is the inverting side of the comparator. R2082 and R2081 serve as a voltage divider, and provide the comparator with a 2.11 V reference voltage.

The remaining transistors execute the logic function. Q2084 is normally on and Q2085 is normally off. When Q2081 and/or Q2087 are turned on by XACK(L) or BUSY(H), the comparator switches, and the CLK(H) signal goes from high to low.

When the manual clock switch is pushed, Q2084 turns off, and 50 ns later Q2085 turns on. This produces a minimum 50 ns clock pulse, as shown in Figure 4-5. The clock pulse occurs regardless of the states of XACK(L) and BUSY(L), because they have in effect been disconnected by Q2084 and bypassed by Q2085.

68 Ohm Termination

The 68 ohm back-termination resistors improve transmission line characteristics of signals carried on the logic analyzer cable.

ACQUISITION CIRCUITRY ◇2

Inhibit Sensor

The inhibit sensor disables the data buffers when it senses Multibus power (+5MB) and self-test power (+5T) simultaneously. This situation can only occur when the PM 112 is configured in the self-test mode and plugged into an SUT. The result of the inhibition is that all zeroes appear in the acquisition memory display's DATA field. This should alert the user that the PM 112 is configured in the self-test mode, and that jumper W3085 should be moved to the NORM, rather than the TEST, position.

Data Buffers

Multibus SUT Data (DAT0(L)-DATF(L)) enters the PM 112 at P4039, and is double-buffered to optimize the setup and hold timing relationship between the SUT and the 7D02. When BHEN(L) goes high, buffer U1045 is disabled. This allows UDC signals to be carried on the upper eight data lines, DI16-DI8, during 8-bit SUT bus cycles or whenever the user forces BHEN(L) to appear high by using jumper W3011. The 7D02 LOOK(H) signal tri-states buffer U2055 when data acquisition is completed, allowing the EPROM to use DI7-DI0 for output to the 7D02.

Address Buffers

Multibus SUT address information (ADR0(L)-ADR13(L), hexadecimal) enters the PM 112 at P4039; is buffered by U4041, U4035, and U3021B; and is then carried to the 7D02 on AI19-AI0. (Note that AI23-AI20 are used only to carry interrupt request information.) The 7D02 LOOK(H) signal tri-states buffers U4041 and U4035 when data acquisition is completed. This allows the 7D02 to use AI10-AI0 (bidirectional) for addressing the EPROM.

EPROM and Buffer

When the 7D02 has completed data acquisition, it pulls the LOOK(H) line high, which tri-states selected data and address buffers (as described previously). This allows use of AI10-AI0 and DI7-DI0 to access the EPROM (U2041). After a short delay, the 7D02 signal SELP(L) enables the EPROM and buffer U2045, allowing information to flow to the logic analyzer. The timing of these events is diagrammed in Figure 4-6.

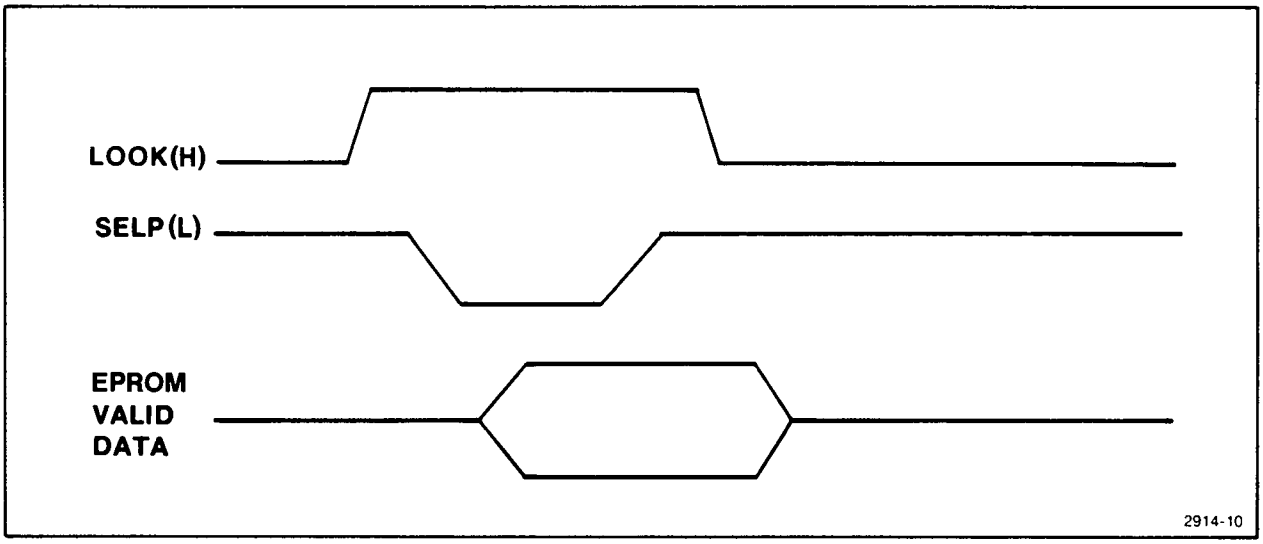


Figure 4-6. LOOK(H), SELP(L), and EPROM Data timing relationships. This diagram shows the timing relationship of the 7D02's LOOK(H) and SELP(L) signals to acquisition of data stored within the PM 112's EPROM.

68 Ohm Termination

The 68 ohm back-termination resistors improve transmission line characteristics of signals carried on the logic analyzer cable.

SELF-TEST GENERATOR (3)

The self-test generator provides a set of simulated Multibus signals to the PM 112's acquisition circuitry. They compose a predefined pattern of 16 simulated bus cycles, representing variations on all of the major Multibus cycle types. Figure 4-10 shows timing relationships of the signals in the self-test pattern. Figure 5-3, in the Performance Checks section of this manual, shows this pattern as acquired by the PM 112/7D02. The self-test generator's data and command signals meet the worst-case system timing specifications. Working in concert with the self-test and acquisition circuitry, the 7D02 firmware diagnostics provide a high degree of confidence that the PM 112 hardware is functioning properly.

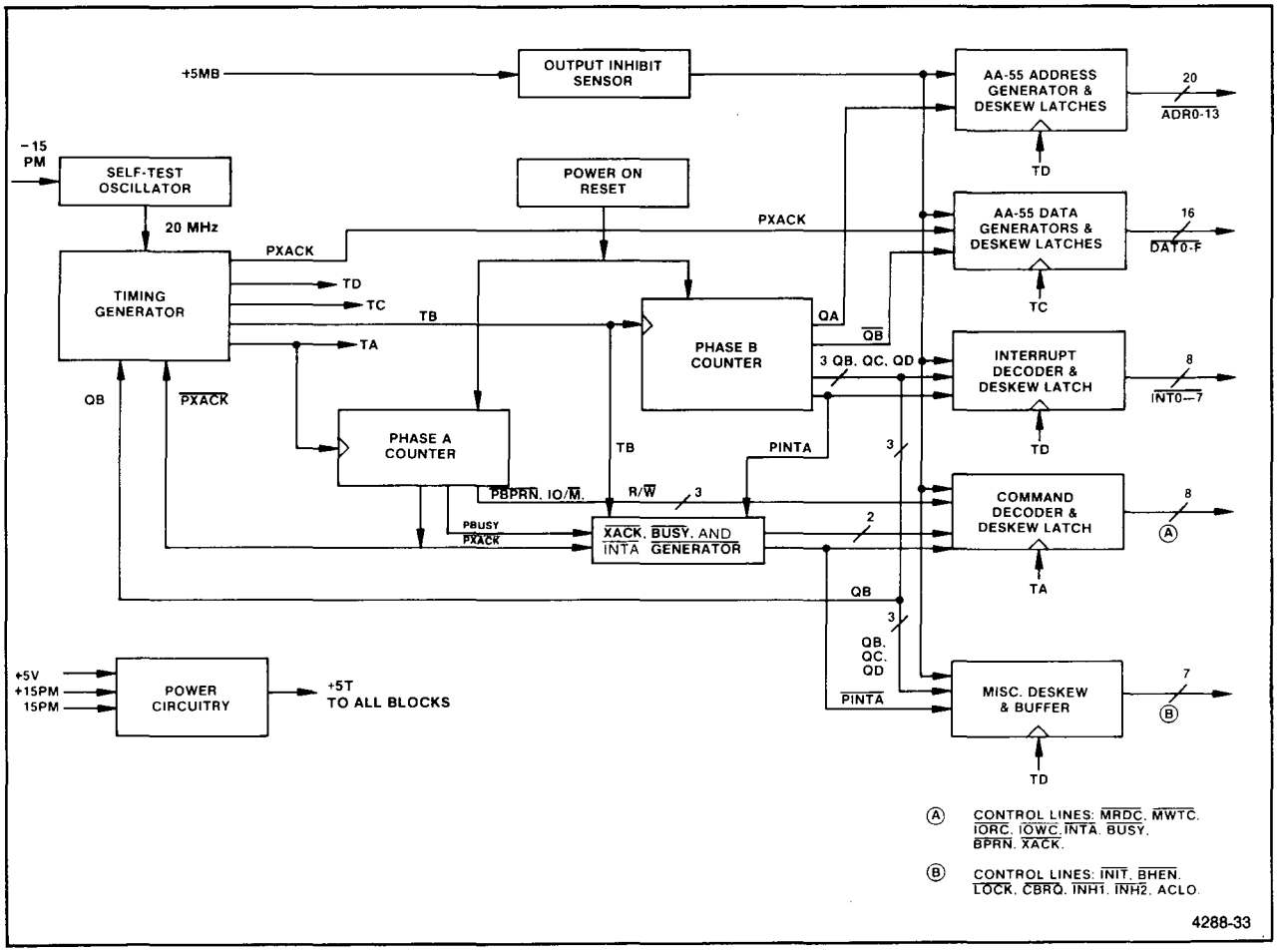


Figure 4-7. Block diagram of PM 112 self-test generator.

Self-Test Oscillator

The +5T voltage source powers a discrete LC oscillator, providing a 20 MHz output (TCLK(H)). The -15PM voltage source

provides biasing for the oscillator. The oscillator's output is pulse-shaped by a hysteresis Schmitt-trigger gate (U4079D) to generate a square wave. The self-test oscillator signal may also be provided by an external TTL level clock. This is accomplished by moving jumper W4075 from the INT to the EXT position, and connecting the external TTL clock's output to TP4075.

Power-On Reset

The power-on reset circuitry insures that the outputs of phase counters A and B (U4071 and U2065, respectively) are held low until after the self-test oscillator is up and running. This delay is accomplished by charging C4089 up to the threshold of inverting gate U4079A. When U4079's output goes low, Q4071 shuts off and the phase counters' CLR inputs are released. The sequence takes place independently of the self-test oscillator, and requires approximately 110 ns from the time the +5T voltage source is first powered.

Power Circuitry

The power circuitry is comprised of W3085 (NORM/TEST jumper), which enables power to the self-test circuitry when in the TEST position; an LED (DS2037) that indicates power from the 7D02 (in both the NORM and TEST modes); and decoupling capacitors to reduce noise on power lines.

Output Inhibit Sensor

The output inhibit sensor tri-states all outputs of the self-test generator when it senses Multibus power (+5MB). This eliminates possible contention with signals from the Multibus SUT.

Timing Generator, Phase A Counter, and Phase B Counter

The timing generator provides timing reference edges for deskew latches and synchronizes generation of PXACK(L). PXACK(L) then returns to the timing generator. Outputs from the deskew latches will change on the rising edge of signals TA(H), TC(H), or TD(H) (depending on the particular latch). Timing relationships of the timing generator's input and output signals are shown in Figure 4-8.

U3075B of the timing generator receives TCLK, divides it by two, and outputs complementary 10 MHz signals. The Q(L) output of U3075B, when inverted by U2071B, is TA(H). TA(H) is used to clock the command decoder's deskew latch.

The phase A counter (U4071) is also clocked by TA(H). This

counter's outputs are: PXACK(L) @ 5 MHz, IO(H)/M(L) @ 2.5 MHz, R(H)/W(L) @ 1.25 MHz, PBPRN(L) @ .62 MHz, and the ripple-carry output, PBUSY(H) @ .62 MHz (once in every 16 TA(H) clocks).

TB(H) is generated by ANDing PXACK(L) with the inverted Q(H) output of U3075B. This is accomplished by components U3071D and U2071C. TB(H) clocks the phase B counter and flip-flop U3075A. Figure 4-8 shows the timing relationship of TB(H) to other timing generator signals.

TC(H) is generated by U4075B as a logical function of U3075B's Q(H) and Q(L), PXACK(L), and QB(H); refer to the Self-Test circuit diagram and Figure 4-8 for details. Because both the Q(H) and Q(L) outputs of U3075B are fed to U4075B, a 2:1 multiplexer function is formed. TC(H) clocks the data generators' deskew latches. On alternate AA data cycles, the data setup time at the output of the self-test generator is reduced from approximately 50 ns to 0 ns, with respect to XACK(L). The 0 ns data setup time simulates worst-case bus timing specifications.

TD(H) is generated by NORing the 10 MHz Q(H) output of U3075B with PXACK(L) (5 MHz). TD(H) clocks the address generator and deskew latches, the interrupt deskew latch, and the miscellaneous deskew latch. Figure 4-8 shows the timing relationship of TD(H) to other timing generator signals.

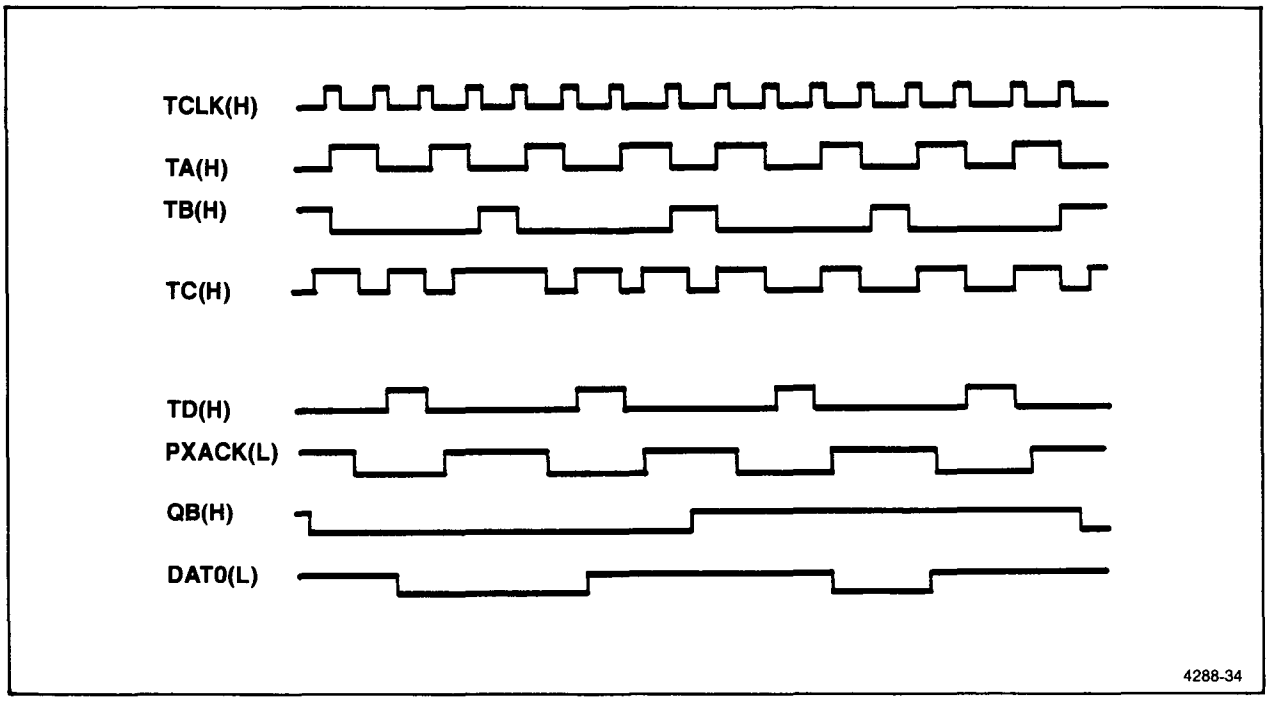


Figure 4-8. Timing generator inputs and outputs.

The phase B counter (U2065) is clocked by TB(H), operates at one-half the rate of the phase A counter, and is 180 degrees out of phase with the phase A counter.

The phase B counter's QA(H) output, and its inverted (U2031F) form, QA(L), are the inputs to the address generator and deskew latches.

The phase B counter's QB(H), QC(H), and QD(H) outputs are decoded by the interrupt decoder to simulate the eight priorities of Multibus interrupt signals. QB(H), QC(H), and QD(H) also provide input to the miscellaneous deskew latch, which simulates various other Multibus signals.

The phase B counter's ripple-carry output, PINTA(H), is a primary component for generation of INTA(L), XACK(L), and BUSY(L).

AA-55 Address Generator and Deskew Latches

This function block supplies an AA-55 (hexadecimal) pattern to the address bus on alternate bus cycles. Stimulus is provided by QA(H) and QA(L) from the phase B counter, and is strobed into deskew latches U3041, U3035, and U3025B by timing signal TD(H). Figure 4-10 shows the timing relationships of the self-test generator's address and other outputs.

AA-55 Data Generators and Deskew Latches

This function block supplies an AA-55 (hexadecimal) pattern to the data bus on alternate bus cycles. Stimulus is provided by QB(L) and PXACK(H), and is strobed into deskew latches U3051 and U3045 by timing signal TC(H). Figure 4-10 shows the self-test generator's data and other outputs (note varying data setup time).

Interrupt Decoder and Deskew Latch

The phase B counter's outputs QB(H), QC(H), and QD(H) are decoded by U3055, and are strobed into deskewing latch U3031 by the timing signal TD(H). U3031 outputs INT0-7(L). When PINTA(L) goes high, the decoder is inhibited and no outputs are asserted, simulating a cycle with no interrupts pending. (The 7D02 displays acquisition of such a cycle with a "." in the interrupt (I) field.)

Command Decoder and Deskew Latch

The command decoder generates MRDC(L), MWTC(L), IORC(L), and IOWC(L) by decoding IO(H)/M(L) and R(H)/W(L) from the phase B counter. The decoder's outputs are inhibited during Interrupt Acknowledge (displayed INA) and Bus Available (displayed AVL) cycles. Its outputs are enabled by PXACK(L) low, and are latched into U4061, along with PBPRN(L), INTA(L), XACK(L), BUSY(L), by the timing signal TA(H).

Miscellaneous Deskew and Buffer

The miscellaneous deskew and buffer function block latches and buffers QB(L), QC(L), and QD(L) from the phase B counter, to simulate various Multibus signals.

XACK(L), BUSY(L) and INTA(L) Generator

PXACK(L) is simply TA(H) divided by two. On every second cycle that PBUSY(L) is asserted, one cycle of PXACK(L) is deleted to form XACK(L), and one cycle of BUSY(L) is generated in its place.

On alternate cycles of PBUSY(H), PINTA(H) is generated to form INTA(L). BUSY(L) and XACK(L) are generated using flip-flop U3075A. When PINTA(H) is low and PBUSY(H) goes high, a low signal is clocked into the flip-flop by timing signal TB(H). The flip-flop Q(H) output goes low, disabling the command decoder, and the Q(L) output goes high, inhibiting U2071A and XACK(L) for one cycle. The signal BUSY(L) is enabled by the low on pin 10 of U3071C.

On cycles where there is no coincidence of PINTA(L) and PBUSY(H), a 1 is loaded into flip-flop U3075A. This enables the command decoder, allows the BUSY(L) line to remain low, and allows the XACK(L) line to be a function of PXACK(L). Figure 4-9 shows timing relationships of the pertinent signals.

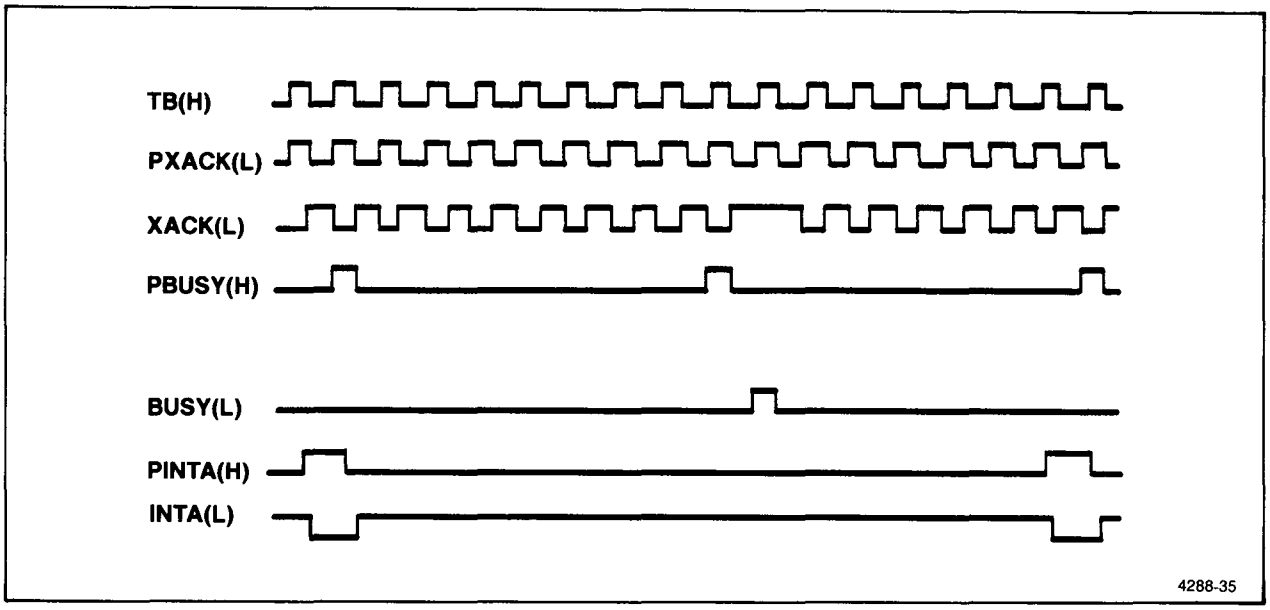


Figure 4-9. XACK(L), BUSY(L), and INTA(L) generator timing relationships.

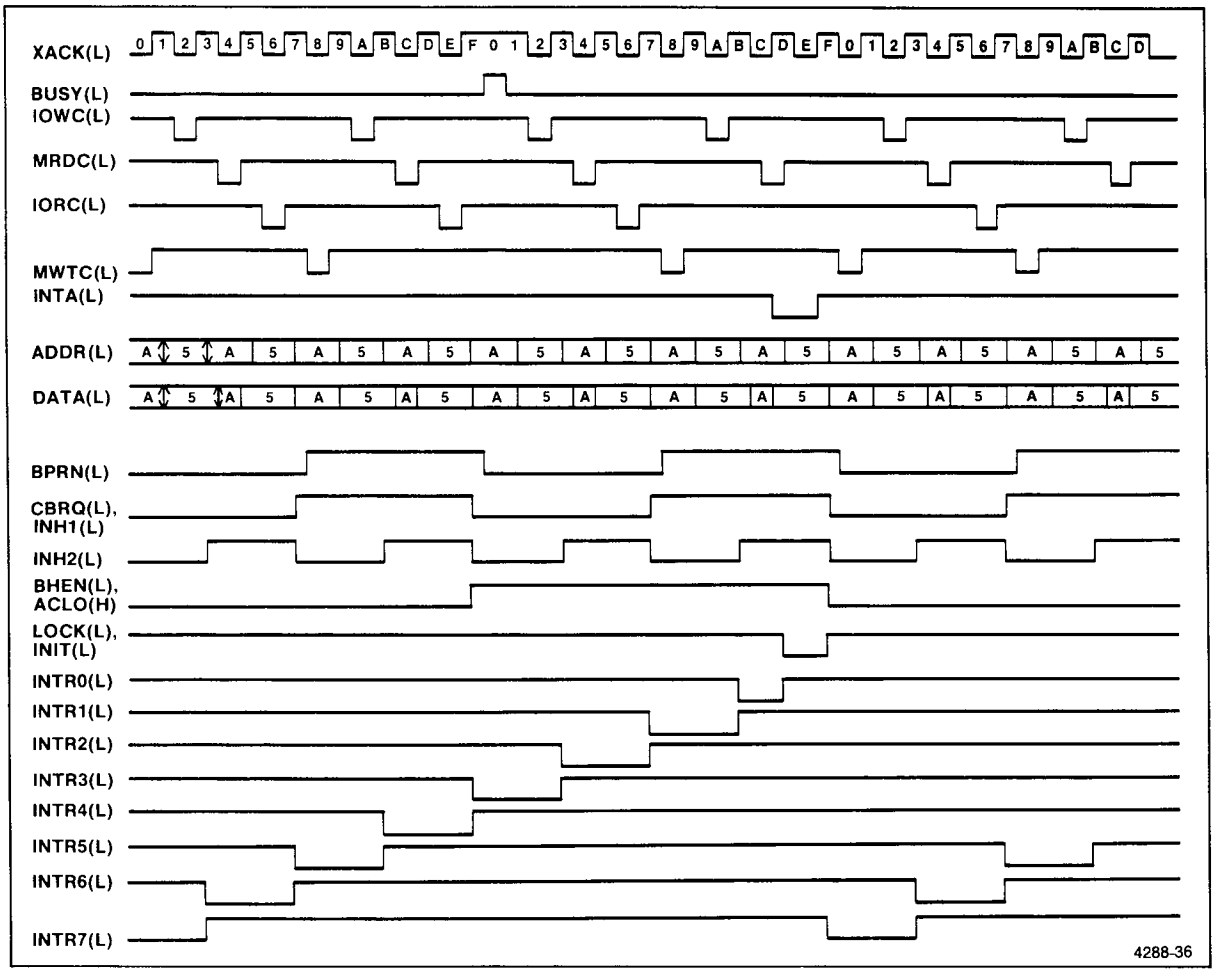


Figure 4-10. Timing relationships of self-test generator outputs.

MULTIBUS P1 EXTENDER ◇4

The PM 112 can serve as an extender board in a Multibus SUT. It will function normally while providing all Multibus P1 (PM 112 P4039) signals to an SUT board at connector socket J1030. Multibus P2 (PM 112 P4079) signals are not extended. C1010, C1012, C1051, and C1057 are decoupling capacitors, used to reduce noise on the extender power traces.

LOGIC ANALYZER PLUG ◇5

The plug board is connected to the PM 112's 64-conductor ribbon cable at J1010, and outputs to the logic analyzer at P7020. It serves to connect the PM 112's signals from the 64-conductor ribbon cable to the 7D02, which uses a different pin numbering system.

PERFORMANCE CHECKS

OVERVIEW

The procedures which follow are methods for checking operation and performance requirements of the PM 112 Personality Module. These procedures should be performed in sequence. It is assumed that the 7D02 Logic Analyzer has already passed its performance check, as detailed in the 7D02 Service Manual.

The Diagnostic Monitor portion of this section uses the 7D02 Logic Analyzer's Diagnostic Monitor to test the PM 112 Personality Module, and to test the PM 112/7D02 Timing Option circuitry (for 7D02s that are so equipped).

The Extended Diagnostics portion of this section is composed of: the Acquisition vs.Self-Test Check, used for determining whether self-test or acquisition circuitry is responsible for Diagnostic Monitor failure (requires the Optional Test Equipment listed in Table 5-1); Self-Test Acquisition check; the Word Recognizer Control Line Check; and the Clock Qualification Check.

Use the Performance Requirements Tests to verify the PM 112's Performance Requirements (listed in the Specifications section of the manual).

If the personality module is suspected of being faulty, complete the Diagnostic Monitor, all Extended Diagnostics (for which equipment is available), and the Performance Requirements Tests. Error numbers are provided for test failures; these numbers refer to symptoms and procedures in the Troubleshooting Error List, which is located in the Maintenance and Troubleshooting section.

EQUIPMENT LIST

Table 5-1 lists both required and optional test equipment. The optional test equipment is used only for the Acquisition vs. Self-Test Check (in the Extended Diagnostics portion of this section). Refer to the documentation supporting the test equipment for detailed operating instructions.

Table 5-1
TEST EQUIPMENT FOR PERFORMANCE CHECKS

Required Equipment	
DESCRIPTION	ITEM (with Tektronix part number)
Logic Analyzer	Tektronix 7D02 Logic Analyzer with Option 03 (Expansion Option); Option 01 (Timing Option) - needed for Perf. Req. Test 5 & Diag. Mod. B
Mainframe	Tektronix 7603 Oscilloscope; 100 MHz (or equivalent 7000 Series mainframe)
Timing Option Probe (T.O.-equipped 7D02s only)	Tektronix P6451 Data Acquisition Probe (010-6451-03)
Test Oscilloscope	Tektronix 465B Oscilloscope; 100 MHz (or equivalent 100 MHz oscilloscope)
Oscilloscope Probes (2 required)	Tektronix P6105; 100 MHz (010-6105-01)
TM 500 Mainframe	Tektronix TM 503 (or larger) Mainframe
Pulse Generator	Tektronix PG 502 Pulse Generator
Pulse Generator	Tektronix PG 508 Pulse Generator
Frequency Counter	Tektronix DC 504 Counter/Timer (or equivalent 50 MHz counter)
Coaxial Cable (10 in.)	50 ohm Coaxial Cable (012-0208-00)
BNC-to-Dual-Lead Adapters (2 required)	BNC Female to EZ Ball (013-0076-01)
BNC Male to BNC Male Adapters (2 required)	Adapter (103-0029-00)
40 cm Lead Set	10 Wires with Pomona Grabbers (012-0670-00)
Connector Socket	86-pin Edge Connector (131-2848-00)
Square Pin Row (T.O.-equipped 7D02s only)	Square Pin Row (131-1614-00)

Table 5-1 (cont.)

TEST EQUIPMENT FOR PERFORMANCE CHECKS

Optional Equipment

DESCRIPTION	ITEM (with Tektronix part number)
Test PM 112	PM 112 Personality Module
2nd Logic Analyzer	Tektronix 7D02 Logic Analyzer with Option 03 (Expansion Option)
2nd Mainframe	Tektronix 7603 Oscilloscope (or equivalent 7000 Series mainframe)
Harmonica Cable (T.O.-equipped 7D02s only)	Cable Set (012-0800-00)

PRELIMINARY SETUP

CAUTION

Always turn off the mainframe power before connecting or disconnecting the personality module to avoid damage to any of the instruments.

1. Turn off the logic analyzer's mainframe power.
2. Insert the PM 112's logic analyzer cable plug into the 7D02's front panel receptacle. (The PM 112 should not be plugged into a Multibus cardcage.)
3. Move the strap on jumper W3085 (located near the ribbon cable and on the edge of the board) to the TEST position.
4. Move all straps on jumpers W2011-0 through W2011-7, W3011, W3015, and W4075 to their default positions (indicated by tick marks on the leftmost pairs of pins).
5. (Timing Option-equipped 7D02s only.) Using Table 5-2, connect the P6451 Timing Option Probe to the row of pins (TP1021) labeled TIMING OPT. STIMULUS, located in the extender socket corner of the PM 112.

NOTE

If you use the optional harmonica cable with the P6451 Timing Option Probe, the wires from the P6451 should be connected to the harmonica cable with square pins of the proper size. You can then use the harmonica cable as a convenient method of connection to the timing option pins at TP1021.

Table 5-2
P6451 TIMING OPTION CONNECTION

COLOR CODE	WIRE #	TP1021 PIN
White	GND	1, GND
Black	0 (lsb)	2, CH0
Brown	1	3, CH1
Red	2	4, CH2
Orange	3	5, CH3
Yellow	4	6, CH4
Green	5	7, CH5
Blue	6	8, CH6
Violet	7 (msb)	9, CH7

DIAGNOSTIC MONITOR

OVERVIEW

The following subsection describes procedures needed to perform the 7D02 Diagnostic Module tests for the personality module and Timing Option. The tests confirm the 7D02's ability to do the following:

- Read and recognize pre-programmed word recognizers.
- Compare the data in the personality module EPROM to the logic information in the 7D02.
- Fill the acquisition memory upon recognition of the appropriate word recognizers. (This requires the PM 112 to properly generate and acquire its self-test stimulus.)
- Compare acquisition memory checksums to checksums stored in the personality module EPROM. (This also requires proper generation and acquisition of the self-test stimulus.)
- Display error codes.

For detailed explanation of these tests and their failure codes, refer to the Diagnostic Module 9 and Diagnostic Module B subsections of this manual's Maintenance and Troubleshooting section, and to the 7D02 Service Manual.

NOTE

Diagnostic Module tests 0, 9, and B will pass only if the PM 112 is configured in the self-test mode (described in Preliminary Setup). When you select one of these tests from the Diagnostic Monitor Menu, the reminder message PLEASE CONNECT SELF-TEST STIMULUS will appear whether or not the PM 112 is already configured in self-test mode.

DIAGNOSTIC MODULE 9 (PER. MOD.-SYSTEM)

To run the subtests of diagnostic module 9, use the following procedure:

1. Turn on the mainframe power and press any 7D02 front panel key (except X or START) within two seconds. Keep the key depressed for at least five seconds to simulate a keyboard failure. Simulating a keyboard failure allows entry into the DIAGNOSTIC MONITOR.

2. Press the X key to bring the DIAGNOSTIC MONITOR menu to the screen.

3. Press the 9 key to test the PER. MOD.- SYSTEM (personality module system).

4. Press the E key to select ENABLE LOOPING.

5. Press the START/STOP key to run Test 1.

6. A number such as 1566-XX (the part number of the personality EPROM), is associated with Test 1 and is normal.

7. Wait at least 5 seconds and press the START/STOP key to run the next test.

8. Repeat part 7 until all of the tests have been completed.

9. A number associated with any test other than Test 1 is a failure. A number associated with any PASS message indicates a transient failure. A number associated with a FAIL message indicates a solid failure. Write down all numbers associated with any PASS or FAIL messages. If any failures are noted, refer to Troubleshooting Error List, Error 1, and Diagnostic Module 9 (PER. MOD.-SYSTEM) in the Maintenance and Troubleshooting section of this manual.

10. Press the START/STOP key, then the X key to return to the menu.

DIAGNOSTIC MODULE B (TIMING OPTION)
(Timing Option-equipped 7D02s only)

To run the subtests of Diagnostic Module B, use the following procedure:

1. If the 7D02 Diagnostic Module 9 (PER. MOD.-SYSTEM) was previously run, continue to step 2. If not, perform steps 1 and 2 of the PER. MOD.-SYSTEM test.

2. Press the B key to run the TIMING OPTION module.

3. Press the E key to ENABLE LOOPING.

4. Press the START/STOP key.

5. Wait for five seconds in between all tests. Using the START/STOP key, run the remaining two tests.

6. A number associated with any test is a failure. A number associated with a PASS message indicates a transient failure. A number associated with a FAIL message indicates

a solid failure. Write down all numbers associated with any PASS or FAIL messages. If any failures are noted, refer to Diagnostic Module B (TIMING OPTION) and Troubleshooting Error List, Error 2, located in the Maintenance and Troubleshooting section of this manual.

EXTENDED DIAGNOSTICS

If no failures were noted using the DIAGNOSTIC MONITOR portion of this section, the Extended Diagnostics need not be performed.

ACQUISITION vs. SELF-TEST CHECK

This test requires the Optional Test Equipment listed in Table 5-1: a PM 112 known to be working properly, and a second 7D02 with mainframe. Provided the equipment is available, this test is highly recommended.

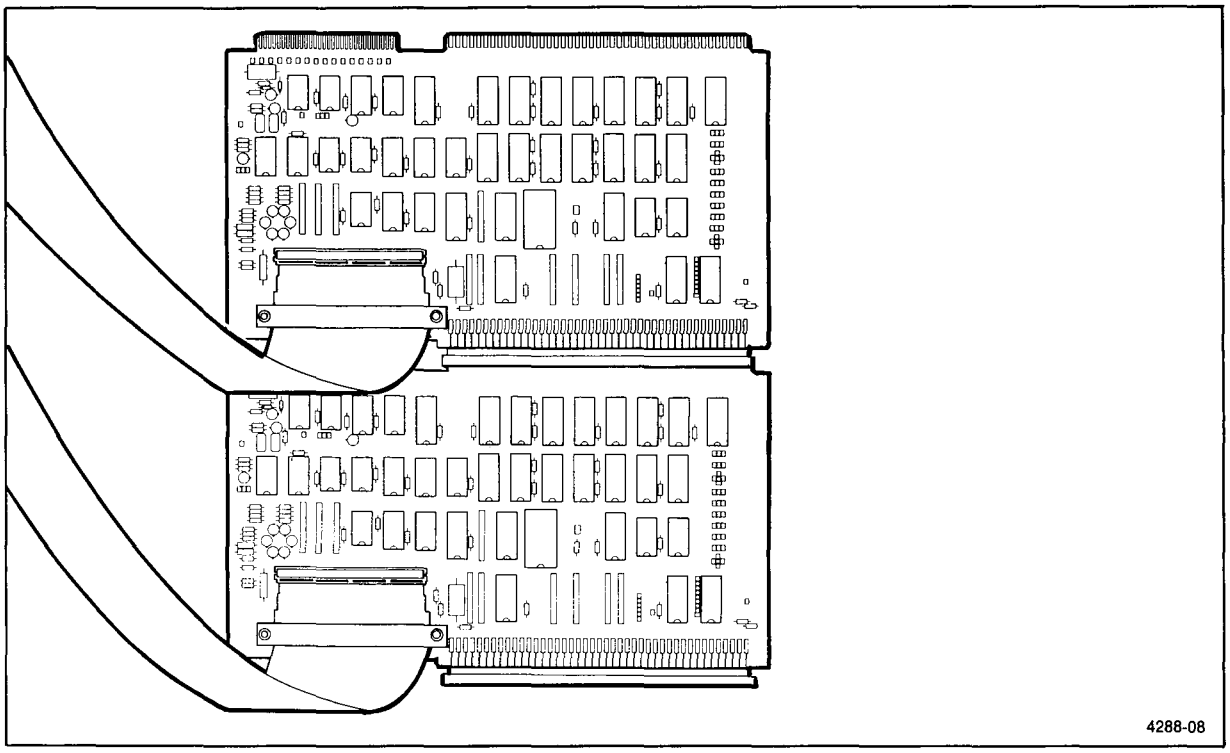


Figure 5-1. Testing a suspect PM 112 with a known-good PM 112.

The Acquisition vs. Self-Test Check is an efficient way to determine whether the PM 112 under test fails DIAGNOSTIC MONITOR tests because its acquisition circuitry is faulty, or because the self-test circuitry itself is faulty. This determination is made by 1) using a known-good PM 112 to supply the self-test stimulus

and observing whether this is correctly acquired by the PM 112-under-test, and 2) using the known-good PM 112 to acquire the PM 112-under-test's self-test stimulus.

Preliminary Equipment Setup

1. Turn off power to both 7D02s.
2. Plug the known-good PM 112 into the extra 7D02. (Both PM 112s will remain unplugged from a Multibus backplane).
3. Move jumper W3085 on the known-good PM 112 to the TEST position.
4. Move jumper W3085 on the PM 112 under test to the NORM position.
5. On both PM 112s, move jumpers W2011-0 through -7, W3011, W3015, and W4075 to their default positions (indicated by tick marks).
6. Plug P4039 of the PM 112 under test into J1030 (the Multibus extender socket) of the good PM 112, as shown in Figure 5-1.
7. Power up both 7D02s.

Acquisition Check

1. Run the Self-Test Acquisition Check (located after the Self-Test vs. Acquisition Check) on the PM 112 under test using the equipment setup detailed above. A known-good stimulus will be generated by the other PM 112.
2. If any failures occur, the acquisition circuitry of the PM 112 under test is suspect. To further identify specific problems, Diagnostic Module 9 (PER. MOD.-SYSTEM) may be run on the PM 112 under test, using the same equipment setup. Note any resulting error codes, and refer to their explanations in the Maintenance and Troubleshooting section. Refer also to the Theory of Operation section and circuit diagrams.

Self-Test Check

1. Use the Preliminary Equipment Setup detailed previously.
2. Move jumper W3085 on the known-good PM 112 to the NORM position.
3. Move jumper W3085 on the PM 112 under test to the TEST position.

4. Run the SELF-TEST ACQUISITION CHECK (following in this section of the manual) on the good PM 112. A questionable stimulus will be generated by the PM 112 under test. Because it is acquired by a known-good PM 112, it will accurately reflect the health of the PM 112-under-test's self-test circuitry.

5. If any failures occur, the self-test circuitry of the PM 112 under test is suspect. To further identify specific problems, Diagnostic Module 9 (PER. MOD.-SYSTEM) may be run on the known-good PM 112, using the same equipment setup. Note any resulting error codes, and refer to their explanations in the Maintenance and Troubleshooting section. Refer also to the Theory of Operation section and circuit diagrams.

SELF-TEST ACQUISITION CHECK

The following check allows you to acquire a listing of the PM 112 self-test acquisition pattern and compare it to Figure 5-3.

Enter the program shown in Figure 5-2 into the 7D02:

1. Power up the 7D02.

2. Push the 7D02 TRIGGER button.

3. Use the 7D02 cursor keys and alphanumeric keypad to enter the values R/W="0", MEM/IO="1", INTA+AVAL="0", INTR="1", and IPR="7", as shown in Figure 5-2.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX XX /BHEN=X
1 ADDRESS=XXXXX
1 R/W=0  MEM/IO=1  INTA+AVAL=0
1 INTR=1  IPR=7
1 /INH1=X /INH2=X  EXT. TRIG. IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    0-STANDARD CLOCK QUAL.
 END TEST 1
```

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Figure 5-2. 7D02 program for PM 112 self-test acquisition.

4. Press the 7D02 START/STOP key. The 7D02 should trigger on DATA="55 55", CMND="MWT", I="7".

5. Using the DATA SCROLLING keys, compare the screen display (0-255) to the display shown in Figure 5-3. The trigger location, marked by "---T", may appear on any line between 0 and 15. Wherever the trigger position occurs, the patterns starting with it should appear identical to the pattern starting with the trigger location shown in Figure 5-3. (The self-test program is a 16 line repeating pattern. The pattern will repeat 16 times in the 7D02 memory, for a total of 256 lines.)

LOC	ADDR	UDC7-0	DATA	CMND	I
---T	55555		5555	MWT	7
016	AAAAA		AAAA	IOW	7
017	55555		5555	MRD	6
018	AAAAA		AAAA	IOR	6
019	55555		5555	MWT	5
020	AAAAA		AAAA	IOW	5
021	55555		5555	MRD	4
022	AAAAA		AAAA	IOR	4
023	55555	01011111	55	AVL	3
024	AAAAA	01010111	AA	IOW	3
025	55555	01111110	55	MRD	2
026	AAAAA	01111011	AA	IOR	2
027	55555	11011101	55	MWT	1
028	AAAAA	11010111	AA	IOW	1
029	55555	11111110	55	MRD	0
030	AAAAA	10101111	AA	INA	.
031	55555		5555	MWT	7

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Figure 5-3. 7D02 display of PM 112 self-test acquisition pattern. This pattern is 16 lines long and will repeat throughout the 7D02 acquisition memory.

6. Any deviation from the pattern shown in Figure 5-3, except for the trigger LOC (location), and LOC of the lines of the pattern following it, should be considered a failure. If any failures occur, make note of the deviations and refer to Troubleshooting Error List, Error 3, in the Maintenance and Troubleshooting section of this manual.

WORD RECOGNIZER CONTROL LINE CHECK

The following procedure verifies the correct operation of the PM 112's control lines C5-C0, which are connected to the 7D02's Word Recognizers.

1. Turn the 7D02 off for five seconds, then on again, to delete any previous programs.

2. Press the 7D02 TRIGGER key.

3. Using the CURSOR and NUMERIC ENTRY keys, change the R/W field to "1", the MEM/IO field to "1", and the INTA+AVAL field to "0", as shown in Figure 5-4.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX XX /BHEN=X
1 ADDRESS=XXXXX
1 R/W=1   MEM/IO=1   INTA+AVAL=0
1 INTR=X   IPR=X
1 /INH1=X /INH2=X   EXT. TRIG. IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1     0-BEFORE DATA
1     0-SYSTEM UNDER TEST CONT.
1     0-STANDARD CLOCK QUAL.
 END TEST 1
                                4288-11
```

Figure 5-4. 7D02 program for PM 112 Control Line Check.

4. Run the program by pressing the 7D02 START/STOP key.

5. The program should trigger on a Memory Read, indicated by "MRD" in the CMND column. (The trigger LOC, indicated by "---T", may occur anywhere from 0 to 15, and the UDC, DATA, and I fields may vary.)

6. If the 7D02 does not trigger on a "MRD" cycle, refer to Troubleshooting Error List, Error 4, in the Maintenance and Troubleshooting section of this manual.

7. Using the CURSOR and NUMERIC ENTRY keys, change the R/W field to "0".

8. Run the program by pressing the 7D02 START/STOP key.

9. The program should trigger on a Memory Write ("MWT"). (The trigger LOC and the UDC, DATA, and I fields may vary.)

10. If the program does not trigger on a Memory Write, refer to Troubleshooting Error List, Error 4, in the Maintenance and Troubleshooting section of this manual.

11. Using Table 5-4, repeat the previous procedure to test for "IOR", "IOW", "INA", and "AVL" type CMND cycles. If the 7D02 does not trigger on the intended CMND cycle type, refer to Troubleshooting Error List, Error 4, in the Maintenance and Troubleshooting section of this manual.

12. Using the CURSOR and NUMERIC ENTRY keys, return the R/W, MEM/IO, and INTA+AVAL fields to "X" (don't care).

13. Change the /BHEN field to "1".

14. Run the program by pressing the 7D02 START/STOP key.

15. The program should trigger on an 8-bit DATA transfer, accompanied by a display of eight bits under the UDC column.

16. If the 7D02 triggers on a cycle showing 16 bits of data, refer to Troubleshooting Error List, Error 5, in the Troubleshooting and Maintenance section of this manual.

17. Using the CURSOR and NUMERIC ENTRY keys, change the /BHEN field to "0".

18. Run the program by pressing the 7D02 START/STOP key.

19. The 7D02 should trigger on a cycle with a 16-bit DATA transfer. The UDC field on this cycle should be blank.

20. If the 7D02 triggers on an 8-bit cycle, refer to Troubleshooting Error List, Error 5, in the Maintenance and Troubleshooting section of this manual.

21. Using the CURSOR and NUMERIC ENTRY keys, place a "1" in the /BHEN field, and a "0" in the /INH1 field.

22. Run the program by pressing the 7D02 START/STOP key.

23. The program should trigger on a cycle with UDC7 (the leftmost bit in the UDC field) equal to "0". (The default signal carried on UDC7 is INH1(L).)

24. If the 7D02 does not trigger with UDC7="0", refer to Troubleshooting Error List, Error 6, in the Maintenance and Troubleshooting section of this manual.

25. Leaving /BHEN="1", place a "1" in the /INH1 field.

26. Run the program.

27. The 7D02 should now trigger on a cycle where UDC7="1".

28. If the 7D02 does not trigger with UDC7="1", refer to Troubleshooting Error List, Error 6, in the Maintenance and Troubleshooting section of this manual.

29. Return the /INH1 field to "X" and place a "0" in the /INH2 field. Leave /BHEN="1".

30. Run the program.

31. The 7D02 should trigger with UDC5 (the third bit from left in the UDC field) equal to "0". (The default signal carried on UDC5 is INH2(L).)

32. If UDC5 does not equal "0", refer to Troubleshooting Error List, Error 7, in the Maintenance and Troubleshooting section of this manual.

33. Leaving /BHEN="1", place a "1" in the /INH2 field.

34. Run the program.

35. The 7D02 should now trigger on a cycle with UDC5="1".

36. If UDC5 does not equal "1", refer to Troubleshooting Error List, Error 7, in the Troubleshooting and Maintenance section of the manual.

CLOCK QUALIFICATION CHECK

The following procedure verifies correct operation for the PM 112's clock qualifier lines, C9 through C4.

1. Move the strap on W3011 to the "8" position.

2. Turn the 7D02 power off for five seconds, then on again, to remove any previous programs.

3. Press the 7D02 TRIGGER key.

4. Using the CURSOR and NUMERIC ENTRY keys, enter a "1" in the STANDARD CLOCK QUAL. field to specify USER CLOCK QUAL.

5. Move the cursor to C9-C4 (ANDED CLOCKS)=XXXXXX. Change C9 (the leftmost bit) to "0". (C9 is connected to BUSY. When "0" is placed in the C9 field, only the cycles on which the bus is Available ("AVL" = Not Busy) are qualified.

6. Run the program by pressing the 7D02 START/STOP key.

7. Every cycle should be an "AVL" (Not Busy) CMND cycle type.

8. If any other types of cycles are acquired, refer to Troubleshooting Error List, Error 8, in the Troubleshooting and Maintenance section of this manual.

9. Now change C9 to "1".

10. Run the program. There should be no "AVL" CMND cycle types.

11. If any "AVL" cycles are acquired, refer to Troubleshooting Error List, Error 8, in the Maintenance and Troubleshooting section of this manual.

12. Return the C9 bit of the C9-C4 (ANDED CLOCKS) field to "X" (don't care), and enter "0" in C8 (to right of C9).

13. Move the W2011-7 (UDC7) jumper strap to the "ACLO" position.

14. Run the program.

15. Every cycle acquired should show UDC7 equal to "0". If not, refer to Troubleshooting Error List, Error 9, in the Maintenance and Troubleshooting section of the manual.

16. Change the "0" in the C8 field to "1" and run the program.

17. Every cycle acquired should now show UDC7="1". If not, refer to Troubleshooting Error List, Error 9, in the Maintenance and Troubleshooting section of this manual.

18. Return the C8 field to "X" (don't care).

19. Continue the procedure for the remaining clock qualifier lines C7 through C4, using the setup and expected results summarized in Table 5-3. After testing a line, return its clock qualifier field to "X" (don't care) before proceeding to the next field.

20. If any of the acquired cycle types are not as expected, the Error number corresponding to the line tested is given in Table 5-3.

Table 5-3
CLOCK QUALIFICATION CHECK PROCEDURE SUMMARY

Control Line	Clk. Qual. Value	Move UDC Strap	Cycle Types Expected	Error Number*
C9	0		all AVL	8
C9	1		none AVL	8
C8	0	UDC7 to ACLO	all UDC7=0	9
C8	1	" " "	all UDC7=1	9
C7	0		all UDC6=0	10
C7	1	" " "	all UDC6=1	10
C6	0	UDC6 to /CBRQ	all UDC0=0	11
C6	1	" " "	all UDC0=1	11
C5	0		all UDC5=0	12
C5	1	" " "	all UDC5=1	12
C4	0	UDC7 to /INH1	all UDC7=0	13
C4	1	" " "	all UDC7=1	13

*If acquired cycle types are not as expected, refer to Troubleshooting Error List in the Maintenance and Troubleshooting section of this manual.

PM 112 PERFORMANCE REQUIREMENTS TESTS

OVERVIEW

The Performance Requirements listed in the Specification Section of this manual may be verified using the procedures which follow.

The following performance test equipment setup procedure is required for verifying the data setup time (Test 1), the data hold time (Test 2), the command setup time (Test 3), the command hold time (Test 4) and the Timing Option setup and hold times (Test 5).

Self-test clock accuracy is measured in Test 6, which has its own test equipment setup procedure.

PRELIMINARY EQUIPMENT SETUP -- TESTS 1, 2, 3, 4, and 5

1. Insert the PM 112 logic analyzer plug into the 7D02.

2. Plug the PM 112 edge connector P4039 into the mating 86-pin edge connector socket (specified in the Required Test Equipment List). Subsequent references to P4039 in this equipment setup procedure and in Tests 1 through 5 will apply to this socket. Make connections to P4039 via the socket's pins, as shown in Figure 5-5.

3. Plug the PG 502 and PG 508 Pulse Generators into the TM 503 mainframe with the PG 502 on the left, and the PG 508 on the right.

4. Set up the PG 502 control knobs and switches as follows:

    a) Pull out the BACK TERM knob.

    b) Set the Pulse Duration range switch to 5 ns.

    c) Set the Variable Pulse Duration knob to approximately the 12 o'clock position.

    d) Set the Period range switch to 0.1 us.

    e) Set the Variable Period knob to approximately the 10 o'clock position.

    f) Press the Complement button (in).

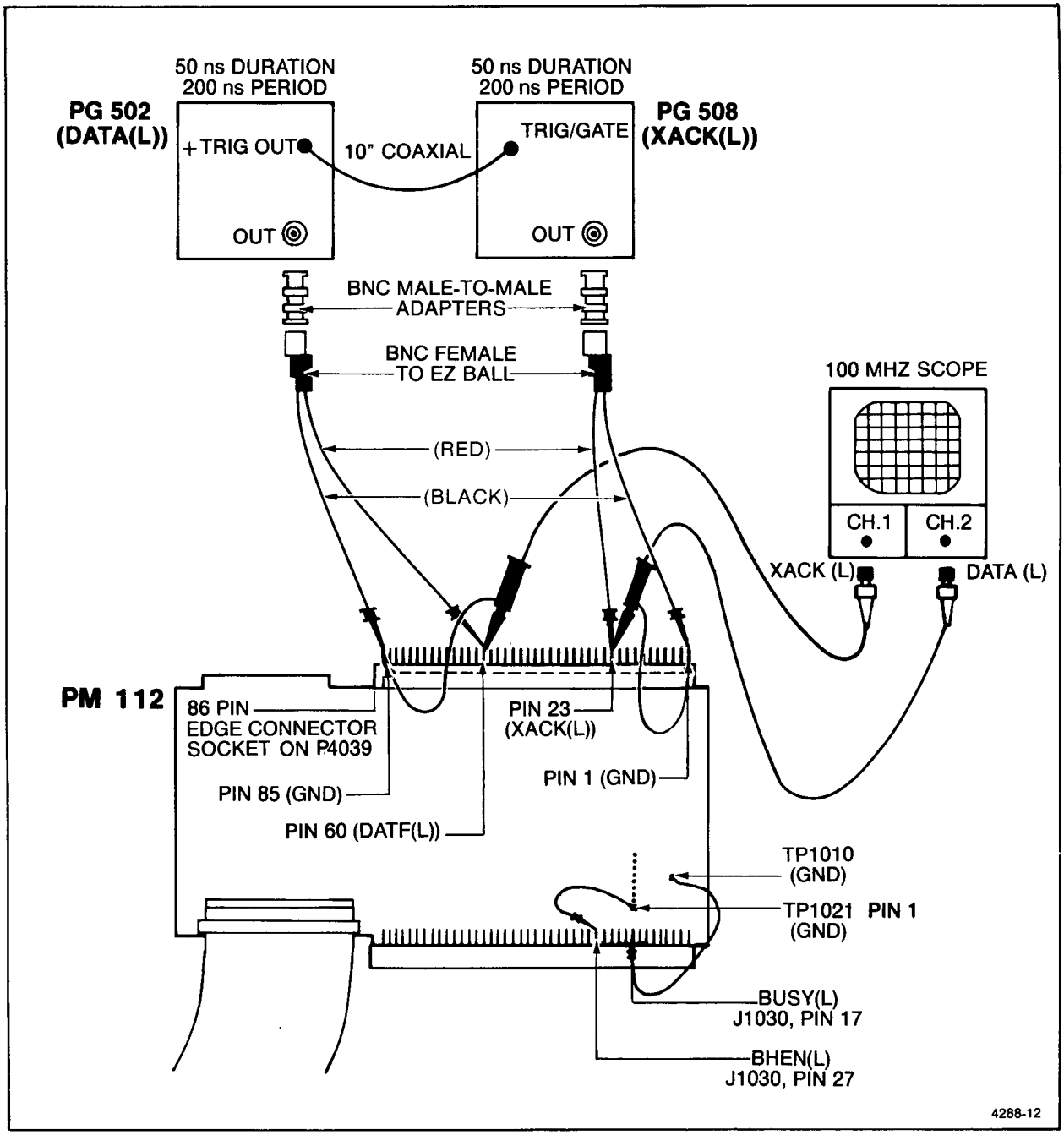

Figure 5-5. Initial equipment connections for Tests 1 through 5. Note that odd-numbered P4039 pins are located on the top (component) side of the board, even numbered pins on the bottom (circuit) side.

5. Set up the PG 508 control knobs and switches as follows:

   a) Set the Transition Time range switch to 5 ns.

b) Set the Leading and Trailing knobs to the X1 position.

c) Set the Trigger Slope button to "-" (out), the Free Run button (out), and the Mode button to Delay (in).

d) Set the Period range switch to EXT TRIG.

e) Set the Variable Period knob fully counter-clockwise to the CAL position.

f) Set the Delay range switch to 10 ns.

g) Set the Variable Delay knob fully clockwise.

h) Set the Duration range switch to 0.1 us.

i) Set the Variable Duration knob fully counter-clockwise.

j) Set the NORM/COMPLEMENT button to the Normal (out) position.

k) Set the PRESET/VAR button to the VAR (out) position.

l) Set the TRIG/GATE LEVEL knob to approximately the two o'clock position.

6. Connect the 10 inch coaxial cable from the +Trigger Out of the PG 502 to the Trig/Gate In of the PG 508. (The PG 502 will trigger the PG 508.) Refer to Figure 5-5.

7. Set up the oscilloscope control knobs and switches as follows:

a) Set the horizontal TIME/DIV to 20 ns.

b) Set trigger slope to minus (-).

c) Set the INT TRIG to CH 1.

d) Set both CH 1 and CH 2 vertical attenuators to 1 VOLT/DIV.

e) Set Vert Mode to ALT.

f) Set both CH 1 and CH 2 vertical input coupling switches to the GND position.

8. Connect EZ Ball adapter to PG 502 OUTPUT, using BNC male to male adapter.

9. Connect second EZ Ball adapter to PG 508 OUTPUT, using second BNC male-to-male adapter.

10. Connect scope CH 1 probe to PG 502 EZ Ball adapter.

11. Connect scope CH 2 probe to PG 508 EZ Ball adapter. Refer to Figure 5-5.

12. Power up oscilloscope.

13. Power up TM 503 mainframe to power the PG 502 and PG 508.

14. Adjust the PG 508 TRIG/GATE LEVEL knob until the green TRIG'D/GATE indicator is blinking. (The blinking indicates that the PG 508 recognizes trigger/gate impulses and is triggering on them.)

15. Adjust scope CH 1 and CH 2 vertical positions for zero volts at the center graticule line.

16. Switch the CH 1 input coupling to DC and adjust the PG 502 output pulses for a low level of +0.6 V and a high level of +2.0 V.

17. Switch the CH 1 input coupling switch to ground, and position the trace 1.4 divisions below the center graticule line. Return the coupling switch to DC.

18. Adjust the PG 502 Variable Period knob to obtain a period of 200 ns at the center graticule. Refer to Figure 5-6.

19. Switch the horizontal TIME/DIV to 10 ns/DIV.

20. Adjust the PG 502 Variable Duration knob for a 50 ns pulse width low.

21. Switch the scope VERT MODE to CH 2.

22. Switch the CH 2 input coupling to DC and adjust the PG 508 output pulses for a low level of +0.6 V and a high level of +2.0 V.

23. Switch the CH 2 input coupling switch to ground, and position the trace 0.6 divisions above the center graticule line. Return the coupling switch to DC.

24. Adjust the PG 508 Variable Duration knob for a 50 ns pulse width low, at the graticule line 2 divisions above the center line. Refer to Figure 5-6.

25. Switch the scope VERT MODE to ALT.

26. Set INT TRIG to CH 2.

27. Adjust the PG 508 VARIABLE DELAY knob to align the falling edges of the two traces, as shown in Figure 5-6.

28. Switch the horizontal TIME/DIV back to 20 ns/DIV.

29. Set up the PM 112 as follows:

    a) Move the strap on jumper W3085 to the NORM position.

    b) Connect a jumper wire from TP1010 (GND) to J1030, pin 17 (BUSY(L)).

    c) Connect a second jumper wire from TP 1021, pin 1 (GND) to J1030, pin 27 (BHEN(L)).

30. Connect the red EZ Ball hook from the PG 508 to the PM 112 P4039, pin 23 (XACK(L)). Refer to Figure 5-5.

31. Connect the oscilloscope CH 2 probe to P4039, pin 23 (XACK(L)).

32. Connect the black ground clips from the scope CH 2 and the PG 508 to P4039, pin 1 (GND).

NOTE

The preceding Preliminary Equipment Setup procedure is required for the following Performance Requirements Tests 1 through 5.

TEST 1 -- DATA (DAT0(L)-DATF(L)) SETUP TIME

1. Connect the red EZ Ball hook from the PG 502 to the PM 112 P4039, pin 60 (DATF(L)).

2. Connect the scope CH 1 probe to P4039, pin 60 (DATF(L)).

3. Connect the black ground clips from the scope CH 1 and the PG 502 to P4039, pin 85 (GND).

4. Confirm that the oscilloscope waveforms are as shown in Figure 5-6.

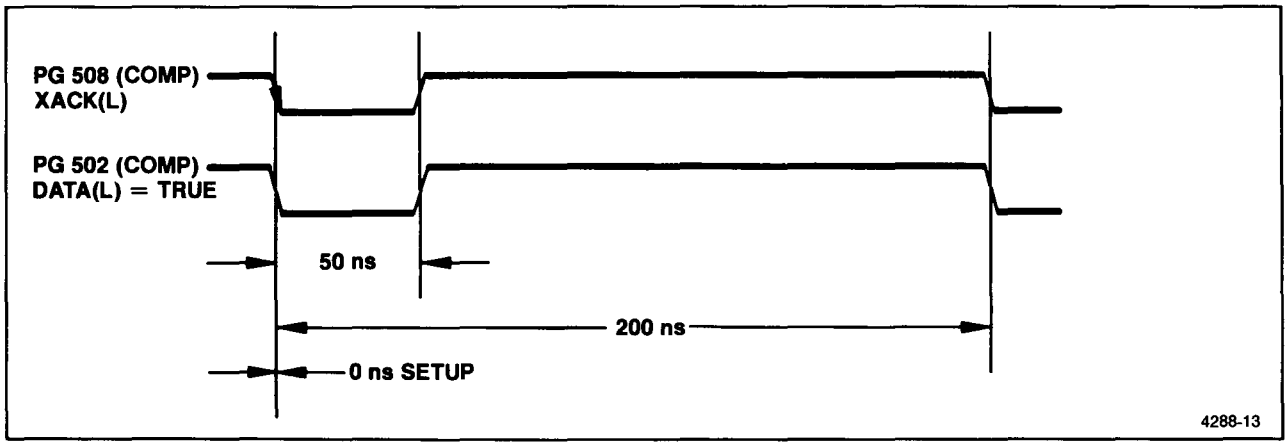

Figure 5-6. DATA setup time (DATA TRUE).

5. Turn the 7D02 power off for five seconds, then on again, to delete any previous programs.

6. Press the 7D02 TRIGGER key to obtain the program shown in Figure 5-7.

7. Enter the Format mode by pressing the 7D02 FORMAT key.

8. Using the CURSOR and NUMERIC ENTRY keys, change the Word Recognizer DATA field to binary radix.

9. Exit the Format mode by pressing the FORMAT key.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX XX /BHEN=X
1 ADDR=XXXXX
1 R/W=X  MEM/IO=X  INTA+AVAL=X
1 INTR=X  IPR=X
1 /INH1=X /INH2=X  EXT. TRIG. IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
      0-BEFORE DATA
      0-SYSTEM UNDER TEST CONT.
      0-STANDARD CLOCK QUAL.
END TEST 1
                                4288-14
```

Figure 5-7. 7D02 program for DATA setup time (Test 1).

10. Check that the Word Recognizer DATA field appears as follows:

    1 DATA=XXXXXXXX XXXXXXXX

11. Change DATF, the far left DATA bit in the 7D02 program, to "0". All other elements should be in the "X" (don't care) state.

12. Run the program by pressing the START/STOP key.

13. The program should run without triggering, or indicating SLOW CLOCK. This will demonstrate that the 7D02 is seeing the minimum clock and data pulse widths, and is meeting the 0 ns maximum setup time.

14. Stop the program by pressing the 7D02 STOP key.

15. If any failures occur, refer to Troubleshooting Error List, Error 14, in the Maintenance and Troubleshooting section.

16. Change the PG 502 Complement button to the NORM position (out) and adjust the oscilloscope to bring the pulses on the screen. Verify that the pulse out of the PG 502 is 0 ns before and 50 ns after the falling edge of the XACK(L) pulse (PG 508). Refer to Figure 5-8.

17. Change DATF, the far left DATA bit in the 7D02 program, to "1". Press the START/STOP key.

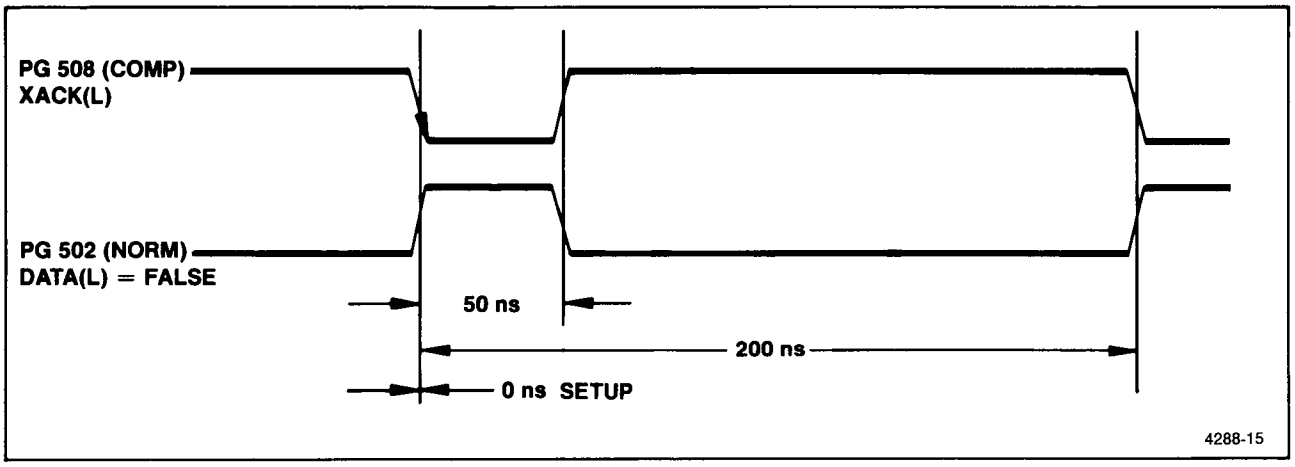

Figure 5-8. DATA setup time (DATA FALSE).

18. No SLOW CLOCK message should be present on the 7D02 display, and no trigger should be received. Press the STOP key.

19. Repeat the test for DATE. Move the PG 502 and scope probes from pin 60 of P4039 to pin 59 (in the row of pins

corresponding to the top of the board).

20. Change the leftmost bit in the DATA field of the 7D02 program to "X", and enter a "0" in the DATA bit immediately to the right of it.

21. After testing for "0" in the word recognizer DATE bit, test for "1" in the DATE bit. Repeat the previous procedure for the remaining data lines (referring to the circuit diagram of the extender for P4039 pin numbers), and remember that:

Word Recognizer DATA Bit	PG 502 COMPLEMENT Button	Multibus Data
1	Normal (out)	False
0	Complemented (in)	True

22. Refer to Figure 5-8.

23. If any failures occur, refer to Troubleshooting Error List, Error 14, in the Maintenance and Troubleshooting section of this manual.

24. If you are proceeding to tests 2, 3, 4, or 5, leave all oscilloscope probes and test clips connected.

TEST 2 -- DATA (DAT0(L)-DATF(L)) HOLD TIME

1. Connect the red EZ Ball hook from the PG 502 to the PM 112 P4039, pin 60 (DATF(L)).

2. Connect the scope CH 1 probe to P4039, pin 60 (DATF(L)).

3. Connect the black ground clips from the scope CH 1 and the PG 502 to P4039, pin 1 (GND).

4. Press the PG 502 Complement button (in).

5. Adjust the PG 508 Variable Delay knob so that the rising edge of DATF(L) occurs 35 ns after the falling edge of XACK(L).

6. Confirm that the oscilloscope waveforms are as shown in Figure 5-9.

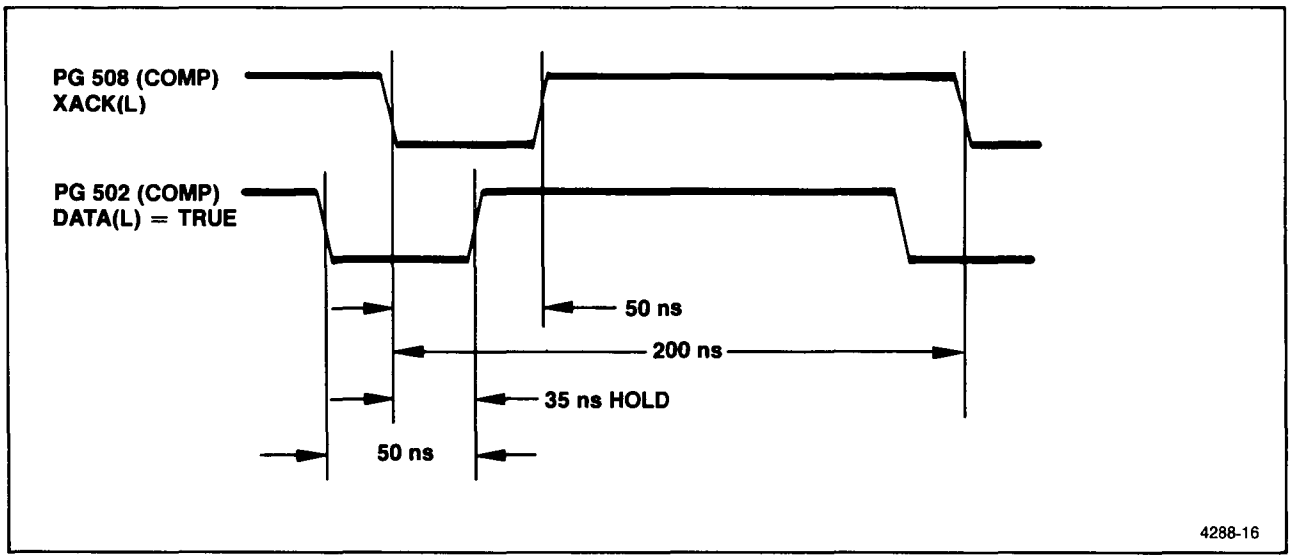

Figure 5-9. DATA hold time (DATA TRUE).

7. Turn the 7D02 power off for five seconds, then on again, to delete any previous programs.

8. Press the 7D02 TRIGGER key to get the program shown in Figure 5-10.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX XX /BHEN=X
1 ADDR=XXXXX
1 R/W=X  MEM/IO=X  INTA+AVAL=X
1 INTR=X  IPR=X
1 /INH1=X /INH2=X  EXT. TRIG. IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER O-MAIN
      O-BEFORE DATA
      O-SYSTEM UNDER TEST CONT.
      O-STANDARD CLOCK QUAL.
END TEST 1
```

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Figure 5-10. 7D02 program for DATA hold time (Test 2).

9. Enter the Format mode by pressing the 7D02 FORMAT key.

10. Using the CURSOR and NUMERIC ENTRY keys, change the Word Recognizer DATA field to binary radix.

11. Exit the Format mode by pressing the FORMAT key.

12. Check that the Word Recognizer DATA field appears as follows:

```
1 DATA=XXXXXXXX XXXXXXXX
```

13. Change DATF, the leftmost DATA bit in the 7D02 program, to "0". All other elements should be in the "X" (don't care) state.

14. Run the program by pressing the START/STOP key.

15. The program should run without triggering, and without indicating SLOW CLOCK. This will demonstrate that the 7D02 is seeing the minimum clock and data pulse widths, and is meeting the 35 ns maximum hold time.

16. Stop the program by pressing the 7D02 STOP key.

17. If any failures occur, refer to Troubleshooting Error List, Error 15, in the Maintenance and Troubleshooting section of this manual.

18. Change the PG 502 Complement button to the NORM position (out) and adjust the oscilloscope to bring the pulses on the screen. Verify that the pulse out of the PG 502 is 0 ns before and 50 ns after the falling edge of the XACK(L) pulse (PG 508). Refer to Figure 5-11.

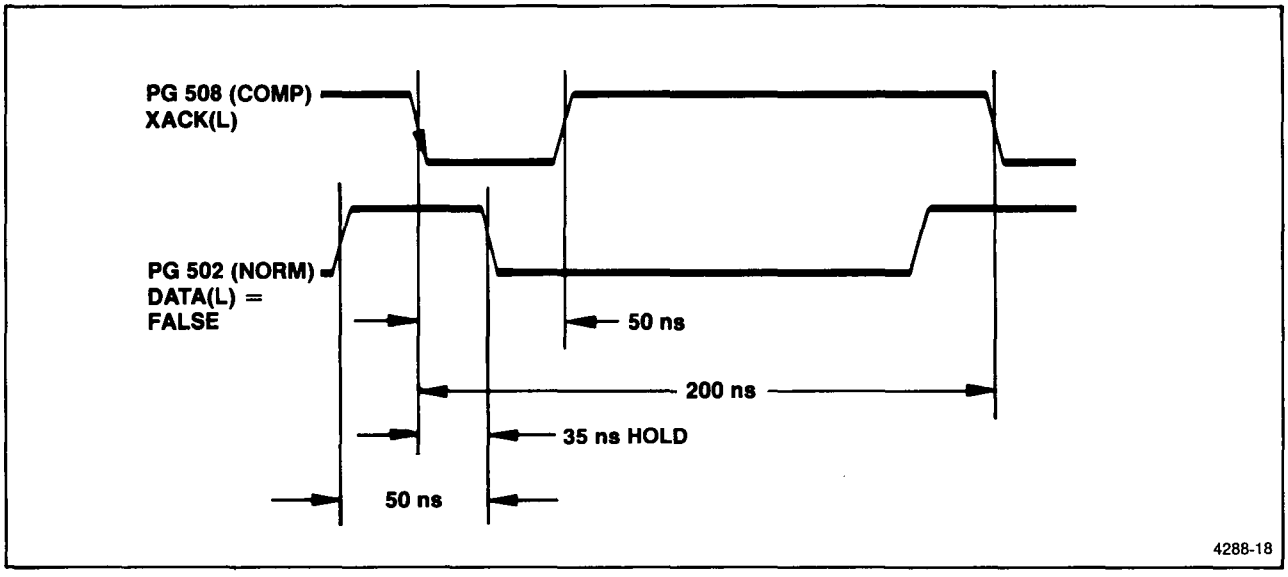

Figure 5-11. DATA hold time (DATA FALSE).

19. Change DATF, the far left DATA bit in the 7D02 program, to "1". Press the START/STOP key.

20. No SLOW CLOCK message should be present on the 7D02 display, and no trigger should be received. Press the STOP key.

21. Repeat the test for DATE. Move the PG 502 and scope probes from pin 60 of P4039 to pin 59 (located on the other side of the board).

22. Change the leftmost bit in the DATA field of the 7D02 program to "X", and enter a "0" in the DATA bit immediately to the right of it.

23. After testing for "0", test for "1" in the DATE bit. Repeat the previous procedure for the remaining data lines (referring to the circuit diagram of the extender for pin numbers), and remember that:

Word Recognizer DATA Bit	PG 502 COMPLEMENT Button	Multibus Data
1	Normal (out)	False
0	Complemented (in)	True

24. Refer to Figure 5-11.

25. If any failures occur, refer to Troubleshooting Error List, Error 15, in the Maintenance and Troubleshooting section of this manual.

26. If you are proceeding to tests 3, 4, or 5, leave all oscilloscope probes and test clips connected.

TEST 3 -- COMMAND SETUP TIME
(MRDC(L), MWTC(L), IORC(L), IOWC(L), & INTA(L))

1. Connect the red EZ Ball hook from the PG 502 to the PM 112 P4039, pin 19 (MRDC(L)).

2. Connect the scope CH 1 probe to P4039, pin 19 (MRDC(L)).

3. Connect the black ground clips from the scope CH 1 and the PG 502 to P4039, pin 1 (GND).

4. Press the PG 502 Complement button (in).

5. Adjust the PG 508 VARIABLE DELAY knob to align the falling edges of the two traces.

6. Confirm that the oscilloscope waveforms are as shown in Figure 5-12.

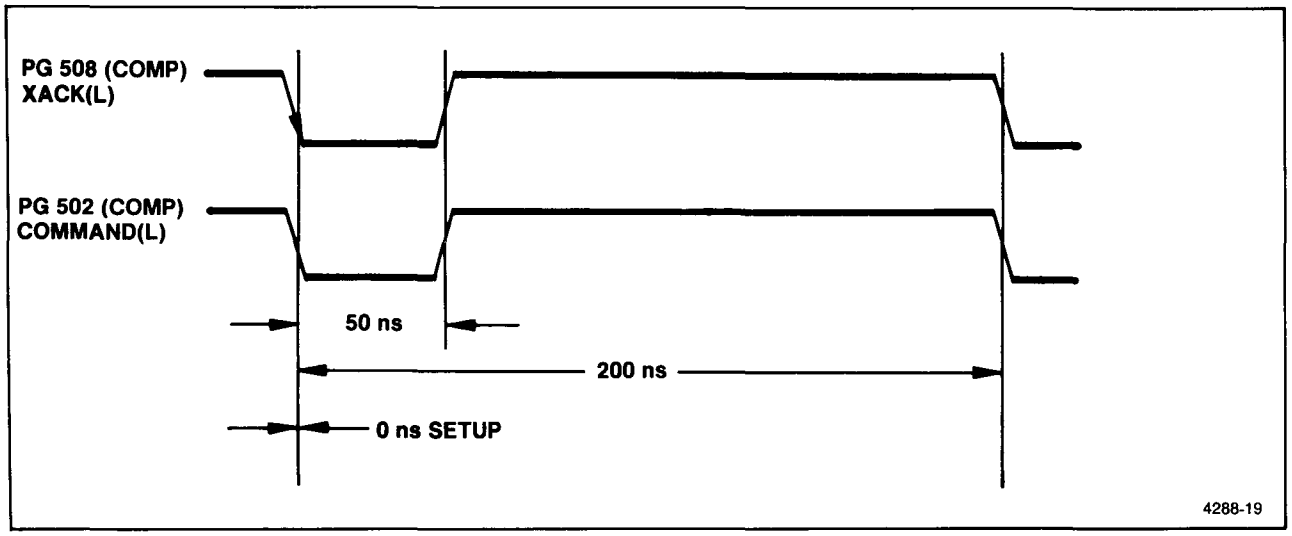

Figure 5-12. Command setup time.

7. Turn the 7D02 power off for five seconds, then on again, to delete any previous programs.

8. Press the following 7D02 keys in sequence: NOT, WD RECOGNIZER, [ ], and TRIGGER.

9. Using the CURSOR and NUMERIC ENTRY keys, change the R/W field to "1", the MEM/IO field to "1", and the INTA+AVAL field to "0", as shown in Figure 5-13.

10. Run the program by pressing the START/STOP key.

11. The program should run without triggering, and without the SLOW CLOCK message appearing on the display screen. This will demonstrate that the 7D02 is seeing the minimum clock pulse width, and is meeting the 0 ns maximum setup time.

12. Stop the program by pressing the START/STOP key.

13. If any failures occur, refer to Troubleshooting Error List, Error 16, in the Maintenance and Troubleshooting section of this manual.

```
 TEST 1
1IF
1 ----------
1¦NOT
1¦WORD RECOGNIZER # 1
1¦DATA=XX XX /BHEN=X
1¦ADDR=XXXXX
1¦R/W=1  MEM/IO=1  INTA+AVAL=0
1¦INTR=X  IPR=X
1¦/INH1=X /INH2=X  EXT. TRIG. IN=X
1¦TIMING WR=X
1 ----------
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    0-STANDARD CLOCK QUAL.
 END TEST 1
                                  4288-20
```

Figure 5-13. 7D02 program for command setup time.

14. Move the red lead from the PG 502 and CH 1 scope probe to P4039, pin 20 (MWTC(L)).

15. Using the CURSOR and NUMERIC ENTRY keys, change the R/W field to "0".

16. Run the program by pressing the START/STOP key.

17. The program should run without triggering, and without the SLOW CLOCK message appearing, as before.

18. Repeat the previous procedure for IORC(L), IOWC(L), INTA(L), and BUSY(L), using the setups summarized in Table 5-4.

19. If any failures occur, refer to Troubleshooting Error List, Error 16, in the Maintenance and Troubleshooting section of this manual.

20. If you are proceeding to Tests 4 or 5, leave all oscilloscope probes and test clips connected.

Table 5-4
COMMAND CHECK CONNECTION SETUP SUMMARY

CYCLE TYPE	R/W	MEM/IO	INTA+AVAL	CMND	P4039 PIN
MRDC(L)	1	1	0	MRD	19
MWTC(L)	0	1	0	MWT	20
IORC(L)	1	0	0	IOR	21
IOWC(L)	0	0	0	IOW	22
INTA(L)	1	0	1	INA	33
BUSY(L)	0	0	1	AVL[a]	17[b]

[a]AVL means bus Available (BUSY not asserted).

[b]Disconnect the grounded jumper lead to J1030 pin 17 when testing the BUSY(L) command line. It must remain grounded for testing all the other command lines (Tests 1-5 only).

TEST 4 -- COMMAND HOLD TIME
(MRDC(L), MWTC(L), IORC(L), IOWC(L), & INTA(L))

1. Connect the red EZ Ball hook from the PG 502 to the PM 112 P4039, pin 19 (MRDC(L)).
2. Connect the scope CH 1 probe to P4039, pin 19 (MRDC(L)).
3. Connect the black ground clips from the scope CH 1 and the PG 502 to P4039, pin 1 (GND).
4. Press the PG 502 Complement button (in).
5. Adjust the PG 508 VARIABLE DELAY knob so that the rising edge of MRDC(L) occurs 35 ns after the falling edge of XACK(L).
6. Confirm that the oscilloscope waveforms are as shown in Figure 5-14.

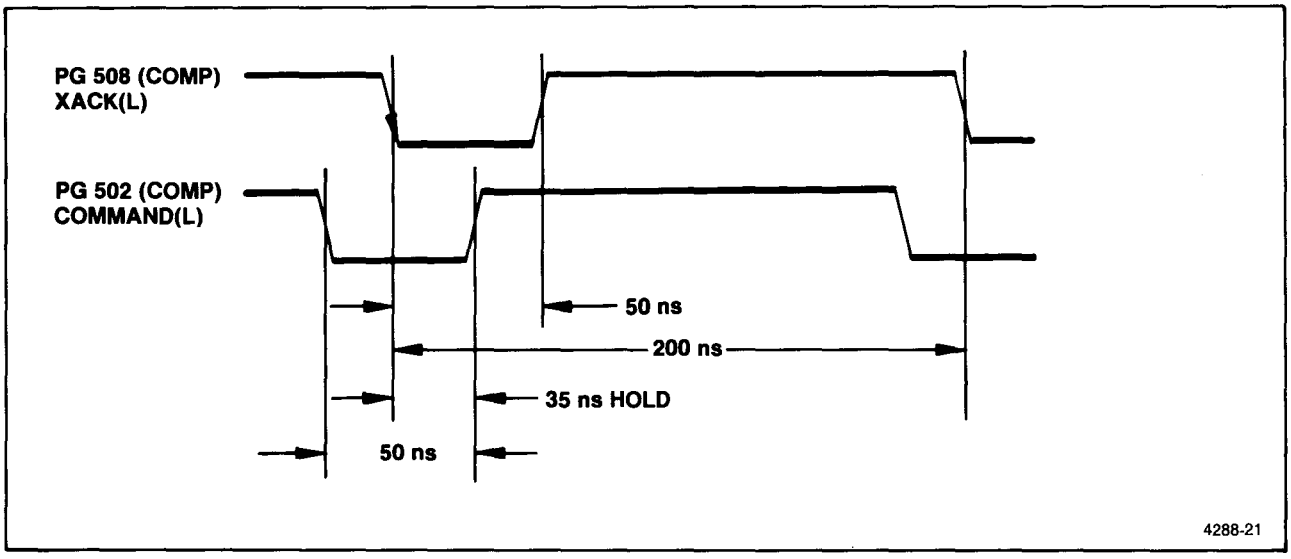

Figure 5-14. Command hold time.

7. Turn power to the 7D02 off for five seconds, then on again, to delete any previous programs.

8. Press the following 7D02 keys in sequence: NOT, WD RECOGNIZER, [ ], and TRIGGER.

9. Using the CURSOR and NUMERIC ENTRY keys, change the R/W field to "1", the MEM/IO field to "1", and the INTA+AVAL field to "0", as shown in Figure 5-15.

```
 TEST 1
1IF
1 ----------
1¦NOT
1¦WORD RECOGNIZER # 1
1¦DATA=XX XX /BHEN=X
1¦ADDR=XXXXX
1¦R/W=1  MEM/IO=1  INTA+AVAL=0
1¦INTR=X  IPR=X
1¦/INH1=X /INH2=X  EXT. TRIG. IN=X
1¦TIMING WR=X
1 ----------
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    0-STANDARD CLOCK QUAL.
 END TEST 1
```

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Figure 5-15. 7D02 program for command hold time (Test 4).

10. Run the program by pressing the START/STOP key.

11. The program should run without triggering, and without the SLOW CLOCK message appearing on the display screen. This will demonstrate that the 7D02 is seeing the minimum clock pulse width, and is meeting the 35 ns maximum hold time.

12. Stop the program by pressing the START/STOP key.

13. If any failures occur, refer to Troubleshooting Error List, Error 17, in the Maintenance and Troubleshooting section of this manual.

14. Move the red lead from the PG 502 and CH 1 scope probe to P4039, pin 20 (MWTC(L)).

15. Using the CURSOR and NUMERIC ENTRY keys, change the R/W field to "0".

16. Run the program by pressing the START/STOP key.

17. The program should run without triggering,, and without the SLOW CLOCK message appearing, as before.

18. Repeat the previous procedure for IORC(L), IOWC(L), INTA(L), and BUSY(L), using Table 5-4.

19. If any failures occur, refer to Troubleshooting Error List, Error 17, in the Maintenance and Troubleshooting section of this manual.

20. Unless proceeding to Test 5, disconnect all oscilloscope probes and test clips from the PG 502 and the PG 508.

TEST 5 -- TIMING OPTION SETUP AND HOLD TIMES

(For Timing Option-equipped 7D02s only.) The following test confirms the ability of the Timing Option to meet the specified performance requirements for Timing Option setup and hold times, while operating synchronously with a clock derived by the PM 112 from XACK(L).

1. Plug the P6451 Timing Option Probe into the 7D02 front panel.

2. Connect the colored leads from the P6451 to the square pin row, in the sequence listed in Table 5-2.

3. Connect the red EZ ball hook from the PG 502 to the P6451 violet lead (bit 7), via the square pin row.

4. Connect the scope CH 1 probe to the P6451 violet lead in the same manner.

5. Connect the black ground clips from the scope CH 1 and the PG 502 to the P6451 white lead (GND), via the square pin row.

6. Set the PG 502 Complement button to NORM (out).

7. Adjust the PG 502 Variable Duration knob for a 45 ns pulse width high.

8. Adjust the PG 508 Variable Delay knob to align the falling edge of the data pulse from the PG 502 with the rising edge of the XACK(L) pulse from the PG 508. Refer to Figure 5-16.

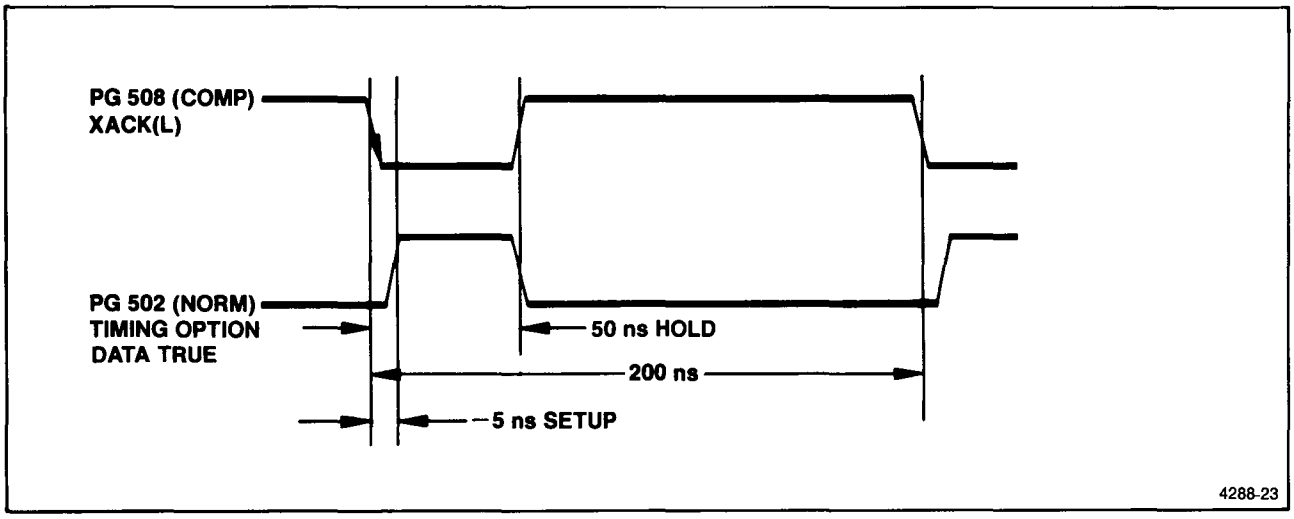


Figure 5-16. Timing Option Data (TRUE) setup and hold time.

9. Turn the 7D02 power off for five seconds, then on again, to delete any previous programs.

10. Press the 7D02 TRIGGER key.

11. Using the CURSOR keys, move the cursor to the TIMING WR box and enter a "1".

12. Move the cursor to the ASYNC box and enter a "0" to specify SYNC.

13. Move the cursor to the msb bit of the timing WORD RECOGNIZER field (far left box), and enter a "0". The program is now set to recognize and trigger if the requirements of the Word Recognizer and the Trigger sections are met.

14. Run the program by pressing the 7D02 START/STOP key.

15. The program should run without triggering, and without indicating SLOW CLOCK. This will demonstrate that the 7D02 is seeing the minimum clock pulse width, and is meeting the -5 ns setup and 50 ns hold time requirements.

16. Stop the program by pressing the 7D02 STOP key.

17. If any failures occur refer to the Troubleshooting Error List, Error 18, in the Maintenance and Troubleshooting section of this manual.

18. Press the PG 502 COMPLEMENT button (in). Verify that the data pulse out of the PG 502 starts 5 ns after the falling edge of XACK(L) (from the PG 508), and ends 50 ns after the falling edge of XACK(L). Refer to Figure 5-17.

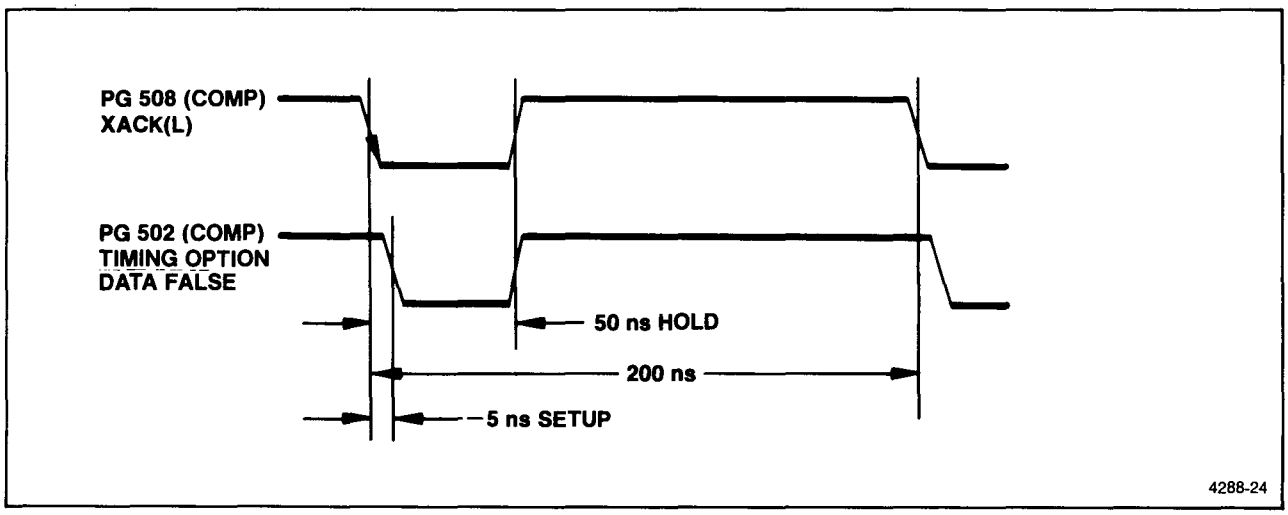


Figure 5-17. Timing Option Data (FALSE) setup and hold time.

19. Change the msb bit in the WORD RECOGNIZER field to "1". Press the START/STOP key.

20. Again, there should be no trigger and no SLOW CLOCK message.

21. Stop the 7D02 program.

22. Repeat the test for the next bit to the right of the msb. Move the PG 502 output and CH 1 scope probe from the violet wire to the blue wire.

23. Change the 7D02 program. Return the leftmost (msb) bit of the timing option word recognizer to "X", and change the next bit right to "0". Press the START/STOP key.

24. Again, there should be no trigger and no SLOW CLOCK message.

25. Stop the 7D02 program.

26. After testing for "0" in the timing option word recognizer bit 6, repeat steps 17-20 of the previous procedure for a "1" in DATA bit 6.

27. Repeat steps 13 through 26 of this procedure to test the remaining timing option data lines 5 through 0. Use Table 5-2 and the following guide:

Timing Word Recognizer	PG 502 COMPLEMENT Button	Timing Option Data
0	Normal (out)	True
1	Complemented (in)	False

28. Refer to Figures 5-16 and 5-17.

29. If any failures occur, refer to Troubleshooting Error List, Error 18, in the Maintenance and Troubleshooting section of this manual.

30. Switch off power to the 7D02 and test equipment. Disconnect all equipment and jumper leads.

TEST 6 -- SELF-TEST CLOCK FREQUENCY ACCURACY

This test checks the ability of the self-test clock circuitry to operate within the 20 MHz ± 5% frequency accuracy specification. It uses its own test equipment setup procedure.

If you use a frequency counter other than the DC 504, modify the following procedure to suit the requirements of the actual frequency counter used.

1. Insert the PM 112 logic analyzer plug into the 7D02.
2. Plug the DC 504 Counter/Timer into the TM 503 mainframe. Unplug unused pulse generators as required to make room.
3. Set the DC 504 FUNCTION switch to Frequency, 1 kHz Resolution. Set the SOURCE switch to EXT.
4. Connect an oscilloscope probe to the INPUT of the DC 504.
5. Power up the TM 503 mainframe to power the DC 504.
6. Move the strap on jumper W3085 on the PM 112 to the NORM position.
7. Remove the strap on W4075.
8. Connect the probe tip from the DC 504 to W4075, pin 1.
9. Connect the ground clip from the frequency counter probe to TP4085 (GND).
10. Turn on the 7D02 power.
11. Adjust the DC 504 TRIGGER LEVEL knob for a stable reading.
12. Confirm that the DC 504 indicates a frequency of between 19 MHz and 21 MHz.
13. If the frequency is not within this range, refer to Troubleshooting Error List, Error 19, in the Maintenance and Troubleshooting section of this manual.
14. Replace the strap on W4075 in the INT position.
15. Turn off and disconnect all test equipment.

MAINTENANCE AND TROUBLESHOOTING

MAINTENANCE

REPAIR

The PM 112 requires no periodic maintenance. Properly handled and cared for, your personality module will give dependable service for many years. However, should repair service be needed at any time, Tektronix provides complete instrument repair at local Field Service Centers and at the Factory Service Center. Contact your local Tektronix Field Office or representative for further information.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be ordered through your local Tektronix Field Office or representative. Many of the standard electronic components may also be available from a local source in your area. However, before you purchase or order a part from a source other than Tektronix, Inc., please check the Replaceable Electrical List and the Replaceable Mechanical Parts List for the proper value, rating, tolerance, and description.

ORDERING PARTS

When ordering replacement parts from Tektronix, it is important that all of the following information be included to ensure receiving the proper parts.

1. Instrument type (include modification or option numbers).
2. Instrument serial number (located on a stamped plastic tag, affixed to the PM 112 circuit board).
3. A description of the part (if electrical, include component number from the Replaceable Electrical Parts List).
4. The Tektronix part number.
5. The quantity of each part desired.

CLEANING INSTRUCTIONS

This instrument should be cleaned as often as the operating environment requires. Accumulation of dirt on components acts as an insulating blanket and prevents efficient heat dissipation. This condition can cause overheating and component breakdown.

Use a jet of dry, low pressure air and a soft brush to remove dust from the circuit board. After soldering or when otherwise required, use isopropyl alcohol with a soft cloth or cotton swab to remove flux, resin, and dirt. As the board is cleaned, make certain that the square pins are not contaminated with residual flux, to prevent impairing electrical contact.

REMOVAL OF INSULATING SHIELD

To access the underside of the circuit board you must remove the personality module insulating shield. If it becomes necessary to do so, as when troubleshooting or soldering, find a clean open space on a table and be sure that screws and other small parts are placed where they will not be lost.

CAUTION

Always turn off the mainframe power before connecting or disconnecting any personality module. Observe static precautions at all times when disassembling or repairing the PM 112.

To remove the insulating shield:

1. Remove the screw, nut, and lock washer in each corner of the circuit board. Store them in a safe place.
2. Remove and store the insulating shield and its spacers.
3. Reverse the above procedure for reassembly.

LOGIC ANALYER PLUG DISASSEMBLY

To disassemble the logic analyzer plug:

1. Remove the four screws holding the logic analyzer plug together with a 3/32" Allen wrench.
2. Pull the halves of the plug apart and remove the cable hold-down clamp.
3. Remove the circuit board by lifting up on the cable end and sliding the board out of the plastic hold-down flanges.
4. Reverse the above procedure to reassemble the logic analyzer plug.

TROUBLESHOOTING

OVERVIEW

Several methods are available to the service technician for localizing and identifying a faulty circuit in the PM 112. Nearly all PM 112 failure modes can be detected by the 7D02 Diagnostic Module 9 (PER. MOD. - SYSTEM). They can be identified by Module 9 Subtest error codes, and by the Self-Test Acquisition Check.

Subtest 7 error codes have directly corresponding numbers and procedures in the Troubleshooting Error List.

Because the PM 112's circuitry is approximately 55% self-test and only 45% acquisition, it cannot be assumed that a diagnostics failure is due to faulty acquisition circuitry. The Acquisition vs. Self-Test Check, detailed in the Performance Checks section, is an efficient way to determine which portion of the PM 112's circuitry is at fault. To perform this test, you must have access to the optional equipment listed in Table 5-1: a known-good PM 112 and a second 7D02 Logic Analyzer with mainframe.

The Self-Test Acquisition Check, also located in the Performance Checks section, will detect improperly encoded command and interrupt priority lines, and will reveal stuck address and data lines. By selecting binary radix (using Format mode) for display of the faulty address or data fields, you can observe each bit in the field (and its corresponding line) individually.

Locate faulty components using the Troubleshooting Error List and/or Circuit Diagrams and Illustrations. Replace suspected components and run the Diagnostic Monitor (located in the Performance Checks section), to confirm that the PM 112 is now functioning properly.

Should problems remain with the PM 112, refer to the word recognizer Control Line Check and the Clock Qualification Check located in the Performance Checks section. These checks are in the Extended Diagnostics subsection, and are complete with references to error numbers and procedures in the Troubleshooting Error List.

SUBSTITUTION METHOD

If another 7D02 Logic Analyzer and/or PM 100 Series Personality Module is available, try substituting and running the diagnostics again. In this way you can immediately determine whether the PM 112 or the 7D02 being used is at fault.

CAUTION

A 7D02 power supply that is seriously out of tolerance could damage a personality module. If you suspect power supply problems, check the 7D02 before connecting a personality module.

DIAGNOSTIC MONITOR

Power-up diagnostic routines are built in and automatically run each time the 7D02 Logic Analyzer/PM 112 Personality Module system is powered on. If a failure is detected, the 7D02 will display the POWER-UP VERIFICATION test results. This display offers you the choice between beginning normal operation (by pressing the START key) or displaying the DIAGNOSTIC MONITOR MENU (by pressing the X key).

Diagnostic Module subtests 0 (TEST ALL), 9 (PER.MOD.-SYSTEM), and B (TIMNG OPTION) will pass only if the PM 112 is configured in the self-test mode. Self-test configuration is described in the Preliminary Setup procedure located in the Performance Checks section. Following the Preliminary Setup you will find procedures for running Diagnostic Modules 9 (PER. MOD.-SYSTEM) and B (TIMING OPTION).

Refer to Diagnostic Module 9 and Diagnostic Module B in this section of the manual for explanation of Diagnostic Module subtests and their failure codes. Refer to the 7D02 Service manual for additional diagnostics information.

Diagnostic Module 9 (PER. MOD.-SYSTEM)

Diagnostic Module 9 contains 7 subtests. Subtests 1, 2, 3, 4, and 7 are personality module specific, and are discussed in the following subsection. Subtests 5 and 6 are the same for all personality modules; refer to the 7D02 Service Manual for more information.

Subtests 1, 2, 3, 4, and 7 require that the PM 112 be configured in the self-test mode. Refer to the Preliminary Setup in the Performance Checks section for connection instructions, and to the procedure following it for test instructions.

Subtest 1. This test reads a byte at address 3:E010 in the personality module EPROM to determine the EPROM length. This indicates the location (E7FC) of the EPROM trailer. The value at E7FC is compared to the value in the next byte, E7FD, which should be its complement. If the two bytes are not complementary, a failure message is displayed as follows:

```
1    FAIL    3E7FD-X
(indicating incorrect value @ 3:E010)
```

where X is the first non-complementary bit after the two bytes are compared on a bit-by-bit basis.

If the part number is correct, the following message is displayed:

```
1    PASS    1566-00
```

Subtest 2. This test calculates a 16-bit checksum on the EPROM. If the checksum does not match the expected value, the calculated value is reported as the following failure message:

```
2    FAIL    XXXX
```

where XXXX = the calculated value.

Subtest 3. This test assigns the following program to the 7D02 State Machine:

```
IF WR1  TRUE
THEN TRIGGER TIMING AND MAIN
```

The 7D02 Acquisition Memory board is set for zero delay. All clock qualifiers are disabled, and the state clock is defined as the falling edge of the PM 112 CLK signal by data stored in the personality module EPROM. After all setups are complete, a DISPLAY command is sent and the 7D02 slow clock detector is checked. A slow clock results in the following failure message:

```
3    FAIL    0FF60-1
(indicating slow or no clock)
```

This can be caused by an erratic or missing clock signal from the personality module. Anything that generates or transfers the test clock to the 7D02 should be checked.

If the clock appears to be running, the 7D02 reads the personality module EPROM to determine how long to wait for a trigger to occur. Then a STORE command is sent. After waiting the specified amount of time (2 ms), the activity monitor on the Acquisition Memory board is examined to see if the Main Section has triggered

and returned to DISPLAY mode. If the Main Section is still in STORE mode, the following failure message is generated:

3 **FAIL** **2E803-7**
(indicating Main Section failed to trigger)

Failure to trigger can be caused by failure of the personality module to generate and/or acquire the word recognizer 1 (WR1) value (refer to Table 6-1).

Table 6-1
PROGRAMMED WORD RECOGNIZER VALUES

	WR 1	WR 2	WR 3	WR 4
DATA*	AAAA	7E55	AFAA	5555
ADDRESS*	AAAAA	55555	AAAAA	55555
INTR* (A23)	1	1	0	1
IPR (A22-A20)	101	010	111	100
/INH2 (C5)	0	1	1	1
/INH1 (C4)	1	0	1	1
/BHEN (C3)	0	1	1	0
INTA+AVAL (C2)	0	0	1	0
MEM/IO (C1)	0	1	0	1
R/W (C0)	0	1	1	1
Cycle Type	I/O Write	Mem. Read	Int. Ack.	Mem. Read

*The word recognizer values specified for the DATA, ADDRESS, and INTR fields are inverted before being supplied to the diagnostics (they are actually active low in the the hardware, inverted by firmware in displays).

Subtest 4. This test involves all four of the 7D02 word recognizers, the two 7D02 Counters, the 7D02 State Machine, and the 7D02 Acquisition Memory.

Subtest 4 programs the 7D02 word recognizers in the same way as described for Subtest 3 (refer to Table 6-1). Also, the test in effect programs the 7D02 State Machine as follows:

```
1IF WR1 THEN [GO TO 2, RESET CTR 1 AND 2]

2IF WR2 THEN [INCR CTR 1, GO TO 3]
2   ELSE INC. CTR 1

3IF WR3 THEN [INCR CTR 2, GO TO 4]
3   ELSE INC. CTR 2

4IF WR4 THEN TRIGGER MAIN
```

All cycles are qualified except the trigger; therefore all cycles are stored except the trigger cycle. The clock qualifiers are the same as for subtest 3 in that all clock qualifiers are disabled, and the state clock is defined as the falling edge of the PM 112 CLK signal.

After all steps are complete, a DISPLAY command is sent and the slow clock detector is checked. A slow clock indication results in the following failure message:

4 FAIL 0FF60-1
(indicating slow or no clock)

This can be caused by an erratic or missing personality module clock. Anything in the personality module that generates or transfers the test clock should be checked.

If the clock appears to be running, the personality module EPROM is read to determine how long to wait for a trigger. Then, a STORE command is sent. After waiting 2 ms, the activity monitor on the 7D02 Acquisition Memory board is examined to see if the Main Section has triggered and returned to DISPLAY mode. If it is still in the STORE mode, the following failure message is generated:

4 FAIL 2E803-7
(indicating Main Section failed to trigger)

Failure to trigger can be caused by failure of the personality module to generate and/or acquire any one of the four word recognizer values.

The next part of the test is a check of the counters. This verifies that the personality module's clock and self-test generator are working properly. First the msb (most significant bit) of Counter 1 is read and compared with the expected value stored in the personality EPROM. If it matches, the lsb (least significant bit) is compared. Then Counter 2 is checked in the same way. If any byte fails to match exactly, the appropriate error message is displayed as follows:

4 FAIL 1E202-X
(indicating CTR 1 msb bit X is wrong)

4 FAIL 1E203-X
(indicating CTR 1 lsb bit X is wrong)

4 FAIL 1E302-X
(indicating CTR 2 msb bit X is wrong)

4 FAIL 1E303-X
(indicating CTR 2 lsb bit X is wrong)

Any of these messages can be the result of a faulty clock signal or self-test generator (incorrect pattern).

The Main Acquisition Memory and Expansion Option Acquisition Memory are checked by summing all bytes between 2:E000 and 2:E3FF in the Main Acq. Memory, and all bytes between 2:E400 and 2:E7FF in the Exp. Opt. Acq. Memory. The checksums are compared with the expected values stored in the personality EPROM. Main Acq. Memory and Exp. Opt. Acq. Memory checksum failures result, respectively, in the following failure messages:

4 FAIL 3E035-X
(indicating one or more dead or intermittent channels among any of the personality module's outputs except A23-A16 and D15-D8.)

4 FAIL 3E036-X
(indicating one or more dead or intermittent channels among A23-A16 and D15-D8.)

Subtests 5 and 6. Subtests 5 and 6 are intended to test only the 7D02, and are described in the 7D02 Service Manual.

Subtest 7. This test checks the clock qualifier lines C9-C4 on the 7D02 front end board.

The test programs the 7D02 State Machine with the following test sequence:

```
1IF WR1 THEN TRIGGER MAIN
1   ELSE GO TO 1
```

C9-C4 are set equal to XXXXXX.

Word Recognizer 1 was programmed in an earlier subtest to a value specified by the personality module EPROM (refer to Table 6-1). This test uses each of the control lines in turn to qualify out the value to which Word Recognizer 1 has been programmed.

If the control line works correctly, the state clock that occurs with Word recognizer 1 will be inhibited and the State Machine will not see the word recognizer output. A PASS condition, then, is indicated by the failure of the Main Section to trigger. The processor waits 2 ms to trigger.

Six bytes in the personality module EPROM specify the value to be sent to the 7D02 front end to inhibit state clocks when word recognizer 1 occurs for each of the six control lines. The following sequence is repeated six times, once for each control line or until a failure occurs:

- Read value from personality module EPROM.
- Write value to front end latch.
- Send STORE command.
- Wait specified length of time.
- Check activity monitor on Acquisition Memory board.
- If in DISPLAY mode, print FAIL and stop.

If Subtests 3 and 4 pass, it is safe to assume C9-C4 are operating correctly.

The Subtest 7 failure messages should be interpreted as follows:

7 **FAIL 3E039**
(C4 didn't inhibit trigger - Error 13[a])

7 **FAIL 3E03A**
(C5 didn't inhibit trigger - Error 12[a])

7 **FAIL 3E03B**
(C6 didn't inhibit trigger - Error 11[a])

7 **FAIL 3E03C**
(C7 didn't inhibit trigger - Error 10[a])

7 **FAIL 3E03D**
(C8 didn't inhibit trigger - Error 9[a])[b]

7 **FAIL 3E03E**
(C9 didn't inhibit trigger - Error 8[a])[b]

[a]Refer to Troubleshooting Error List in this section.
[b]These two failure codes will not be indicated appropriately when looping mode is enabled.

Subtest 8. The 7D02 does not perform Subtest 8 with the PM 112.

Diagnostic Module B (TIMING OPTION)
(Timing Option-equipped 7D02s only)

This module consists of 3 subtests. Subtests 1 and 2 are the same for every personality module. Refer to the 7D02 Service Manual for more information. Subtest 3 is personality module specific.

This test requires that the P6451 Timing Option Probe be connected in order to carry the stimulus from the self-test circuitry. Subtest 3 is not run during the POWER-UP VERIFICATION.

The timing option word recognizer is set to trigger on the occurrence of A0H.

Subtest 3. The 7D02 State Machine is in effect programmed as follows:

```
1IF TIMING OPTION WR=A0H
1THEN GO TO 4

4IF TIMING OPTION WR=A0H
4THEN TRIGGER TIMING AND MAIN
```

The timing option memory address counter is set to 0. All word recognizers, except the timing option, are set to X (don't care).

The slow clock indicator is checked for the presence of a clock. If none is detected, the following failure is displayed.

```
3    FAIL    0FF60-1
(slow or no clock detected)
```

If the clock appears to be running, a byte is read from the personality module EPROM that specifies how long to wait for the trigger. Then a STORE command is sent. After waiting the specified amount of time (2 ms), the 7D02 Acquisition Memory activity monitor is examined to see if the Main Section has triggered. If it hasn't, the following failure is reported.

```
3   FAIL    2E803-7
(indicating Main Section failed to trigger)
```

This can be caused by the self-test circuitry not generating the A0H value or the P6451 not transferring data properly.

If the trigger occurred, the timing option memory address counter is examined to determine the last data location and the trigger location is calculated. The value saved in the trigger location is then compared with the value in the personality module EPROM that was used to program the timing option word recognizer. If the two are not complementary (data inverted), the following failure is reported.

3 **FAIL 3E03F-X**
(indicating trigger value incorrect)

where X is the first offending bit.

This can be caused by a faulty timing relationship between the clock and the data.

If the trigger test passes, the timing option acquisition memory at address 2:F000 - 2:F0FF is checksummed (with the exception of one data byte which is Xs), and the result compared with the expected value stored in the personality module EPROM. If the values are not the same, the following failure is reported.

3 **FAIL 3E040-X**
(checksum error 2:F000 - 2:F0FF)

where X is the first bit that didn't match.

This can be caused by the PM 112 self-test circuitry not generating the correct pattern all the time, or an intermittent failure in the P6451.

JUMPER PLUGS AND TEST POINTS

The following Table 6-2 provides the signal name and number of the jumper plugs and test points located on the PM 112 circuit board.

Table 6-2
PM 112 JUMPER PLUGS AND TEST POINTS

Jumper Plug or Test Point	Board Location	Common Name
TP1010	A1	GND
TP1025	A1	/HALT SUT
TP4075	D2	EXT CLK IN
TP4085	D2	GND
W3011	A2	8 8/16
W3015	A2	PAR SER
W3085	D2	TEST NORM (mode)
W4075	C2	TEST CLK
TP1027-1	B1	CCLK(L)[a]
" "-2	""	XACK(L)[a]
-3		BREQ(L)[a]
" "-4	""	BUSY(L)[a]
-5		BPRO(L)[a]
" "-6	""	BCLK(L)[a]
TP4079-13	D3	PFSR(L)[b]
-17		PFSN(L)[b]
" "-19	""	PFIN(L)[b]
-20		MPRO(L)[b]
" "-27	""	PAR1(L)[b]
-28		HALT(L)[b]
" "-29	""	PAR2(L)[b]
-30		WAIT(L)[b]
" "-31	""	PLC(H)[b]
-32		ALE(H)[b]
" "-36	""	BD RESET(L)[b]
-38		AUX RESET(L)[b]
TP4079-55	D3	ADR16(L)[b]
-56		ADR17(L)[b]
" "-57	""	ADR14(L)[b]
-58		ADR15(L)[b]

[a] Multibus signals from P1 (P4039) connector.

[b] Multibus signals from P2 (P4079) connector.

TROUBLESHOOTING ERROR LIST and PROCEDURES

When performance checks or troubleshooting detect a failure, reference notes will direct the service technician to a specific error number listing. This list may in turn direct the technician to a specific procedure to isolate the problem.

This error list assumes the 7D02 is known to be operating correctly, the personality module has been properly connected, and all power supplies are within their specified tolerances.

Table 6-3
PM 112 TROUBLESHOOTING ERROR LIST

Error No.	Symptom	Possible Causes/Suggestions
1	Diagnostic Module 9 (PER. MOD. - SYSTEM) Fails	Run Extended Diagnostics tests (located in Performance Checks section). See Error numbers referenced in Extended Diagnostics. Test and repair as suggested for particular Error number. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
2	Diagnostic Module B (TIMING OPTION) Fails	Go to Troubleshooting Procedure 2.
3	SELF-TEST ACQUISITION CHECK Fails	If possible (Optional Test Equipment is available), run Acquisition vs. Self-Test Check, located in Performance Checks section, to determine whether acquisition or self-test circuitry is faulty. Rerun Self-Test Acquisition Check, using the 7D02 FORMAT mode to change address and data field displays to binary radix. Lines stuck high or low are now easily identified. Consult circuit diagrams to locate corresponding parts. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.

Table 6-3 (cont.)
PM 112 TROUBLESHOOTING ERROR LIST

Error No.	Symptom	Possible Causes/Suggestions
4	Does not trigger on correct command	Command Encoder or Self-Test Command Generator faulty. Check CI0-CI2 circuitry: **Acquisition** -- U4021, U2021; **Self-Test** -- U4061, U4065, U3071, U2065, U2071, U4071, U3075, U4079, Q4083, U4015, U2031. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
5	Does not trigger on 8- or 16-bit cycles when appropriate	BHEN(L) buffers or Self-Test Generator faulty. Check CI3 circuitry: **Acquisition** -- U4025, U2031; **Self-Test** -- U3025, U2065, U2071, U3071, U4071, U3075, U4079, U4015, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
6	Does not trigger on INH1(L) low or high when appropriate	INH1(L) buffers or Self-Test Generator faulty. Check CI4 circuitry: **Acquisition** -- U4025, U1015; **Self-Test** -- U3025, U2065,U2071, U3071, U4015, U4071, U3075, U4079, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
7	Does not trigger on INH2(L) low or high when appropriate	INH2(L) buffers or Self-Test Generators faulty. Check CI5 circuitry: **Acquisition** -- U4025, U1015; **Self-Test** -- U3025, U2065,U2071, U3071, U4015, U4071, U3075, U4079, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
8	Does not store all or does not store any AVL cycles when appropriate	BUSY buffers or Self-Test Generator faulty. Check CI9 circuitry: **Acquisition** -- U2031, U4025, DL3081, Q2087, Q2084, Q2085, Q2081, Q2083, Q2086, U2021; **Self-Test** -- U4061, U2031, U3071, U3075, U2065, U4071, U2071, U4079, U4015, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.

Table 6-3 (cont.)
PM 112 TROUBLESHOOTING ERROR LIST

Error No.	Symptom	Possible Causes/Suggestions
9	Does not store all or does not store any ACLO cycles when appropriate	ACLO(L) buffers or Self-Test Generator faulty. Check CI8 circuitry: **Acquisition** -- U2031, U1021, U4025, U1015; **Self-Test** -- U4015, U3025, U2065, U2071, U3071, U4071, U3075, U4079, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
10	Does not store all or does not store any LOCK(L) cycles when appropriate	LOCK(L) buffers or Self-Test Generator faulty. Check CI7 circuitry: **Acquisition** -- U4025, U1015, U2031, U1021; **Self-Test** -- U3025, U2065, U2071, U3071, U4071, U3075, U4079, U4015, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
11	Does not store all or does not store any CBRQ(L) cycles when appropriate	CBRQ(L) buffers or Self-Test Generator faulty. Check CI6 circuitry: **Acquisition** -- U2031, U1021, U4025, U1015; **Self-Test** -- U4015, U3025, U2065, U2071, U3071, U4071, U3075, U4079, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
12	Does not store all or does not store any INH2(L) cycles when appropriate	INH2(L) buffers or Self-Test Generator faulty. Check CI5 circuitry: **Acquisition** -- U4025, U1015, U2031, U1021; **Self-Test** -- U3025, U2065, U2071, U3071, U4071, U3075, U4079, U4015, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.

Table 6-3 (cont.)
PM 112 TROUBLESHOOTING ERROR LIST

Error No.	Symptom	Possible Causes/Suggestions
13	Does not store all or does not store any INH1(L) cycles when appropriate	INH1(L) buffers or Self-Test Generator faulty. Check CI4 circuitry: **Acquisition** -- U4025, U1015, U2031, U1021; **Self-Test** -- U3025, U2065, U2071, U3071, U4071, U3075, U4079, U4015, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
14	DATA Setup Time failure	Data buffers too slow or dead; XACK(L) delay too fast, or dead; Self-Test Generator faulty. Check **DATA buffers:** U4051, U2055, U4045, U1045, U4025. **XACK(L) delay:** U4021, DL3081, Q2081, Q2083, Q2084, Q2085, Q2086, Q2087. **Self-test:** U3045, U2061, U3065, U3051, U3061, U3079, U4015, U2031, U4075, U2071, U2065, U3071, U4071, U3075, U4079, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
15	DATA Hold Time failure	Data buffers too fast or dead; XACK(L) delay too slow or dead; Self-Test Generator faulty. Check **DATA buffers:** U4051, U2055, U4045, U1045, U4025. Check **XACK(L) delay:** U4021, DL3081, Q2081, Q2083, Q2084, Q2085, Q2086, Q2087. **Self-Test:** U3045, U2061, U3065, U3051, U3061, U3079, U4015, U2031, U4075, U2071, U2065, U3071, U4071, U3075, U4079, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.

Table 6-3 (cont.)
PM 112 TROUBLESHOOTING ERROR LIST

Error No.	Symptom	Possible Causes/Suggestions
16	COMMAND Setup Time failure	COMMAND buffer or encoder too slow or dead; XACK(L) delay too fast or dead; Self-Test Generator faulty. Check **buffers and encoder:** U4021, U2031, U2021. **XACK(L) delay:** U4021, DL3081, Q2081, Q2083, Q2084, Q2085, Q2086, Q2087. **Self-Test:** U4061, U4065, U3071, U2065, U2071, U4071, U3075, U4079, U4015, U2031, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
17	COMMAND Hold Time failure	COMMAND buffer or encoder too fast or dead; XACK(L) delay too slow or dead; Self-Test Generator faulty. Check **buffers and encoder:** U4021, U2031, U2021. **XACK(L) delay:** U4021, DL3081, Q2081, Q2083, Q2084, Q2085, Q2086, Q2087. **Self-Test:** U4061, U4065, U3071, U2065, U2071, U4071, U3075, U4079, U4015, U2031, Q4083, Q4071. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
18	TIMING OPTION Setup and/or Hold Time failure	XACK(L) delay too fast or dead; Timing Option Self-Test Generator faulty. Check **XACK(L) delay:** U4021, DL3081, Q2081, Q2083, Q2084, Q2085, Q2086, Q2087. **Self-Test:** U1021, U2031, U4021, U4025, U1045, U4045, U3045, U2061, U3065, U4075, U2031, U2071, U4015, U2065, U3071, U4071, U3075, U4079, U4061, U4065, U3025, Q4083, Q4071, Q4085. Replace suspected parts and retest. If unsuccessful, go to Troubleshooting Procedure 1.
19	Self-Test Clock Frequency not as specified	Slow or dead transistor; inductor or capacitors out of tolerance. Check Q4083, U4079, L4083, C4081, C4083, and -15V power supply. Replace suspected parts and retest. If unsuccessful, go to Trouble-shooting Procedure 1.

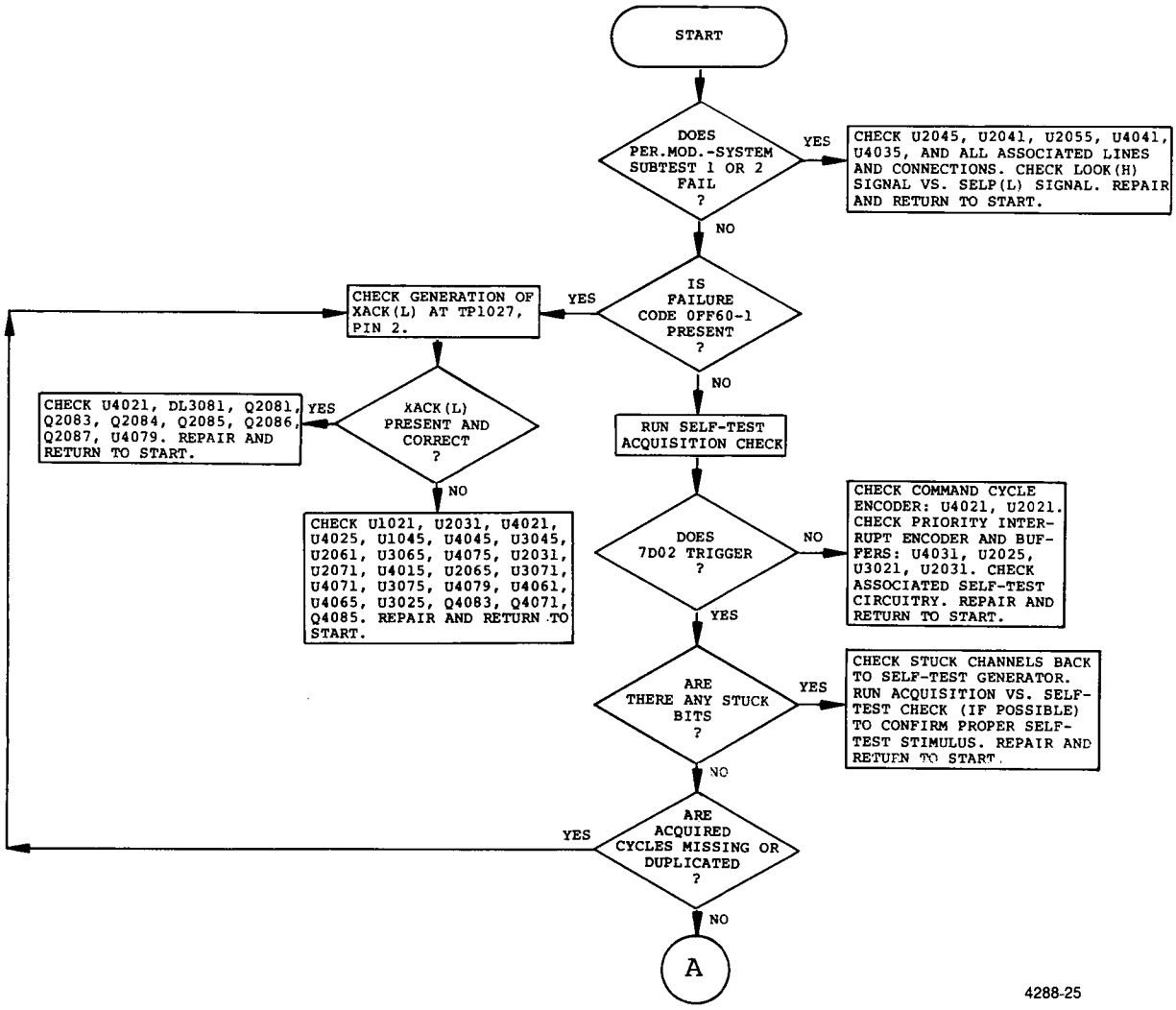


Figure 6-1. Troubleshooting Procedure 1.

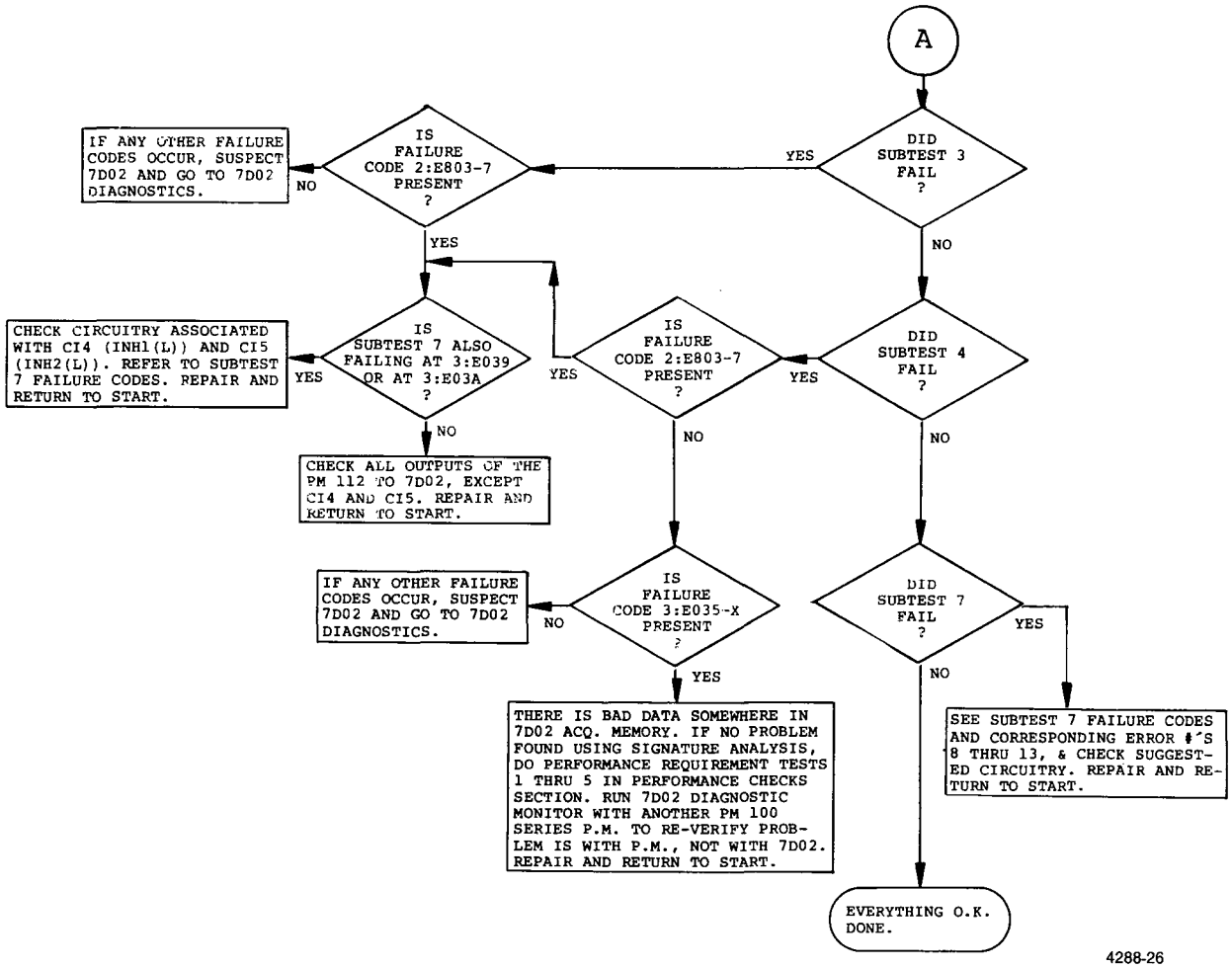


Figure 6-1. Troubleshooting Procedure 1 (continued).

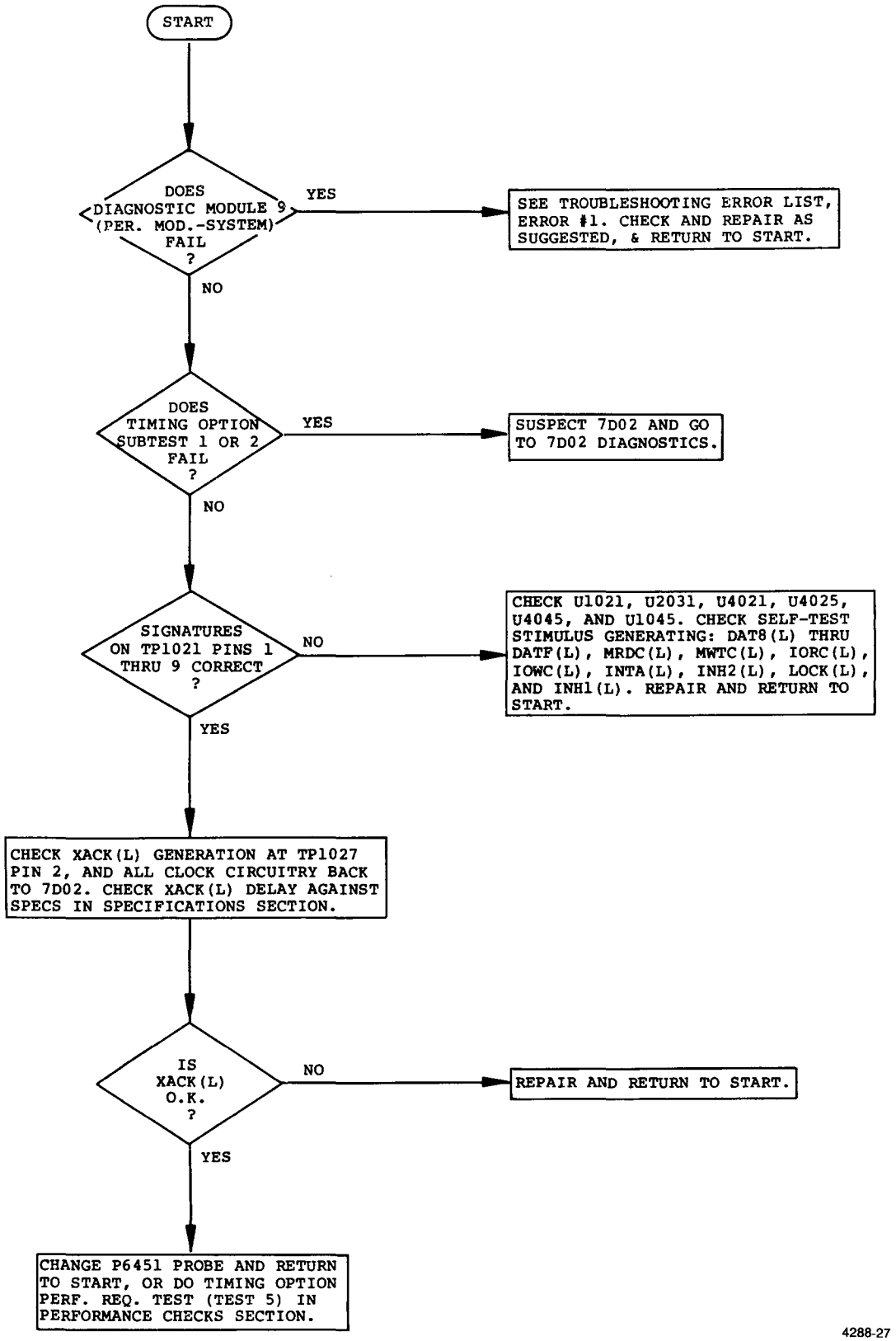


Figure 6-2. Troubleshooting Procedure 2.

SIGNATURE ANALYSIS

The Signature Analysis Procedure allows the service technician to check the condition of a logic circuit node in the PM 112 with respect to a specific operating time window.

Troubleshooting With Signature Analysis Procedure

A signature is a four-digit hexadecimal number representing time-dependent logic activity during a specified measurement interval (referred to as a window) for a given circuit node. Any change in the behavior of this node (even a transition that occurs one clock cycle late) will produce a different signature, indicating a probable malfunction in the circuit.

The signal that causes the node to produce a signature is the stimulus. In signature analysis, the stimulus is supplied by the personality module itself when it is in the self-test mode. This way, a controlled environment is created wherein selected portions of the circuit are tested independently, while maintaining full dynamic operation.

Preliminary Setup

1. Use the Sony/Tektronix 308 Data Analyzer with P6451 probe.
2. Leave the mainframe power off. Insert the personality module logic analyzer plug into the logic analyzer.
3. Set all PM 112 jumpers to their default pin 1 positions (indicated by tick marks).
4. Set jumper W3085 to the TEST position.
5. Connect the signature analyzer probe clock lead to U4071, pin 2.
6. Connect the signature analyzer start/stop leads to U4061, pin 15.
7. Switch the signature analyzer power on.
8. Set the START triggering to falling edge.
9. Set the STOP triggering to rising edge.
10. Set CLOCK to rising edge.
11. Switch on logic analyzer power while holding down any 7D02 key (except X and START). This will force the 7D02 into the diagnostic mode.

12. Press the 7D02 X key to obtain a display of the diagnostic menu.

13. Press the F key to select SIGNATURE EXERCISER MENU.

14. Press the 7 key to select PER.MOD.-SYSTEM.

15. The serial signature probe ground clip must be connected to TP4085, TP1010, or another grounded point on the PM 112. The following signature table lists the PM 112 signatures.

NOTE

The signature for +5 V = 9FA8, and the signature for GND = 0000. An asterisk (*) denotes an unstable signature.

Table 6-4
PM 112 SIGNATURES

U1015	U1021	U1045	J1075
1) 0000	1) UFP7	1) 62HA	1) 0000
2) 93H7	2) 2A41	2) PC5A	2) 0000
3) 62HA	3) 8294	3) F951	3) 0000
4) AHU5	4) C438	4) PC5A	4) 0000
5) 19UH	5) 33P6	5) 5H33	5) P12U
6) *	6) 93H7	6) PC5A	6) 6AC7
7) 19UH	7) 1933	7) 78HC	7) P12U
8) *	8) 93H7	8) PC5A	8) 6AC7
9) 9FA8	9) C07P	9) 78HC	9) P12U
10) 0000	10) 0000	10) 0000	10) 6AC7
11) 9FA8	11) 1C69	11) 77U2	11) P12U
12) 9FA8	12) 78HC	12) C07P	12) 6AC7
13) 1C69	13) AHU5	13) 77U2	13) P12U
14) 9FA8	14) 78HC	14) 1933	14) 6AC7
15) 1C69	15) 470H	15) 77U2	15) P12U
16) AHU5	16) 5433	16) 33P6	16) 6AC7
17) 604U	17) 57F6	17) 77U2	17) P12U
18) 9982	18) F951	18) 8294	18) 6AC7
19) 0000	19) UFP7	19) 62HA	19) P12U
20) 9FA8	20) 9FA8	20) 9FA8	20) 6AC7

Table 6-4 (cont.)
PM 112 SIGNATURES

J1075 (cont.)	U2021	U2031 (cont.)	U2045
21) P12U	1) 2A41	5) 052A	1) 9FA8
22) 6AC7	2) 57F6	6) 5CPA	2) *
23) P12U	3) C438	7) 0H10	3) *
24) 6AC7	4) 470H	8) 9FA9	4) *
25) FHPH	5) 0000	9) 8C99	5) *
26) 16A3	6) 121A	10) 0000	6) *
27) U9FF	7) 60P2	11) 1731	7) PC5A
28) 07CU	8) 0000	12) 0001	8) *
29) 5664	9) 8F63	13) 91C8	9) *
30) FAFF	10) 9FA8	14) F742	10) 0000
31) 5664	11) 9FA8	15) 9982	11) 77U2
32) FAFF	12) 93H7	16) 1730	12) *
33) 5664	13) 9FA8	17) 0000	13) *
34) FAFF	14) 1H65	18) UFP7	14) *
35) 5664	15) 81FH	19) 0000	15) *
36) FAFF	16) 9FA8	20) 9FA8	16) *
37) 89C4			17) *
38) 8397			18) *
39) 1HH6	U2025	U2041	19) 9FA8
40) 32P5			20) 9FA8
41) 383P	1) 672C	1) 8688	
42) U205	2) 1HU0	2) 1A20	
43) 30UP	3) C4CH	3) 8688	U2055
44) 26A3	4) A156	4) 1A20	
45) 9FA8	5) 0000	5) 8688	1) 0000
46) 8F63	6) U399	6) 1A20	2) PC5A
47) 60P2	7) *	7) 8688	3) *
48) 121A	8) 0000	8) 1A20	4) PC5A
49) 62HA	9) *	9) *	5) *
50) 8HC4	10) 7U80	10) *	6) PC5A
51) 56UA	11) 829A	11) *	7) 77U2
52) 8HC4	12) 9H4C	12) 0000	8) PC5A
53) 9982	13) 9FC6	13) *	9) 77U2
54) 62HC	14) 052A	14) *	10) 0000
55) 9FA8	15) 9982	15) *	11) 77U2
56) 9FA8	16) 9FA8	16) *	12) *
57) 9FA8		17) *	13) 77U2
58) 9FA8		18) 9FA8	14) PC5A
59) 0000	U2031	19) 1A20	15) 77U2
60) 0000		20) 0000	16) PC5A
61) 9FA8	1) 0000	21) 9FA8	17) 77U2
62) 0000	2) 604U	22) 8688	18) PC5A
63) 9FA8	3) 9FA8	23) 1A20	19) 0000
64) 0000	4) 8C98	24) 9FA8	20) 9FA8

Table 6-4 (cont.)
PM 112 SIGNATURES

U2061

1) F742
2) 1730
3) 9FA8
4) *
5) 1730
6) 9FA8
7) H6C5
8) 0000
9) H6C5
10) 9FA8
11) 1730
12) H6C5
13) 9FA8
14) 1730
15) 91C8
16) 9FA8

U2065

1) 9FA8
2) 8C98
3) 0000
4) 0000
5) 0000
6) 0000
7) 9FA8
8) 0000
9) 9FA8
10) 9FA8
11) 6567
12) 36H3
13) 5CPA
14) 91C8
15) 1PUU
16) 9FA8

U2071

1) 1731
2) 8C98
3) 0003
4) 0000
5) 9FA8
6) 9FA8
7) 0000

U2071 (cont.)

8) 1730
9) 0000
10) 8C98
11) 8C98
12) 5CPA
13) 2196
14) 9FA8

U3021

1) 0000
2) *
3) 8688
4) *
5) 1A20
6) 8688
7) 1A20
8) *
9) U9FF
10) 0000
11) U399
12) 9FA8
13) 1A20
14) 8688
15) 1A20
16) FHPH
17) 8688
18) 16A2
19) 0000
20) 9FA8

U3025

1) 0000
2) 604U
3) 6567
4) 8257
5) 93H7
6) AHU5
7) 5CPA
8) 36H3
9) 1C69
10) 0000
11) 1730
12) 8688

U3025 (cont.)

13) 0H10
14) 91C8
15) 1A20
16) 8688
17) 0H10
18) 91C8
19) 1A20
20) 9FA8

U3031

1) 0000
2) 7U80
3) *
4) 9U6P
5) 9H4C
6) 672C
7) FP57
8) P614
9) C4CH
10) 0000
11) 1730
12) A156
13) C5UF
14) 9P19
15) 1HU0
16) 9FC6
17) 9F94
18) A0FH
19) 829A
20) 9FA8

U3035

1) 0000
2) 1A20
3) 91C8
4) 0H10
5) 8688
6) 1A20
7) 91C8
8) 0H10
9) 8688
10) 0000
11) 1730

U3035 (cont.)

12) 1A20
13) 91C8
14) 0H10
15) 8688
16) 1A20
17) 91C8
18) 0H10
19) 8688
20) 9FA8

U3041

1) 0000
2) 8688
3) 0H10
4) 91C8
5) 1A20
6) 8688
7) 0H10
8) 91C8
9) 1A20
10) 0000
11) 1730
12) 1A20
13) 91C8
14) 0H10
15) 8688
16) 1A20
17) 91C8
18) 0H10
19) 8688
20) 9FA8

U3045

1) 0000
2) 77U2
3) 67A7
4) H6C5
5) PC5A
6) 77U2
7) *
8) *
9) PC5A
10) 0000

Table 6-4 (cont.)
PM 112 SIGNATURES

U3045 (cont.)

11) F742
12) PC5A
13) H6C5
14) 67A7
15) 77U2
16) PC5A
17) *
18) 4A1H
19) 77U2
20) 9FA8

U3051

1) 0000
2) 77U2
3) 67A7
4) UC0U
5) PC5A
6) 77U2
7) 67A7
8) UC0U
9) PC5A
10) 0000
11) F742
12) PC5A
13) *
14) 67A7
15) 77U2
16) PC5A
17) UC0U
18) 67A7
19) 77U2
20) 9FA8

U3055

1) 5CPA
2) 36H3
3) 6567
4) 0000
5) 1PUU
6) 9FA8
7) C5UF
8) 0000
9) P614

U3055 (cont.)

10) 9P19
11) FP57
12) 9F94
13) 9U6P
14) A0FH
15) 5UH2
16) 9FA8

U3061

1) F742
2) 1730
3) 9FA8
4) UC0U
5) 1730
6) 9FA8
7) *
8) 0000
9) UC0U
10) 9FA8
11) 1730
12) UC0U
13) 9FA8
14) 1730
15) 91C8
16) 9FA8

U3065

1) F742
2) 1730
3) 9FA8
4) 4A1H
5) 1730
6) 9FA8
7) 67A7
8) 0000
9) 67A7
10) 9FA8
11) 1730
12) *
13) 9FA8
14) 1730
15) 91C8
16) 9FA8

U3071

1) 0528
2) 8257
3) 9980
4) 1PUU
5) 1PUU
6) 8257
7) 0000
8) 9FA9
9) 0003
10) 9980
11) 1730
12) 9FA8
13) 8C98
14) 9FA8

U3075

1) 9FA8
2) 9980
3) 8C98
4) 9FA8
5) 9FAC
6) 0003
7) 0000
8) 9FA8
9) 0000
10) 9FA8
11) 9FA8
12) 9FA8
13) 9FA8
14) 9FA8

U3079

1) F742
2) 1730
3) 9FA8
4) 67A7
5) 1730
6) 9FA8
7) 67A7
8) 0000
9) 67A7
10) 9FA8
11) 1730

U3079 (cont.)

12) 67A7
13) 9FA8
14) 1730
15) 91C8
16) 9FA8

U4015

1) 0000
2) *
3) 0000
4) 93H7
5) 9FA8
6) 604U
7) 9FA8
8) 1C69
9) 91C8
10) 0000
11) 91C8
12) 1C69
13) *
14) 604U
15) *
16) 93H7
17) 0000
18) 9FA8
19) 0000
20) 9FA8

U4021

1) 0000
2) 93H7
3) 470H
4) 2A41
5) 1730
6) 57F6
7) 93H7
8) C438
9) 1C69
10) 0000
11) 1C69
12) C438
13) 93H7
14) 57F6

Table 6-4 (cont.)
PM 112 SIGNATURES

U4021 (cont.)

15) 1730
16) 2A41
17) 470H
18) 93H7
19) 0000
20) 9FA8

U4025

1) 0000
2) 1C69
3) 9FA8
4) AHU5
5) 604U
6) 93H7
7) 8HC4
8) 604U
9) 62HA
10) 0000
11) 604U
12) 604U
13) 8HC4
14) 93H7
15) 604U
16) AHU5
17) 9FA8
18) 1C69
19) 0000
20) 9FA8

U4031

1) 0000
2) C4CH
3) A156
4) 672C
5) 1HU0
6) 9H4C
7) 9FC6
8) 7U80
9) 829A
10) 0000
11) 829A
12) 7U80
13) 9FC6

U4031 (cont.)

14) 9H4C
15) 1HU0
16) 672C
17) A156
18) C4CH
19) 0000
20) 9FA8

U4035

1) 0000
2) 8688
3) 1A20
4) 1A20
5) 8688
6) 8688
7) 1A20
8) 1A20
9) 8688
10) 0000
11) 8688
12) 1A20
13) 1A20
14) 8688
15) 8688
16) 1A20
17) 1A20
18) 8688
19) 0000
20) 9FA8

U4041

1) 0000
2) 1A20
3) 1A20
4) 8688
5) 8688
6) 1A20
7) 1A20
8) 8688
9) 8688
10) 0000
11) 8688
12) 8688

U4041 (cont.)

13) 1A20
14) 1A20
15) 8688
16) 8688
17) 1A20
18) 1A20
19) 0000
20) 9FA8

U4045

1) 0000
2) PC5A
3) PC5A
4) 77U2
5) 77U2
6) PC5A
7) PC5A
8) 77U2
9) 77U2
10) 0000
11) 77U2
12) 77U2
13) PC5A
14) PC5A
15) 77U2
16) 77U2
17) PC5A
18) PC5A
19) 0000
20) 9FA8

U4051

1) 0000
2) PC5A
3) PC5A
4) 77U2
5) 77U2
6) PC5A
7) PC5A
8) 77U2
9) 77U2
10) 0000
11) 77U2

U4051 (cont.)

12) 77U2
13) PC5A
14) PC5A
15) 77U2
16) 77U2
17) PC5A
18) PC5A
19) 0000
20) 9FA8

U4061

1) 0000
2) 2A41
3) U17A
4) 0A74
5) 57F6
6) C438
7) FH89
8) 1C69
9) 8HC4
10) 0000
11) 0000
12) 93H7
13) 8257
14) 0001
15) 0000
16) 1730
17) 8C99
18) 2CP3
19) 470H
20) 9FA8

U4065

1) 1A20
2) AHU5
3) 0000
4) 8C98
5) 1PUU
6) 9FAC
7) 9FA8
8) 0000
9) 9FA8
10) 9FA8

Table 6-4 (cont.)
PM 112 SIGNATURES

U4065 (cont.)

11) 9FA8
12) FH89
13) U17A
14) 2CP3
15) 0A74
16) 9FA8

U4071

1) 9FA8
2) 0000
3) 0000
4) 0000
5) 0000
6) 0000
7) 9FA8
8) 0000
9) 9FA8
10) 9FA8
11) 1C69
12) AHU5
13) 1A20
14) 8C98
15) 0528
16) 9FA8

U4075

1) 9FA8
2) 0000
3) 9FA8
4) 9FA8
5) 8C98
6) 1730
7) 0000
8) F742
9) 2196
10) 0000
11) 0000
12) 0000
13) 5CPA
14) 9FA8

U4079

1) 9FA8
2) 9FA8
3) 0000
4) 9FA8
5) 9FA8
6) 0000
7) 0000
8) 9FA8
9) 0000
10) 0000
11) 9FA8
12) 9FA8
13) 0000
14) 9FA8

P4039

(odd # pins)
13) 0000
15) 8HC4
17) 0000
19) 2A41
21) C438
23) 1730
25) 93H7
27) 604U
29) 1C69
31) 0000
33) 93H7
35) 829A
37) 9FC6
39) 1HU0
41) A156
43) 1A20
45) 1A20
47) 1A20
49) 1A20
51) 1A20
53) 1A20
55) 1A20
57) 1A20
59) 77U2
61) 77U2

P4039 (cont.)

63) 77U2
65) 77U2
67) 77U2
69) 77U2
71) 77U2
73) 77U2

P4039

(even # pins)
14) 93H7
16) 8HC4
18) 0000
20) 57F6
22) 470H
24) 1C69
26) AHU5
28) 1A20
30) 8688
32) 1A20
34) 8688
36) 7U80
38) 9H4C
40) 672C
42) C4CH
44) 8688
46) 8688
48) 8688
50) 8688
52) 8688
54) 8688
56) 8688
58) 8688
60) PC5A
62) PC5A
64) PC5A
66) PC5A
68) PC56
70) PC5A
72) PC5A
74) PC5A

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

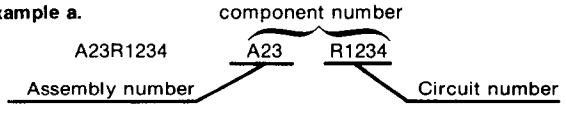
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

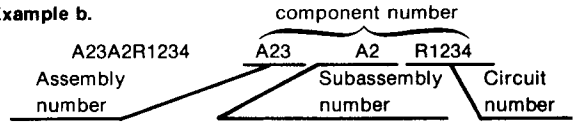
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
01961	PULSE ENGINEERING, INC.	7250 CONVOY COURT	SAN DIEGO, CA 92111
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
09353	C AND K COMPONENTS, INC.	103 MORSE STREET	WATERTOWN, MA 02172
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Replaceable Electrical Parts - PM 112

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A01	670-7458-00			CKT BOARD ASSY:PERSONALITY MODULE	80009	670-7458-00
A02	670-6149-00			CKT BOARD ASSY:PROBE CONNECTOR	80009	670-6149-00
	----- -----			(NO ELECTRICAL PARTS)		
A01	----- -----			CKT BOARD ASSY:PERSONALITY MODULE		
A01C1010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C1012	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C1025	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C1045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C1051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C1053	290-0747-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	500D148
A01C1055	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C1057	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C2025	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C2035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C2051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C2065	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C2075	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C2080	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C2081	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C2085	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C2086	281-0758-00			CAP.,FXD,CER DI:15PF,20%,100V	72982	314022C0G0150M
A01C3025	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3039	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3049	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3055	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3065	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3071	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3075	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C4025	281-0775-00			CAP.,FXD,CER DI:Q.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C4035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C4045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C4049	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C4051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C4061	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C4071	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C4075	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C4081	283-0625-00			CAP.,FXD,MICA D:220PF,1%,500V	00853	D105F221F0
A01C4083	283-0625-00			CAP.,FXD,MICA D:220PF,1%,500V	00853	D105F221F0
A01C4089	290-0748-00			CAP.,FXD,ELCTLT:10UF,+50-10%,20V	56289	500D149
A01CR4085	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A01DL3081	119-1169-00			DELAY LINE:DUAL,30NS,120 OHM,16 DIP	01961	PE22376
A01DS2037	150-1001-02			LT EMITTING DIO:RED,660NM,50MA MAX	80009	150-1001-02
A01J1030	131-2848-01			CONN,RCPT,ELEC:EDGE CARD,2 X 43	80009	131-2848-01
A01L4083	108-0735-00			COIL,RF:FIXED,560NH	80009	108-0735-00
A01Q2081	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A01Q2083	151-0271-00			TRANSISTOR:SILICON,PNP	04713	SPS8236
A01Q2084	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A01Q2085	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A01Q2086	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A01Q2087	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A01Q3085	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A01Q4071	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A01Q4083	151-0367-00			TRANSISTOR:SILICON,NPN,SEL FROM 3571TP	01295	SKA6516

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A01Q4085	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A01R1031	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1033	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1035	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1041	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1051	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1053	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R1083	322-0612-00			RES.,FXD,FILM:500 OHM,1%,0.25W	75042	CEBT0-5000F
A01R1085	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A01R1087	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A01R2037	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A01R2051	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R2065	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A01R2075	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R2077	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R2079	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A01R2081	321-0170-00			RES.,FXD,FILM:576 OHM,1%,0.125W	91637	MFF1816G576R0F
A01R2082	321-0181-00			RES.,FXD,FILM:750 OHM,1%,0.125W	91637	MFF1816G750R0F
A01R2083	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A01R2084	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A01R2085	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A01R2086	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A01R2087	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A01R2088	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A01R2089	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A01R3075	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A01R3079	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A01R3080	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A01R3081	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A01R3085	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A01R3087	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A01R3089	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A01R4021	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A01R4025	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A01R4061	317-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.125W	01121	BB1815
A01R4071	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A01R4081	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A01R4083	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A01R4084	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A01R4085	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A01SW1085	260-1962-00			SWITCH,PUSH:SPDT,0.4VA,20V	09353	8125AE
A01U1015	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A01U1021	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	18324	N74LS240N
A01U1045	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A01U2021	156-1252-00			MICROCIRCUIT,DI:8/3 LINE PRIORITY ENCODER	80009	156-1252-00
A01U2025	156-1252-00			MICROCIRCUIT,DI:8/3 LINE PRIORITY ENCODER	80009	156-1252-00
A01U2031	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A01U2041	160-1566-00			MICROCIRCUIT,DI:2048 X 8 EPROM	80009	160-1566-00
A01U2045	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A01U2055	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A01U2061	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP MUX	01295	SN74LS157P3
A01U2065	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A01U2071	156-0690-03			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A01U3021	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A01U3025	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A01U3031	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A01U3035	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A01U3041	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A01U3045	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A01U3051	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A01U3055	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A01U3061	156-0530-02			MICROCIRCUIT,DI:QUAD 2 INP MUX	01295	SN74LS157P3
A01U3065	156-1395-01			MICROCIRUIT,DI:QUAD 2 LINE TO 1 LINE DATA	01295	SN74LS158
A01U3071	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A01U3075	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POSITIVE EDGE	80009	156-0331-03
A01U3079	156-1395-01			MICROCIRCUIT,DI:QUAD 2 LINE TO 1 LINE DATA	01295	SN74LS158
A01U4015	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A01U4021	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A01U4025	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A01U4031	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A01U4035	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A01U4041	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A01U4045	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A01U4051	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A01U4061	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A01U4065	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A01U4071	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A01U4075	156-1040-01			MICROCIRCUIT,DI:2 WIDE 2 INPUT/INVERT GATE	80009	156-1040-01
A01U4079	156-0721-02			MICROCIRCUIT,DI:QUAD 2-IN NAND SCHMITT TRI	04713	SN74LS132NDS
A01VR4085	152-0744-00			SEMICOND DVC,DI:ZEN,SI,3.6V,5%,0.4W	04713	1N747A

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

PM 112

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

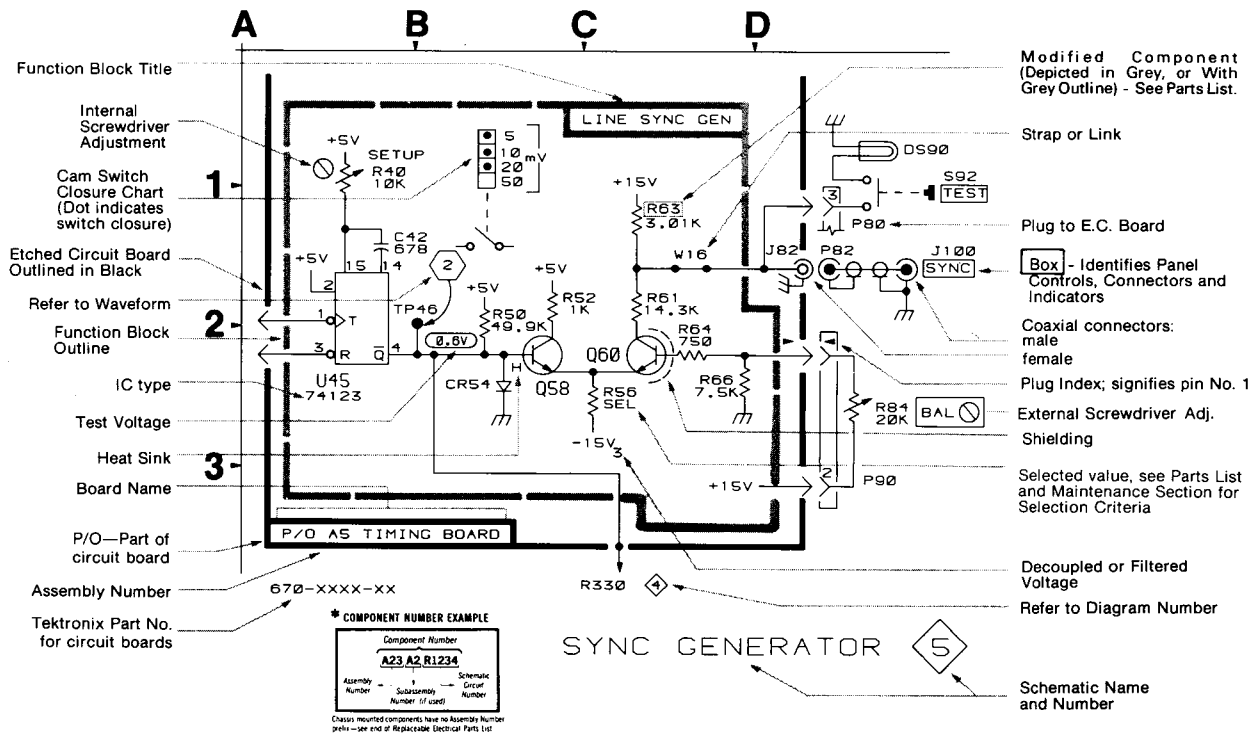
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



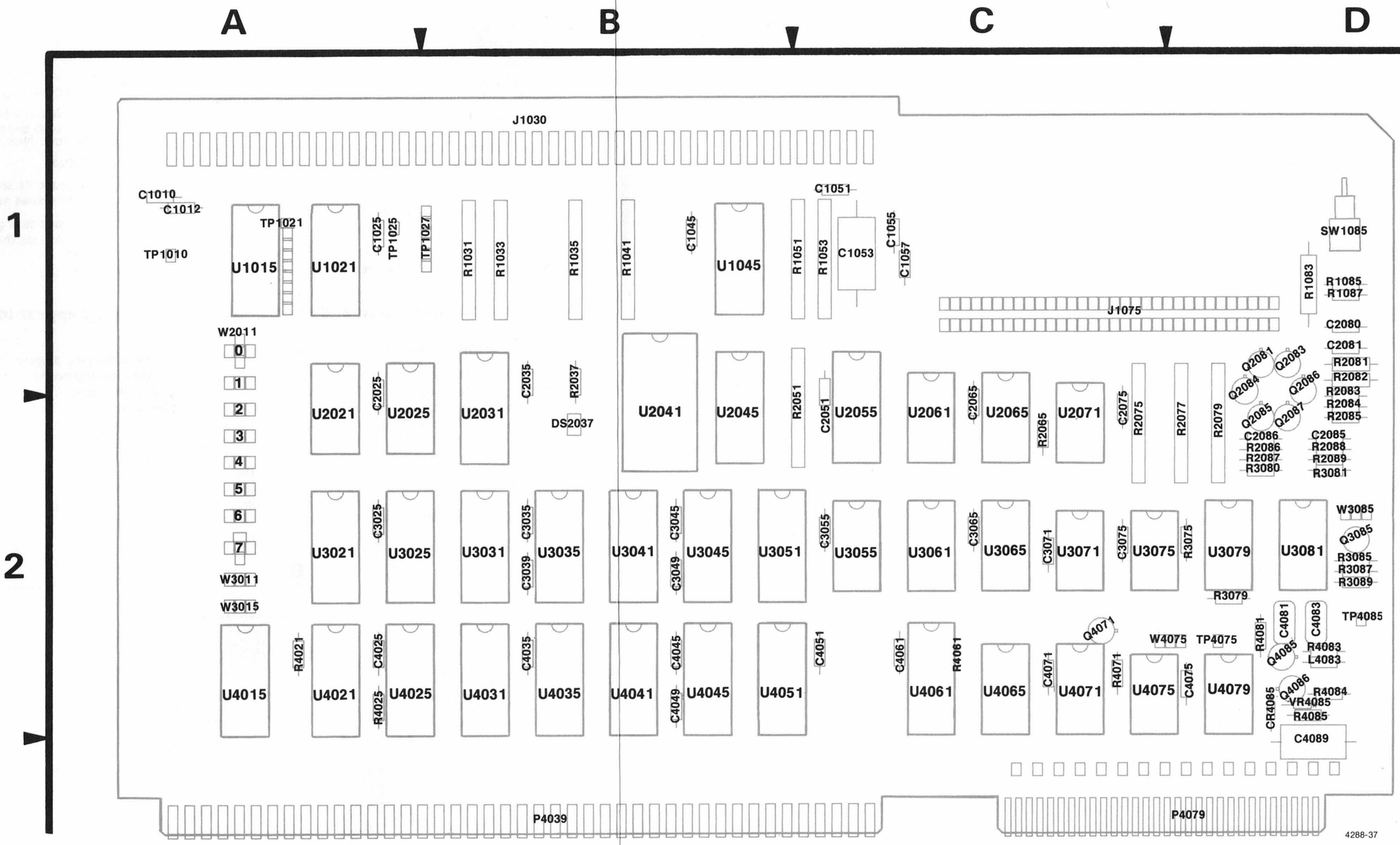


Figure 8-1. PM 112 Circuit Board Component Locations.

Table 8-1

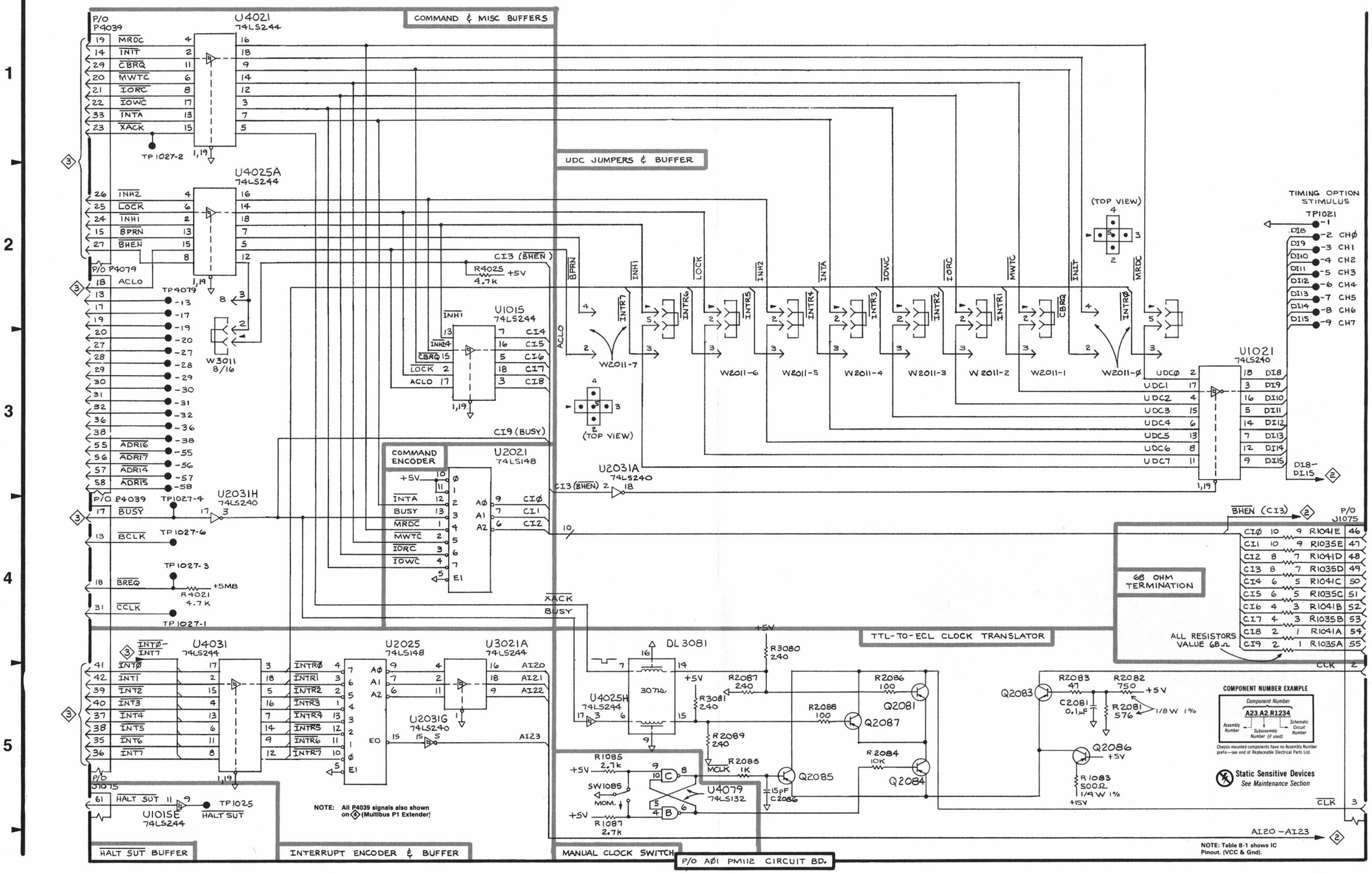
IC PIN INFORMATION

Device Type	VCC	GND
2716	24	12
74S00	14	7
74S02	14	7
74S51	14	7
74S74	14	7
74LS132	14	7
74LS138	16	8
74LS148	16	8
74LS157	16	8
74LS158	16	8
74LS161	16	8
74LS240	20	10
74LS244	20	10
74LS374	20	10
81LS97	20	10

PM 112 ACQUISITION

ASSEMBLY A01

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C2081	E5	D1
C2086	D5	D2
DL3081	C5	D2
J1075	F4	C1
J1075	A5	C1
P4039	A1	B3
P4039	A4	B3
P4079	A2	D3
Q2081	D5	D1
Q2083	E5	D1
Q2084	D5	D1
Q2085	D5	D2
Q2086	E5	D1
Q2087	D5	D2
R1035A	F4	B1
R1035B	F4	B1
R1035C	F4	B1
R1035D	F4	B1
R1035E	F4	B1
R1041A	F4	B1
R1041B	F4	B1
R1041C	F4	B1
R1041D	F4	B1
R1041E	F4	B1
R1083	E5	D1
R1085	C5	D1
R1087	C5	D1
R2081	E5	D1
R2082	E5	D1
R2083	E5	D2
R2084	D5	D2
R2085	D5	D2
R2086	D5	D2
R2087	D5	D2
R2088	D5	D2
R2089	C5	D2
R3080	D4	D2
R3081	C5	D2
R4021	A4	A2
R4025	B2	A2
SW1085	C5	D1
TP1021	F2	A1
TP1025	A5	A1
TP1027-1	A4	B1
TP1027-2	A1	B1
TP1027-3	A4	B1
TP1027-4	A4	B1
TP1027-6	A4	B1
TP4079	A2	D3
U1015	B3	A1
U1015E	A5	A1
U1021	F3	A1
U2021	B4	A2
U2025	B5	A2
U2031A	C3	B2
U2031G	B5	B2
U2031H	A4	B2
U3021A	B5	A2
U4021	A1	A2
U4025A	A2	A2
U4025H	C5	A2
U4031	A5	B2
U4079A	C5	D2
U4079B	C5	D2
W2011-0	E3	A2
W2011-1	E3	A2
W2011-2	E3	A2
W2011-3	D3	A2
W2011-4	D3	A2
W2011-5	D3	A2
W2011-6	D3	A2
W2011-7	C3	A2
W3011	A3	A2



PM 112 ACQUISITION

ASSEMBLY A01

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1075	F1	C1
J1075	A2	C1
J1075	A5	C1
P4039	B1	B3
P4039	A3	B3
Q3085	B2	D2
R1031A	F3	B1
R1031B	F3	B1
R1031C	F3	B1
R1031D	F2	B1
R1031E	F2	B1
R1033A	F3	B1
R1033B	F3	B1
R1033C	F3	B1
R1033D	F2	B1
R1033E	F2	B1
R1051A	F3	C1
R1051B	F4	C1
R1051C	F4	C1
R1051D	F5	C1
R1051E	F5	C1
R1053A	F3	C1
R1053B	F4	C1
R1053C	F5	C1
R1053D	F5	C1
R1053E	F5	C1
R2051A	F2	B2
R2051B	F2	B2
R2051C	F2	B2
R2051D	F2	B2
R2051E	F2	B2
R2075A	F4	C2
R2075B	F4	C2
R2075C	F4	C2
R2075D	F4	C2
R2075E	F4	C2
R2077A	F4	D2
R2077B	F4	D2
R2077C	F4	D2
R2077D	F2	D2
R2077E	F2	D2
R2079A	F1	D2
R2079B	F1	D2
R2079C	F1	D2
R2079D	F1	D2
R2079E	F1	D2
R3085	A2	D2
R3087	A2	D2
R3089	B2	D2
U1045	C4	B1
U2041	D3	B2
U2045	E3	B2
U2055	C3	C2
U3021B	E2	A2
U4025E	B5	A2
U4035	D2	B2
U4041	C2	B2
U4045	B4	B2
U4051	B3	B2

P/O P4039 57 58 55 56 53 54 51 52 — 49 50 47 48 45 46 43 44 — 28 30 32 34

ADRØ ADR1 ADR2 ADR3 ADR4 ADR5 ADR6 ADR7 — ADR8 ADR9 ADRA ADRB ADRC ADRD ADRE ADRF — ADR10 ADR11 ADR12 ADR13

68 OHM TERMINATION

P/O J1075

3 ADRØ-ADR13

INHIBIT SENSOR

+5MB R3085 10K Q3085 +5T R3087 1k R3089 510

U4041 74LS244 17 15 13 11 2 4 6 8 — 1,19 1,19 — 3 5 7 9 18 16 14 12 — AIØ AI1 AI2 AI3 AI4 AI5 AI6 AI7

U4035 74LS244 4 6 8 2 17 15 13 11 — 16 14 12 18 3 5 7 9 — AI8 AI9 AI10 AI11 AI12 AI13 AI14 AI15

U3021B 74LS244 15 17 13 6 — 19 — 5 3 7 14 — AI16 AI17 AI18 AI19

24

P/O J1075 62 LOOK 1 AI20-AI23

ADDRESS BUFFERS

EPROM & BUFFER

P/O P4039 3 DATØ-DATF

U4051 74LS244 1,19 — U2055 74LS244

73 DATØ 11 — 9 11 — 9 DIØ
74 DAT1 13 — 7 8 — 12 DI1
71 DAT2 15 — 5 13 — 7 DI2
72 DAT3 17 — 3 6 — 14 DI3
69 DAT4 8 — 12 15 — 5 DI4
70 DAT5 6 — 14 4 — 16 DI5
67 DAT6 4 — 16 17 — 3 DI6
68 DAT7 2 — 18 2 — 18 DI7

1,19

U4045 74LS244 — U1045 74LS244

65 DAT8 11 — 9 17 — 3 DI8
66 DAT9 13 — 7 2 — 18 DI9
63 DATA 15 — 5 15 — 5 DI10
64 DATB 17 — 3 4 — 16 DI11
61 DATC 8 — 12 13 — 7 DI12
62 DATD 6 — 14 6 — 14 DI13
59 DATE 4 — 16 11 — 9 DI14
60 DATF 2 — 18 8 — 12 DI15

1,19

U4025E 74LS244 9 11

BHEN(C3) DI8-DI15

P/O J1075 1

63 SELP

U2041 2716

AIØ 8 AØ
AI1 7 A1
AI2 6 A2
AI3 5 A3
AI4 4 A4
AI5 3 A5
AI6 2 A6
AI7 1 A7
AI8 23 A8
AI9 22 A9
AI10 19 A10
+5V 21 A11
20 OE
18 CE

U2045 81LS97

DØ 9 12 — 11 DIØ
D1 10 8 — 9 DI1
D2 11 14 — 13 DI2
D3 13 6 — 7 DI3
D4 14 16 — 15 DI4
D5 15 4 — 5 DI5
D6 16 18 — 17 DI6
D7 17 2 — 3 DI7

1,19

P/O J1075

AIØ 10 9 R2079E 5
AI1 8 7 R2079D 6
AI2 6 5 R2079C 7
AI3 4 3 R2079B 8
AI4 2 1 R2079A 9
AI5 10 9 R2077E 10
AI6 8 7 R2077D 11
AI7 10 9 R2051E 12
AI8 7 8 R2051D 13
AI9 5 6 R2051C 14
AI10 3 4 R2051B 15
AI11 2 1 R2051A 16
AI12 8 7 R1031D 17
AI13 10 9 R1031E 18
AI14 8 7 R1033D 19
AI15 10 9 R1033E 20
AI16 2 1 R1031A 21
AI17 2 1 R1033A 22
AI18 4 3 R1031B 23
AI19 4 3 R1033B 24
AI20 6 5 R1031C 25
AI21 6 5 R1033C 26
AI22 1 2 R1051A 27
AI23 1 2 R1053A 28

ALL RESISTORS VALUE 68 Ω

DIØ 6 5 R2077C 29
DI1 4 3 R2077B 30
DI2 2 1 R2077A 31
DI3 10 9 R2075E 32
DI4 8 7 R2075D 33
DI5 6 5 R2075C 34
DI6 4 3 R2075B 35
DI7 2 1 R2075A 36
DI8 3 4 R1051B 37
DI9 3 4 R1053B 38
DI10 5 6 R1051C 39
DI11 5 6 R1053C 40
DI12 7 8 R1051D 41
DI13 7 8 R1053D 42
DI14 9 10 R1051E 43
DI15 9 10 R1053E 44

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

NOTE: All P4039 signals also shown on 4 (Multibus P1 Extender)

DATA BUFFERS

P/O AØ1 PM112 CIRCUIT BD.

Static Sensitive Devices — See Maintenance Section

NOTE: Table 8-1 shows IC Pinout. (VCC & Gnd).

PM112 INSTRUCTION

4288-51

PM112 ACQUISITION 2

PM 112 SELF-TEST

ASSEMBLY A01

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1025	A5	A1	R4083	A3	D2
C1045	A5	B1	R4084	A4	D2
C1053	A5	C1	R4085	A4	D2
C1055	A5	C1	TP1010	A5	A1
C2025	A5	A2	TP1027-5	F4	B1
C2035	A5	B1	TP4075	A2	D2
C2051	A5	C2	TP4085	A5	D2
C2065	A5	C2	U2031B	B3	B2
C2075	A5	C2	U2031C	C4	B2
C2080	A5	D1	U2031D	E5	B2
C2085	A5	D2	U2031E	E5	B2
C3025	A5	A2	U2031F	B2	B2
C3035	A5	B2	U2061	E2	C2
C3039	A5	B2	U2065	C4	C2
C3045	A5	B2	U2071A	E5	C2
C3049	A5	B2	U2071B	B3	C2
C3055	A5	C2	U2071C	B4	C2
C3065	A5	C2	U2071D	C5	C2
C3071	A5	C2	U3025A	F5	A2
C3075	A5	C2	U3025B	E1	A2
C4025	A5	A2	U3031	F2	B2
C4035	A5	B2	U3035	D1	B2
C4045	A5	B2	U3041	C1	B2
C4049	A5	B2	U3045	E2	B2
C4051	A5	C2	U3051	D2	B2
C4061	A5	C2	U3055	F2	C2
C4071	A5	C2	U3061	C2	C2
C4075	A5	D2	U3065	D2	C2
C4081	A3	D2	U3071A	D4	C2
C4083	A3	D2	U3071B	D4	C2
C4089	A4	D3	U3071C	E5	C2
CR4085	A4	D2	U3071D	B4	C2
DS2037	A4	B2	U3075A	E4	C2
J1075	A5	C1	U3075B	B3	C2
L4083	A3	D2	U3079	B3	D2
P4039	F4	B3	U4015A	F5	A2
P4039	F5	B3	U4015E	C4	A2
P4039	A1	B3	U4015H	C3	A2
P4079	F5	D3	U4061	F4	C2
Q4071	A4	C2	U4065	E4	C2
Q4083	A3	D2	U4071	B4	C2
Q4085	A4	D2	U4075A	B2	C2
R2037	A4	B1	U4075B	C5	C2
R2065	B4	C2	U4079A	A4	D2
R3075	E5	D2	U4079D	A3	D2
R3079	A3	D2	VR4085	A4	D2
R4061	F4	C2	W3015	F4	A2
R4071	A4	C2	W3085	A5	D2
R4081	A3	D2	W4075	A2	C2

AA-55 ADDRESS GENERATOR & DESKEW LATCHES

U3041 74LS374 — ADRØ ADR1 ADR2 ADR3 ADR4 ADR5 ADR6 ADR7

U3035 74LS374 — ADR8 ADR9 ADRA ADRB ADRC ADRD ADRE ADRF

U3025B 74LS374 — ADR10 ADR11 ADR12 ADR13

20 ADRØ–ADR13 ②

U2031F 74LS240

U4075A 74S51 — PXACK

EXT CLK IN TP4075 — W4075 — EXT / INT / TEST CLK — TCLK

SELF-TEST OSCILLATOR

+5T — R4081 2.7K — L4083 560nH — U4079D 74LS132 — Q4083 — C4081 220pF — C4083 220pF — R4083 10K — −15PM

U3075B 74S74

U2071B 74S02

U2031B 74LS240

U3079 74LS158 — U3061 74LS157 — U3051 74LS374 — U3065 74LS158 — U2061 74LS157 — U3045 74LS374 — DATØ DAT1 DAT2 DAT3 DAT4 DAT5 DAT6 DAT7

PXACK — QB — TC — TD — QA

U3055 74LS138 — U3031 74LS374 — INTØ INT1 INT2 INT3 INT4 INT5 INT6 INT7 — INTØ–INT7 ①

DATØ–DATF ②

AA-55 DATA GENERATORS & DESKEW LATCHES

INTERRUPT DECODER & DESKEW LATCH

COMMAND DECODER & DESKEW LATCH

POWER-ON RESET — R4085 390 — R4084 4.7K — R3079 2.2K — Q4085 — VR4085 3.6V — Q4071 — R4071 1K — U4079A 74LS132 — CR4085 — C4089 10µF

TA

U4015H 74LS244 — R2065 2K — +5MB — OUTPUT INHIBIT SENSOR

PHASE A COUNTER — U4071 74LS161 — CLR ENT ENP LD RCO QA QB QC QD — PXACK — ID/M — R/W

U3071D 74S00 — U2071C 74S02 — U2065 74LS161 — U4015E 74LS244 — U2031C 74LS240 — TB — QA — QC — QD — PINTA

PHASE B COUNTER

IO/M — R/W — PINTA — PXACK

U3071B 74S00 — U3071A 74S00 — U3075A 74S74 — U3071C 74S00 — U2031D 74LS240 — U2071A 74S02 — U2031E 74LS240 — PBUSY — PXACK — PINTA

U9065 74LS138 — A B C G2B G2A G1 — Y0 Y1 Y2 Y3

U4061 74LS374 — BPRO BPRN MWTC IOWC MRDC IORC BUSY XACK INTA

W3015 PAR — TP1027-5 SER — P/O P4039

U4015A 74LS244 — ACLO CBRQ INIT

U3025A 74LS374 — LOCK INH1 BHEN INH2

XACK, BUSY, & INTA GENERATOR

MISC. DESKEW & BUFFER — P/O P4039

POWER CIRCUITRY — R 2037 220 — DS 2037 — POWER ON — TEST — NORM — W3085 — P/O P4039 — P/O J1075 — +5MB

TIMING GENERATOR — TP1010 — TP4085 — C1053 100µF — C2080 0.1µF — C2085 0.1µF — C1025 C1045 C1055 C2025 C2035 C2051 C4025 C4035 C4045 C4049 C4051 — C2065 C2075 C3025 C3035 C3045 C3055 C3039 — C3065 C3075 C4061 C4071 C4075 C3071 C3049

+5T CONNECTED TO ALL I.C. VCC PINS ON ③ EXCEPT U2031 AND U4079

PBRN — PBUSY — TB

R3075 4.7K

COMPONENT NUMBER EXAMPLE — Component Number A23 A2 R1234 — Assembly Number / Subassembly Number (if used) / Schematic Circuit Number — Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

NOTE: All P4039 signals also shown on ④ (Multibus P1 Extender)

Static Sensitive Devices — See Maintenance Section

NOTE: Table 8-1 shows IC Pinout. (VCC & Gnd).

P/O AØ1 PM112 CIRCUIT BD.

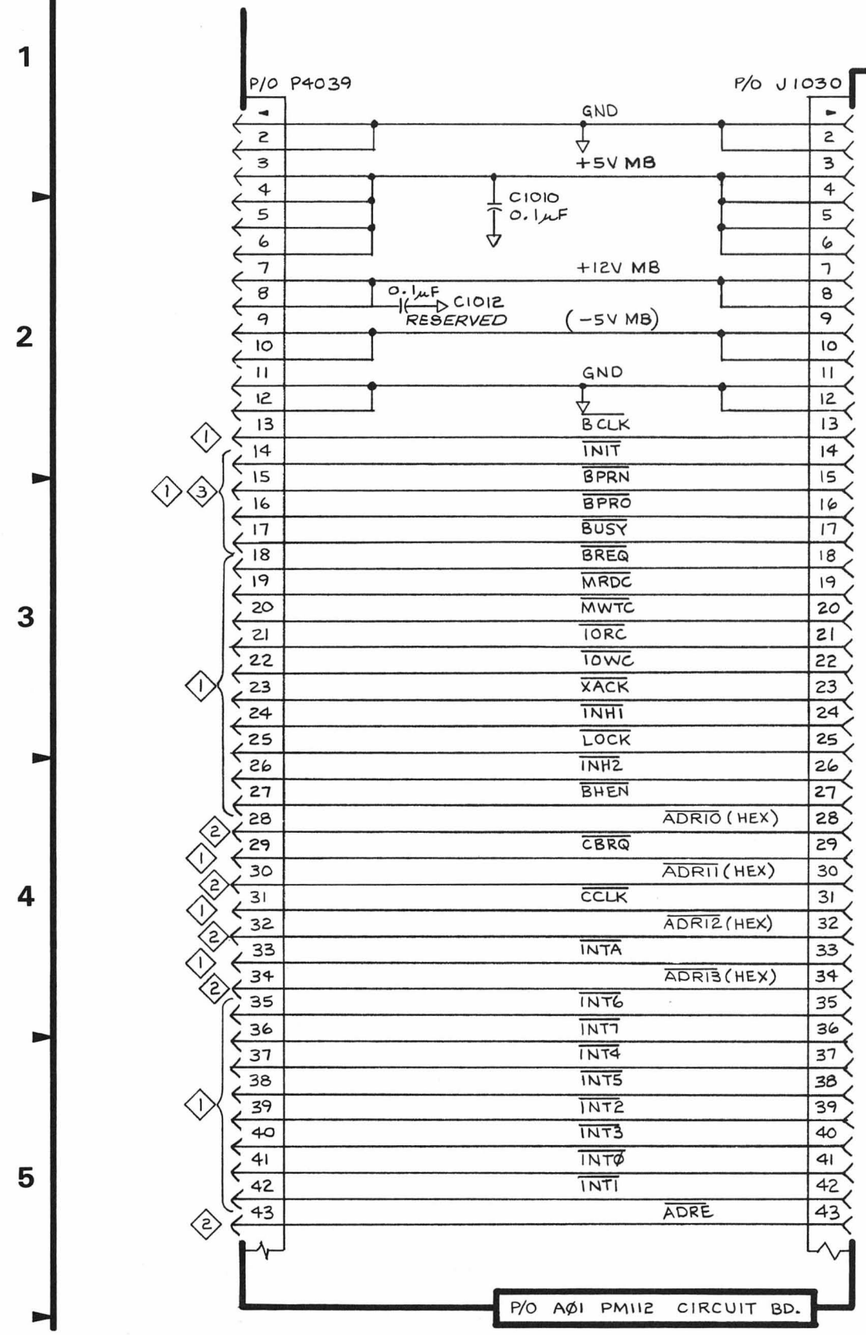
PM112 INSTRUCTION

4288-52

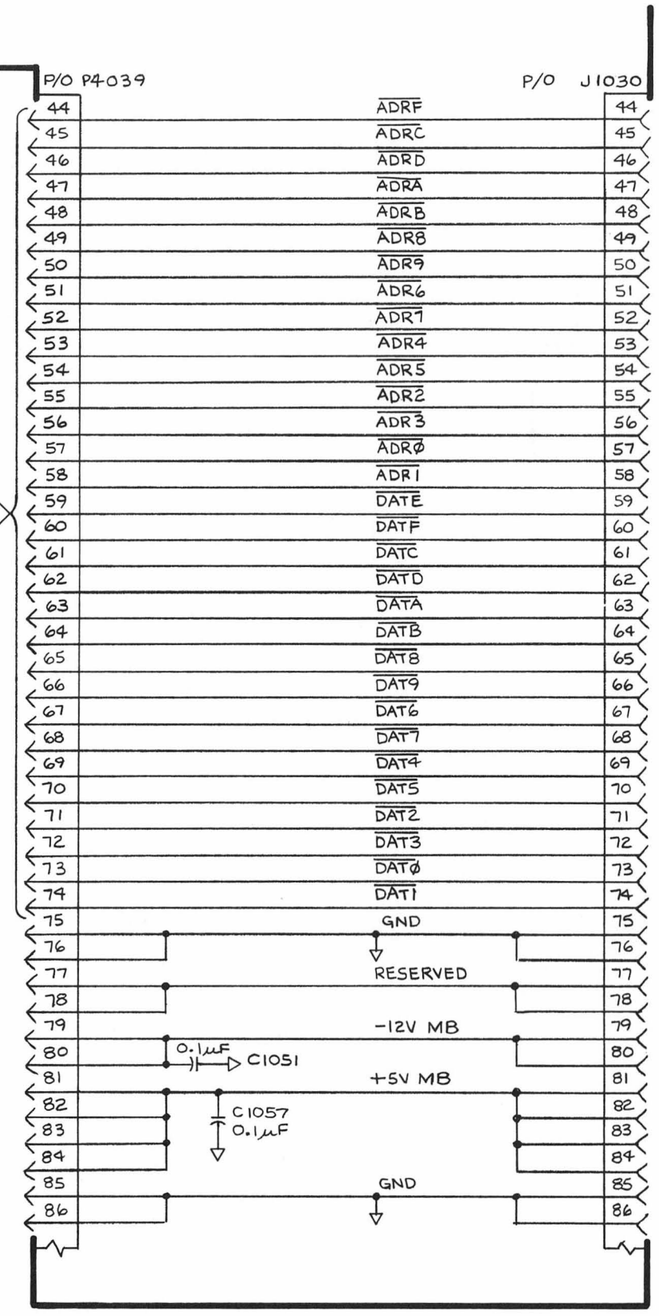
PM112 SELF-TEST ③

MULTIBUS P1 EXTENDER 

ASSEMBLY A01		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1010	B2	A1
C1012	B2	A1
C1051	E5	C1
C1057	E5	C1
J1030	F1	B1
J1030	C1	B1
P4039	D1	B3
P4039	A1	B3



PM112 INSTRUCTION 4288-53



MULTIBUS P1 EXTENDER 4

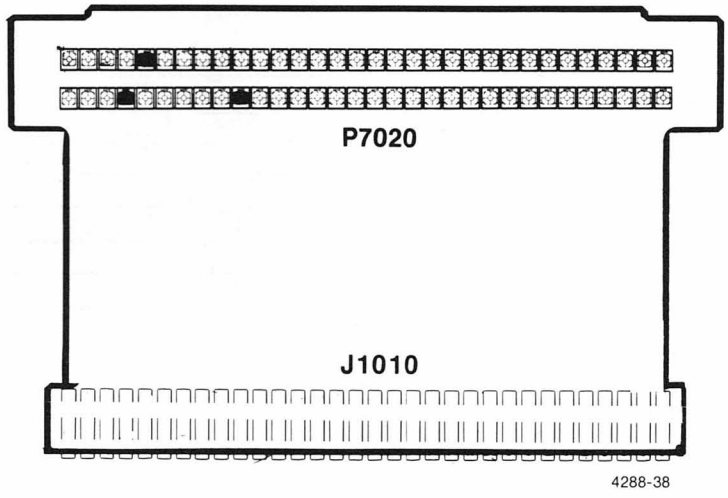
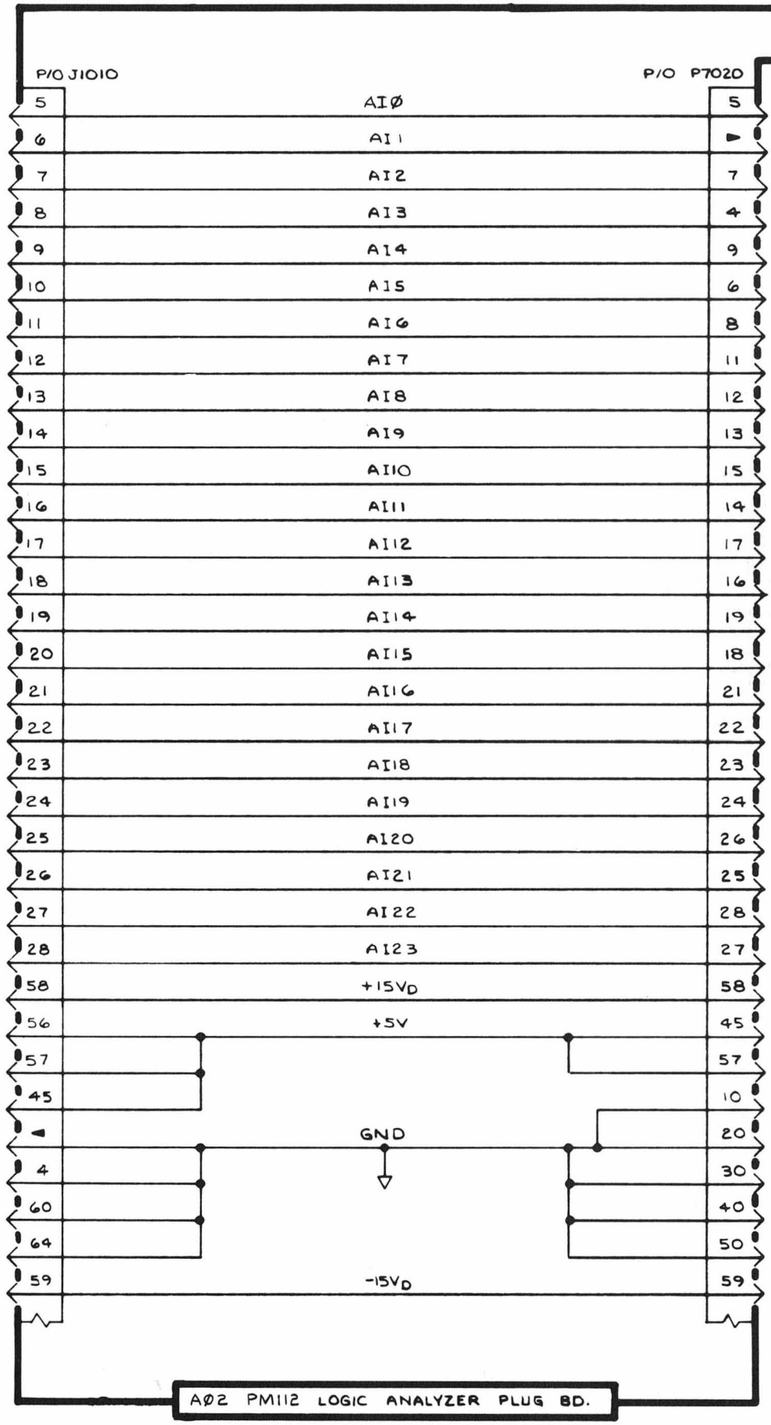
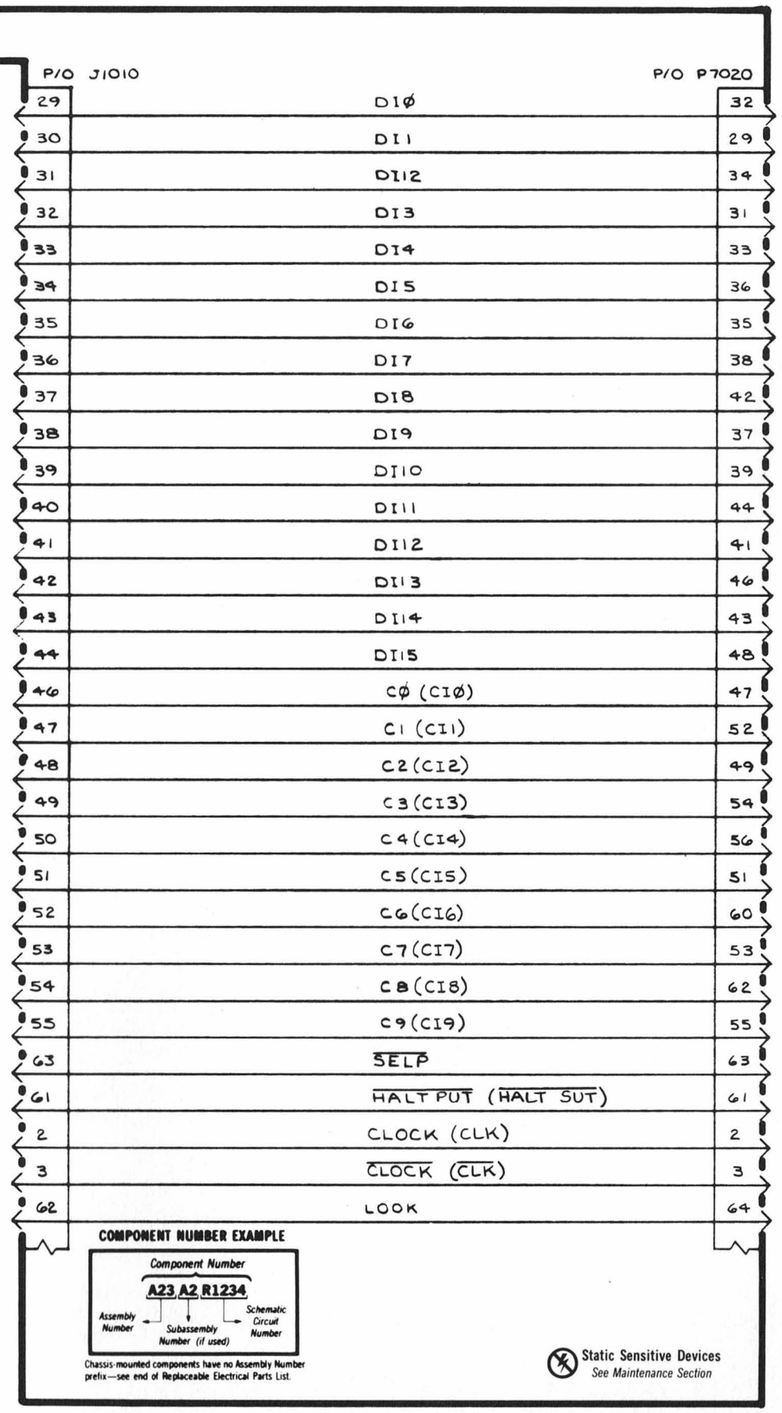


Figure 8-2. A02 Logic Analyzer Plug Board.



PM112 INSTRUCTION 4288-54



LOGIC ANALYZER PLUG 5

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
\- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
\- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
\- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000AH	STANDARD PRESSED STEEL CO., UNBRAKO DIV.	8535 DICE ROAD	SANTA FE SPRINGS, CA 90670
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
18677	SCANBE MFG. CORP.	3445 FLETCHER AVE.	EL MONTE, CA 91731
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-	131-2613-01			1		CONN,RCPT,ELEC:CABLE,32/64 MALE	80009	131-2613-01
-1	334-3722-00			1		. PLATE,IDENT:PERSONALITY MODULE PM100 SERIES	80009	334-3722-00
-2	380-0591-00			1		. HSG HALF,CKT BD:TOP	80009	380-0591-00
						(ATTACHING PARTS)		
-3	211-0225-00			2		. SCR,CAP,SOC HD:4-40 X 0.312 INCH,STL	000AH	OBD
-4	211-0093-00			2		. SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-5	210-0551-00			4		. NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	000BK	OBD
						- - - * - - -		
-6	380-0590-01			1		. HSG,HALF:BOTTOM	80009	380-0590-01
-7	343-0836-00			2		. CLAMP,CABLE:3.72 L	80009	343-0836-00
-8	213-0055-00			4		. SCR,TPG,THD FOR:2-32 X 0.188 INCH,PNH STL	93907	OBD
-9	----- -----			1		. CKT BOARD ASSY:(SEE A02 REPL)		
-10	131-0608-00			64		. . TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-11	175-3537-02			1		. CA ASSY,SP,ELEC:64,28 AWG,48.0 L,RIBBON	80009	175-3537-02
-12	343-1059-00			1		CLAMP,CABLE:ALUMINUM	80009	343-1059-00
						(ATTACHING PARTS)		
-13	211-0510-00			2		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
-14	210-0802-00			2		WASHER,FLAT:0.15 ID X 0.312 INCH OD	12327	OBD
-15	343-1058-00			1		CLAMP,CABLE:ALUMINUM	80009	343-1058-00
-16	----- -----			1		CKT BOARD ASSY:(SEE A01 REPL)		
-17	105-0144-00			1		. EJECTOR,CKT CD:MOLD PLASTIC,W/ROLL PIN	18677	S203
-18	213-0055-00			4		. SCR,TPG,THD FOR:2-32 X 0.188 INCH,PNH STL	93907	OBD
-19	----- -----			1		. CONN,RCPT,ELEC:(SEE A01J1030 REPL)		
-20	131-0608-00			139		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-21	131-0993-00			13		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-22	136-0751-00			1		. SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-23	337-3058-00			1		SHIELD,CKT BD:PLASTIC LAMINATE	80009	337-3058-00
						(ATTACHING PARTS)		
-24	211-0038-00			4		SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG	83385	OBD
-25	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
-26	210-1006-00			4		WASHER,FLAT:0.12 ID X 0.062 THK,AL,0.25	80009	210-1006-00
						- - - * - - -		

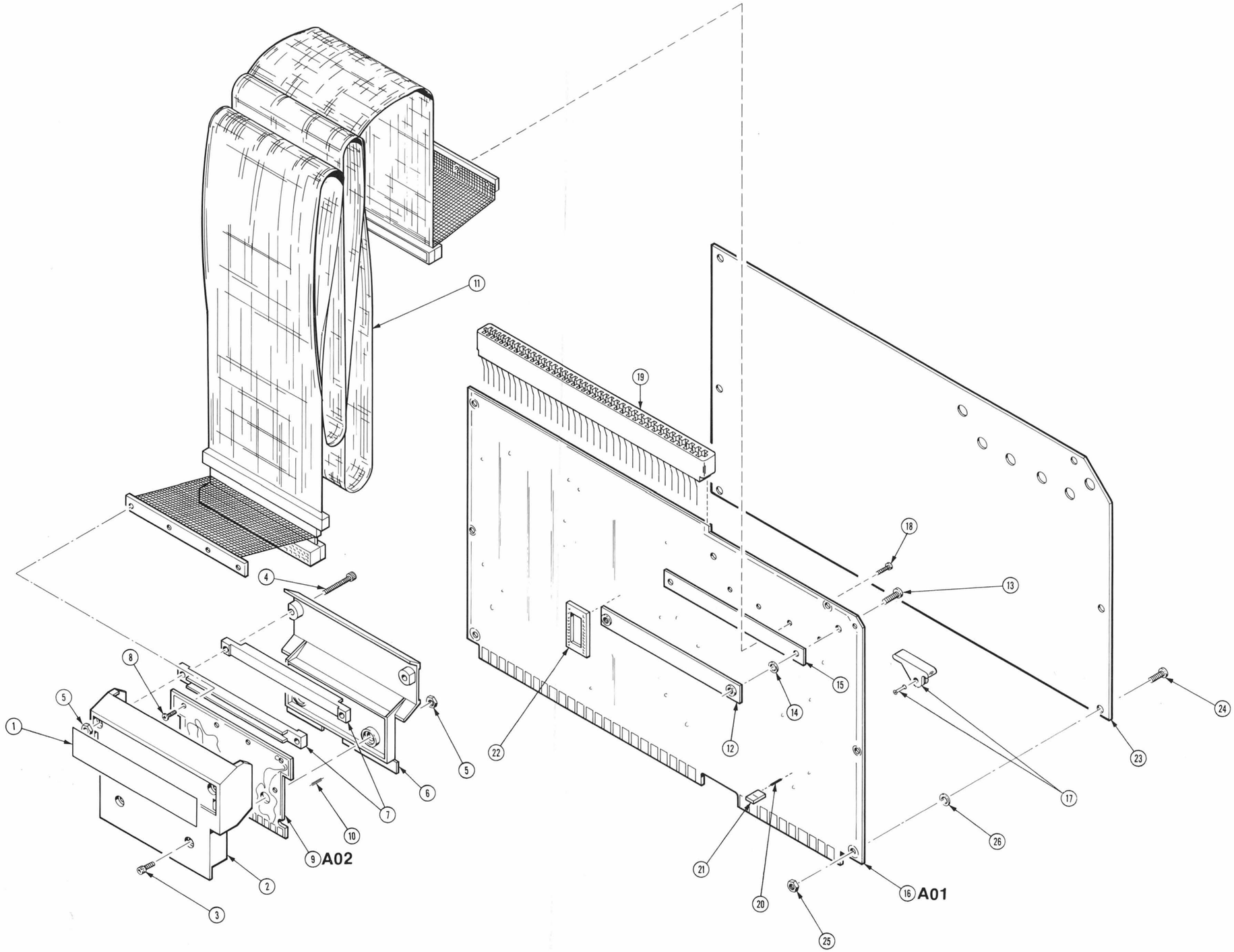


FIGURE 1 EXPLODED

PM112

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
	070-4288-00			1		MANUAL,TECH:INSTRUCTION	80009	070-4288-00
						OPTIONAL ACCESSORIES		
	012-0655-01			1		LEAD SET,ELEC:INPUT,W/10 40CM L WIRES	80009	012-0655-01

SIGNAL GLOSSARY

This section contains an alphabetical listing of all the signals which go to or from the PM 112 Personality Module, and a brief description of what each signal does.

A23-A0 — **PM 112 Address Lines (24 lines).** These lines are labeled as AI23-AI0 on circuit diagrams. A19-A0 carry Multibus address information to the logic analyzer (the Multibus address bit values are inverted by the PM 112's firmware to appear active high to the user). A10-A0 are bidirectional and are used to address the PM 112's PROM, following the completion of data acquisition. A23 is used to carry INTR(L) (also firmware inverted), and lines A22-A20 are used to carry IPR(H). In newer Multibus systems using 24 address lines, the four most significant address bits can be monitored using the PM 112's UDC lines.

AACK(L) — **Multibus Advance Acknowledge Signal.** In some early versions of the Multibus specification, a master that detects AACK(L)=0 may avoid some wait states. In later versions of the bus specification, this line is redefined as LOCK(L). See LOCK(L) listing in this glossary.

ACLO(H) — **Multibus AC Low Signal.** This signal is produced by the power supply when ac voltage drops, indicating dc power failure is imminent. (This line is reserved and not bussed in the IEEE P796 bus specification.)

ADR0(L)-ADR17(L) — **Multibus Address Lines (24 lines).** The original Multibus specification called for 20 address lines (ADR0(L)-ADR13(L)). Newer Intel and IEEE specifications provide 24 lines, the upper four being carried on the P2 connector of the board. The PM 112 has test point pins for these upper four address lines, allowing the user to connect them to UDC lines with jumper wires.

AI23-AI0 — **PM 112 Address Lines.** See A23-A0.

ALE(H) — **Multibus Address Latch Enable Signal.** A signal used by the CPU to enable an auxiliary address latch. (This line is reserved in the IEEE P796 bus specification.)

BD RESET — **Multibus Board Reset Signal.** BD RESET is an externally generated signal used to initiate a power-up sequence, and is carried on P2 connector pin 36. (This line is reserved and not bussed in the IEEE P796 bus specification.)

BCLK(L) — **Multibus Bus Clock Signal.** This signal is used to synchronize bus contention logic. It may be slowed, stopped, or single-stepped.

BHEN(L) — **Multibus Byte High Enable Signal.** In systems having 16-bit memory and I/O modules, the most significant byte of a 16-bit data word is enabled by BHEN(L)=0.

BPRO(L) — **Multibus Bus Priority Out Signal.** Used with serial (daisy chain) bus priority resolution, BPRO((L)=0 is passed to the BPRN(L) input of the master currently next highest in priority.

BPRN(L) — **Multibus Bus Priority In Signal.** A master that detects BPRN(L)=0 is assured that no bus requests of higher priority are pending.

BREQ(L) — **Multibus Bus Request Signal.** Used with parallel bus priority resolution, a master uses BREQ(L)=0 to request bus control.

BUSY(L) — **Multibus Bus Busy Signal.** The current bus master generates BUSY(L)=0 to maintain control of the bus. BUSY(L) goes high when the bus is inactive, or when a Bus Exchange is taking place. The PM 112 always inverts this signal to form BUSY(H), except at Test Point TP1027-3 and in generation of BUSY(L) as a self-test stimulus. To generate the PM 112 CLK(H) and CLK(L) signals, the falling edge of BUSY(H) is ORed with the falling edge of XACK(L).

C9-C0 — **PM 112 Control lines.** These lines are labeled as CI9-CI0 on circuit diagrams. This is a loosely defined category of signals from the PM 112 to the logic analyzer, which fall into the following subcategories of use:

- C0 through C3 are available for word recognition and are stored by the logic analyzer's acquisition memory.
- C4 and C5 are available for word recognition and clock qualification, but are not stored by the acquisition memory.

- C6 through C9 are available for clock qualification, but are not available for word recognition and are not stored.

C9-C0 are assigned to the following signals:

C0: R(H)/W(L)	C5: INH2(L)
C1: MEM(H)/IO(L)	C6: CBRQ(L)
C2: INTA+AVAL(H)	C7: AACK(L)
C3: BHEN(L)	C8: ACLO(H)
C4: INH1(L)	C9: BUSY(H)

CBRQ(L) — **Multibus Common Bus Request Signal.** CBRQ(L)=0 indicates that a master wants control of the bus. Conversely, CBRQ(L)=1 indicates to the bus master that it may retain control of the bus.

CCLK(L) — **Multibus Common Clock Signal.** This is a constant frequency, active low clock signal. It is generated by a single master and used as the system clock.

CI9-CI0 — **PM 112 Control Lines (see C9-C0).**

CLK(H), CLK(L) — **PM 112 Clock Signals.** These differential ECL signals cause the logic analyzer to perform an acquisition strobe. The CLK signals are generated by ORing the falling edge of XACK(L) with the rising edge of BUSY(L).

D7-D0 — **PM 112 Data Lines (least significant byte).** These lines are labeled as DI7-DI0 on circuit diagrams. The Multibus data bus values are inverted by the PM 112's firmware to appear active high to the user. These lines are also used to carry information from the PM 112's PROM, following the completion of data acquisition.

D15-D8 — **PM 112 Data Lines (most significant byte).** These lines are labeled as DI15-DI8 on circuit diagrams. The Multibus data bus values are inverted by the PM 112's firmware to appear active high to the user. These 8 lines are also used to carry UDC7-UDC0 when BHEN(L)=1.

DAT0(L)-DATF(L) — **Multibus Data Lines.** Sixteen bidirectional data lines are available for 16-bit systems (the Multibus BHEN(L) signal enables the high data byte on 16-bit data transfer operations). Only DAT0(L)-DAT7(L) are used with 8-bit systems.

DI15-DI0	**PM 112 Data Lines.** See D15-D8 and D7-D0.
HALT(L)	**Multibus Halt Signal.** HALT(L)=0 indicates that the CPU is halted. (This line is reserved and not bussed in the IEEE P796 bus specification.)
HALT SUT(L)	**Logic Analyzer Halt System Under Test Signal.** This signal (called HALT PUT on 7D02 circuit diagrams) is generated by the logic analyzer. If selected in the trigger menu, the HALT SUT(L) signal goes low when data acquisition is completed. HALT SUT can only be accessed via a square pin on the personality module. It must be connected to the appropriate SUT line using a jumper wire. If you connect this signal, be sure that there is no electrical contention with an existing Halt line input to the microprocessor.
INH1(L)	**Multibus Inhibit RAM Signal.** INH1(L)=0 prevents RAM from responding to addresses and commands on the bus, thus enabling ROM and memory-mapped I/O devices to share RAM addresses.
INH2(L)	**Multibus Inhibit ROM Signal.** INH2(L)=0 prevents ROM from responding to addresses and commands on the bus, allowing shadow ROMs to share memory space.
INIT(L)	**Multibus Initialize Signal.** INIT(L)=0 resets the entire system to a known state.
INTA(L)	**Multibus Interrupt Acknowledge Signal.** This signal is generated by the bus master in response to an interrupt request. This causes the interrupt status to freeze and the interrupt vector address to be placed on the data bus.
INTA+AVAL(H)	**PM 112 Interrupt Acknowledge + Bus Available Signal.** This signal is generated by PM 112 hardware from the Multibus MWTC(L), MRDC(L), IORC(L), IOWC(L), INTA(L), and BUSY(L) signals. INTA+AVAL(H)=1 indicates either an Interrupt Acknowledge cycle or a cycle on which the bus is available (i.e., not Busy, no master has control of the bus). The R(H)/W(L) line can be used to distinguish these two cycles from each other.
IPR	**PM 112 Interrupt Priority Lines (3 lines carried on A22-A20).** This is a 3-bit word

recognizer field into which the PM 112 hardware encodes the Multibus INT0(L)-INT7(L) signals. The value of the IPR field on any given cycle is the number of the highest priority pending request, where 0 is the highest possible priority, and 7 is the lowest. In the data display I field (interrupt request information) a "." indicates that no requests are pending.

INT0(L)-INT7(L) **Multibus Interrupt Request Signals (8 lines).** Used for parallel resolution of interrupt priority. INT0(L) is the highest priority and INT7(L) is the lowest.

INTR(L) **PM 112 Interrupt Request Signal (carried on A23).** This signal is generated by the PM112 hardware from the Multibus INT0(L)-INT7(L) lines, and is then inverted by PM 112 firmware to appear active high to the user. The signal indicates that an interrupt has been requested.

IORC(L) **Multibus I/O Read Command.** This signal indicates that the address of an I/O port is on the address bus, and that the port's output should be placed on the data bus.

IOWC(L) **Multibus I/O Write Command.** This signal indicates that the address of an I/O device is on the address bus, and that the port should output the information on the data bus.

LOCK(L) **Multibus Lock Signal.** This signal is used by a master when locked access to the bus during read-modify-write cycles is required.

LOOK(H) **Logic Analyzer Look Signal.** This is a control signal from the logic analyzer to the PM 112. It serves to tri-state some of the personality module input buffers, preventing electrical contention from them when it reads the personality module's PROM.

MEM(H)/IO(L) **PM 112 Memory/IO Line.** The signal is generated by PM 112 hardware from the Multibus MWTC(L), MRDC(L), IOWC(L), IORC(L), INTA(L), and BUSY(L) signals. MEM(H) or I/O(L)=1 normally indicates that a data transfer is to or from memory. MEM(H)/IO(L)=0 normally indicates that an I/O operation of some type is taking place.

MPRO(L) **Multibus Memory Protect Signal.** When dc power is faulty, this signal prevents memory operation by inhibiting memory requests. MPRO(L) is

carried on P2 connector pin 20. (This line is reserved and not bussed in the IEEE P796 bus specification.)

MRDC(L) **Multibus Memory Read Command.** This signal indicates that the address on the bus is valid, and that the contents of that address are to be placed on the data bus.

MWTC(L) **Multibus Memory Write Command.** This signal indicates that the address on the bus is valid and that the information on the data bus is to be written there.

PAR1(L), PAR2(L) **Multibus Parity Lines 1 and 2.** These signals are located on the P2 connector at pins 27 and 29, respectively. (These lines are reserved and not bussed in the IEEE P796 bus specification.)

PFIN(L) **Multibus Power Fail Interrupt Signal.** This signal interrupts the processor when a power failure has occurred. It is driven by an auxiliary power source, and is carried on P2 connector pin 19. (This line is reserved and not bussed in the IEEE P796 bus specification.)

PFSN(L) **Multibus Power Fail Sense Signal.** This signal indicates that a power failure has occurred. It is driven by an auxiliary power source, and is carried on P2 connector pin 17. (This line is reserved and not bussed in the IEEE P796 bus specification.)

PFSR(L) **Power Fail Sense Reset Signal.** This signal resets PFSN(L). It is carried on P2 connector pin 13. (This line is reserved and not bussed in the IEEE P796 bus specification.)

PLC(H) **Multibus Power Line Clock.** Carried on P2 connector pin 31. (This line is reserved and not bussed in the IEEE P796 bus specification.)

R(H)/W(L) **PM 112 Read/Write Line.** This signal is generated by the PM 112 hardware from the Multibus MWTC(L), MRDC(L), IOWC(L), IORC(L), INTA(L), and BUSY(L) signals. R(H)/W(L)=1 normally indicates that a Read operation of some type is taking place, and R(H)/W(L)=0 normally indicates a Write operation.

RESET(L) **Multibus Reset Signal.** This signal initiates a power-up sequence. It is carried on P2 connector pin 36. (This line is reserved and not

bussed in the IEEE P796 bus specification.)

SELP(L)

Logic Analyzer Select PROM Signal. This is a control signal from the logic analyzer to the PM 112. SELP(L) enables the PM 112 PROM to be read by the logic analyzer.

UDC7-UDC0

PM 112 User-Defined Control Lines. These user-definable lines can be used to monitor a variety of Multibus signals. These signals are accessed with movable jumper straps and/or flying leads. They are carried on the PM 112's data lines D15-D8 when 8-bit bus transactions are performed by the SUT (or whenever BHEN(L)=1). For use with 16-bit processors, a jumper is provided on the PM 112 hardware to force BHEN(L)=1 (as seen by the PM 112) on all cycles.

The most significant eight data bits in the logic analyzer's word recognizer menu can be used for UDC7-UDC0 values as well as for data -- see WORD RECOGNIZER MENU and USING UDC LINES in Operation Instructions section.

The default assignments of the UDC lines are as follows:

UDC0: MRDC(L)	UDC4: INTA(L)
UDC1: MWTC(L)	UDC5: INH2(L)
UDC2: IORC(L)	UDC6: LOCK(L)
UDC3: IOWC(L)	UDC7: INH1(L)

WAIT(L)

Multibus Bus Master Wait State Signal. This signal indicates that the master's processor is in a wait state. (This line is reserved and not bussed in the IEEE P796 bus specification.)

XACK(L)

Multibus Transfer Acknowledge Signal. A slave module uses this signal to acknowledge that a master's command has been executed, and that information has been received from or placed onto the data lines. The PM 112 uses the falling edge of this signal ORed with the rising edge of BUSY(L) to generate the PM 112 CLK(H) and CLK(L) signals. This in turn causes the 7D02 to generate an acquisition strobe.