Engineering News

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IDG's Evolving Family Look

In October, Information Display Group's Industrial Design department gave fifteen presentations to a cross-section of Tektronix employees. The presentations had two purposes. One was to identify Industrial Design's role in product development. The other purpose was to show where IDG is now in the evolution of its family look.

Stu Whitcomb, IDG Industrial Design manager, began the presentation with a description of Industrial Design's role and a definition of its charter. He explained that Industrial Design is an active member of each product development team, which includes manufacturing, engineering, and marketing. Part of Industrial Design's role is to be the generalist on the team, to be in a position to propose appearance designs that satisfy the special needs of the other team members.

Figure 1. IDG Industrial Design Manager, Stu Whitcomb.

Engineering's role is to solve electrical and mechanical design problems and to manage development costs. Marketing watches the competition, listens to customers and potential customers, and then defines the features that the products should have and the performance levels the products should attain. In the early stages of product development, manufacturing gives the rest of the team insight into the least expensive and most convenient ways to manufacture the product.

Stu briefly described the IDG family look, and then introduced industrial designers Maki Myoga and Al Correa. Maki and Al talked about the requirements that affect every product's appearance. Those requirements are man-machine interface (also called "human factors"), family identity, product identity, aesthetics, and function.

HUMAN FACTORS

The narrators illustrated the human factors requirements with diagrams. By defining viewing angles and keyboard placement for the average male and female, they showed how industrial design can control crt reflections and awkward keyboard heights.

FAMILY LOOK

Since IDG's products often are used together, one of Industrial Design's goals is to maintain a consistent appearance so that customer or potential customer can identify the products as a family. At the same time, he should be able to identify the product family with the Tektronix image.

AESTHETICS

The narrators also talked about aesthetics: using color, proportion, and shape to make the product more appealing to the customer. They went on to explain the practical value of graphic delineation (using color contrasts, for example) to give visual impact and a sense of organization to the control and viewing areas.

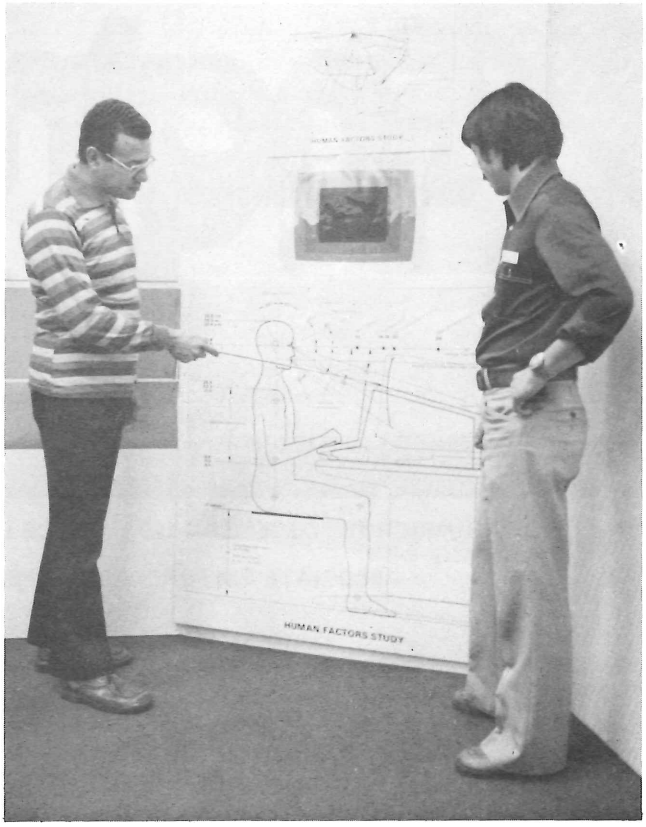


Figure 2. Industrial Designers Al Correa (left) and Maki Myoga make a point regarding human factors.

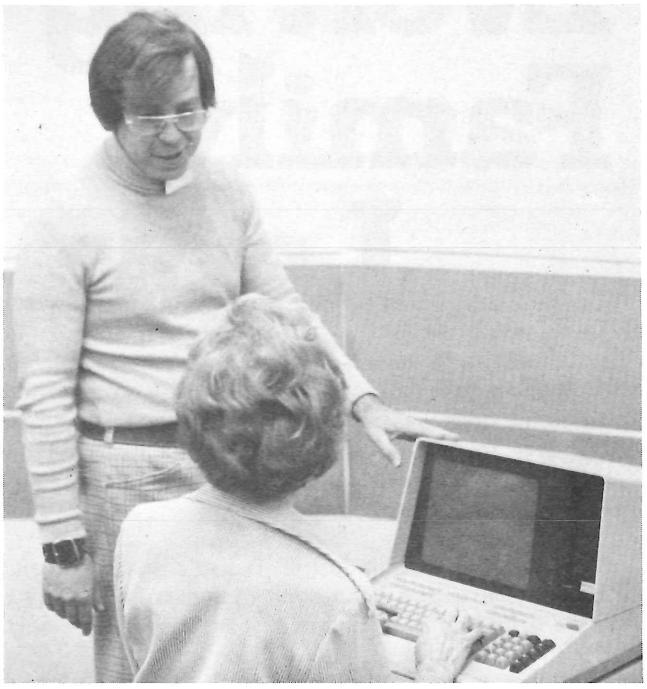


Figure 3. Stu Whitcomb and Ruth Miller role playing keyboard requirements.

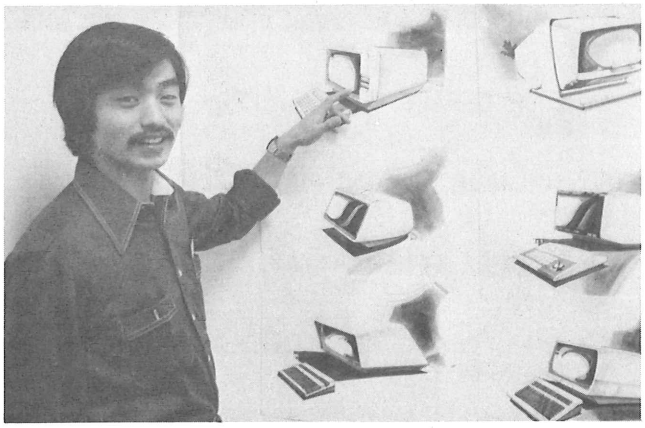


Figure 4. Designer Maki Myoga recounts some early design proposals.

FUNCTION

Function, which affects every product's appearance, was the last requirement discussed. One function is manufacturing flexibility, an example of which is modularity. Modularity allows development money to be put into one component that can be used in different ways, instead of spreading the money over several one-shot designs. That allows us to produce a single sophisticated design.

Al and Maki used a series of large design sketches to illustrate their points. They leafed through background sketches for keyboards, monitors, peripherals and desks. Each sketch represented a rejected alternative. There were a lot of them.

Each sketch represents a compromise. Part of Industrial Design's job is to reconcile conflicting demands. Engineering, marketing, and manufacturing inputs are seldom directly compatible.

For example, there's a lot of price-competition in the IDG marketplace. Raising prices to cover greater development and production costs would lose customers for the product line. Yet there's a need to give the product a rich look that's appealing to customers working in a business environment. Industrial Design's job, then, is to recommend design and assembly concepts that will combine the rich appearance with low-cost development and production. A skillful use of color, shape, and proportion can enhance the appearance while still keeping a lid on costs.

SLIDE SHOW

The next part of the presentation was a slide-show view of Tektronix' competition. The narrator used two slide projectors to compare the Tektronix family look to the family look of other companies. In the last segment of the slide show, the audience saw Industrial Design's current recommendations as they would appear in a typical customer environment.

A question-and-answer period ended the presentation. It offered two-way communication. Stu Whitcomb answered questions for the Industrial Design group, and the industrial designers were able to make contact with people outside of IDG. For example, Tom Bohan (manager of Engineering Support in the T and M operations group) pointed out several projects in T and M that could affect Industrial Design's recommendations. Until now, Industrial Design has been relying mostly on IDG input and outside vendors for alternatives.

After the question-and-answer period, the audience was treated to a hands-on and sit-down experience. On stage were full-scale models of some proposed products. There were desks, monitors, keyboards, a plotter and a standard rack cabinet modified to fit Industrial Design's recommended family look.

The show was a good model for anyone setting up a presentation. There were slides, sketches, handout sheets, and models available for hands-on. The fast pace of the presentation and the multimedia approach kept the audience tied to the subject.

The Industrial Design group accomplished what it set out to do. . .present concepts for IDG's product family, and identify Industrial Design's role in product development.

Unfortunately, we can't show you Industrial Design's most recent suggestions for the IDG family look. . .the competition may be watching. That COMPANY CONFIDENTIAL label on the top of the front page should protect the contents. But it may only be attracting attention instead. However, the IDG industrial designers will be happy to help satisfy your curiosity. Call extension 2552 in Wilsonville.

Scientific Computer Center

CURVET CAN DO MORE, NOW

CURVET is a routine on the Scientific Computer Center's Cyber Computer system. CURVET presents characterization information based on dc parameters of BJT's and other three-terminal devices that you can put into the SPICE2 input format. (SPICE2 is a general-purpose program that simulates circuits for linear ac analysis, and non-linear dc and transient analysis).

Recently the Scientific Computer Center added three new plot types and two new capabilities to the CURVET routine. The new plot types are:

- beta-ac versus frequency.
- f_T versus frequency.
- junction capacitance versus junction voltage.

The two new capabilities are:

- plotting data points along with the calculated curve.
- reading control information from a local file that the user has set up to specify the type of analysis he wants (this saves the user the time it takes to type the control information again and again).

Before you enter CURVET you'll need to set up a file that contains a description of the device model. Use the .MODEL or .SUBCKT input format of SPICE2. To start execution of CURVET, enter:

–CURVET (M=MODFILE)

where MODFILE is the name of the model file.

If you want to compare measured data points with the calculated curve, add the D=DFILE parameter to the CURVET call:

–CURVET (M=MODFILE, D=DFILE)

```
ENTER ANALYSIS TYPE(1,2,3,4)
      1) DC TRANSFER CURVES
      2) IC, IB VS VBE (BETA VS IC)
      3) BETAAC VS FREQ & FT VS IC
      4) JUNCTION CAPACITANCE VS VOLTAGE
? 3

TYPE OF DEVICE ? (NPN,PNP)
? NPN

DO YOU WANT BETAAC PLOTS ? (Y,N)
? Y

FREQ SWEEP (FMIN FMAX)
? 1K 1G

IC (MIN MAX NO. OF PTS/DECADE)
? .3M 300M 1

ENTER VCB
? 10

ENTER TITLE FOR PLOT
? 151-0190-00 CHARACTERISTICS
```

Figure 1. Dialogue for obtaining AC BETA versus frequency.

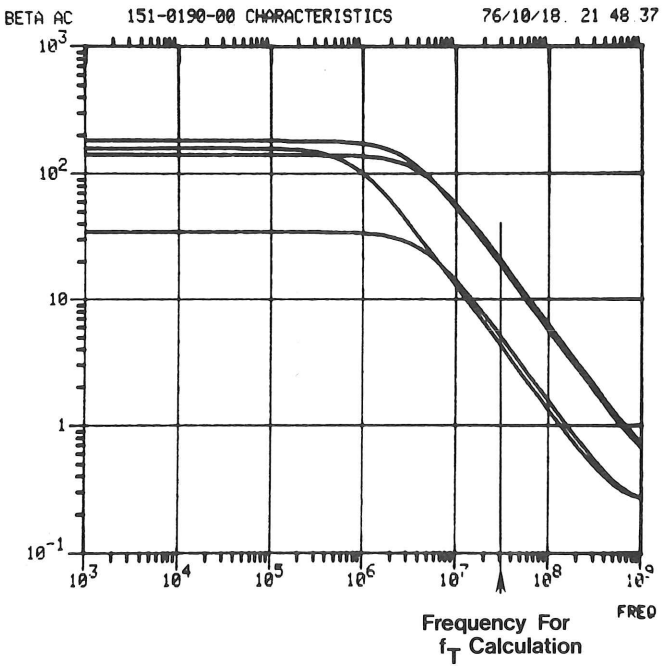


Figure 2. AC BETA curves showing how to determine the frequency for f_T calculations.

DFILE is the data-point file. When you set up the file, use this format:

format:	example:
title	FTDATA
data header	IC FT
	IM 300MEG
	3M 550MEG
data	10M 700MEG
	30M 620MEG
	100M 350MEG

There are several rules for setting up the data-point file:

- the number of columns of data (there are two in the example above) must equal the number of traces you asked for, plus one.
- each column of data must have a header.
- the order of the columns must match the order of the headers (the headers may be in any order, however).

The ENTER ANALYSIS TYPE (1,2,3,4) question comes up as soon as you enter CURVET. Which header you use depends on how you answer the question:

analysis type	header
1	VCE IC IC ...
2	VBE IB IC
3	IC FT
4	CJ VJ

The second capability that has been added is having CURVET read its control information from a local file rather than only from the keyboard. This capability is especially useful if you are using the same control information again and again . . . like when you're adjusting a model to fit some measured results. To get CURVET to read the local file, add the INPUT=CFILE parameter to the CURVET call:

—CURVET (M=MODFILE, D=FILE, INPUT=CFILE)

There are two new analysis types, 3 and 4. Type 3 lets you plot f_T against your device's collector current. Before you do that, though, you'll need to run beta-ac plots to determine which frequency you'll need for the f_T calculation. Figure 1 shows the dialogue between CURVET and the user. Figure 2 shows the beta-ac plot called for in figure 1. At the frequency used for calculating f_T all of the curves must be rolling off at 20 dB/decade.

```
ENTER ANALYSIS TYPE(1,2,3,4)
     1) DC TRANSFER CURVES
     2) IC, IB VS VBE (BETA VS IC)
     3) BETAAC VS FREQ & FT VS IC
     4) JUNCTION CAPACITANCE VS VOLTAGE
? 3

TYPE OF DEVICE ? (NPN,PNP)
? NPN

DO YOU WANT BETAAC PLOTS ? (Y,N)
? N

FREQ FOR FT CALCULATION & OPTIONAL PLOT
LIMITS FTMIN,FTMAX
? 30MEG

IC (MIN MAX NO. OF PTS/DECADE)
? .3M 300M 10

ENTER VCB
? 10

ENTER TITLE FOR PLOT
? 151-0190-00 CHARACTERISTICS
```

Figure 3. Dialogue for f_T versus collector current.

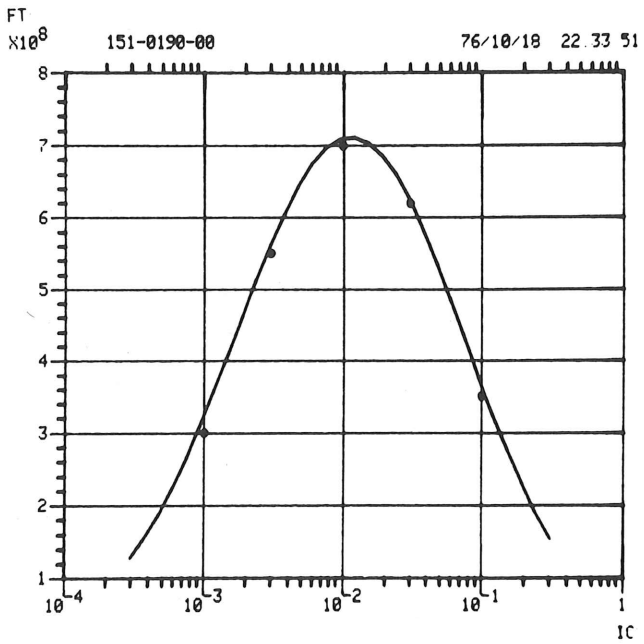


Figure 4. F_T versus collector current with user data points.

Once you've got the calculation frequency, you can go through the ENTER ANALYSIS TYPE sequence again, but this time ask for a plot of f_T against Ic. Figure 3 shows the sequence. Figure 4 shows the plot. The data-point file for the plot is the same as the example we looked at when we talked about DFILE.

Analysis type 4 lets the user plot junction capacitance against junction voltage. Figure 5 shows the sequence. Figure 6 shows the plot that results. Figure 7 shows the data-point file for the plot. There are a couple of things you should notice. First, note that positive voltage corresponds to forward bias. Second, for type 4 analysis you don't need to set up a model file.

If you have any questions, you can type HELP,CURVET or call Ron Bohlman at extension 5866.

```
ENTER ANALYSIS TYPE(1,2,3,4)
     1) DC TRANSFER CURVES
     2) IC, IB VS VBE (BETA VS IC)
     3) BETAAC VS FREQ & FT VS IC
     4) JUNCTION CAPACITANCE VS VOLTAGE
? 4

ENTER CJO PHI M CK & OPTIONAL FC
? 1P 1 .5 .1P

ENTER VMIN VMAX DELTAV & OPTIONAL PLOT
LIMITS CMIN CMAX
? -5 .4 .1

ENTER TITLE FOR PLOT
? PN JUNCTION CAPACITANCE
```

Figure 5. Dialogue for junction capacitance versus voltage plot.

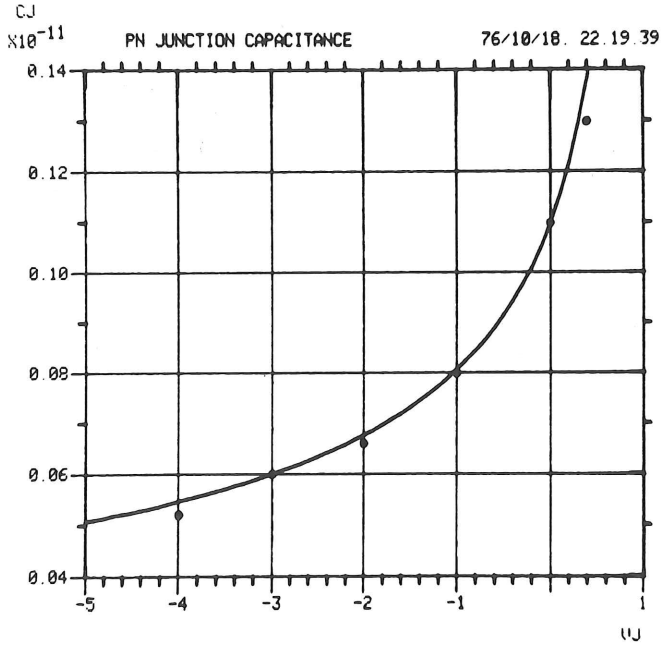


Figure 6. Junction capacitance plot with user data points.

```
CAPACITANCE DATA
VJ  CJ
-4   .52P
-3   .6P
-2   .66P
-1   8P
 0  1.1P
.4  1.3P
```

Figure 7. Data file for junction capacitance points.

Scientific Computer Center

More on FORTRAN Standard

In their July meeting, the ANSI (X3J3) FORTRAN Standards Committee amended FORTRAN/76 so that it would include an IF—THEN—ELSE block control structure. The FORTRAN Standards Committee accepted the IF—THEN—ELSE block control structure described in a Scientific Computer Center article in the May 1976 issue of *Engineering News*. . .with one exception: the keyword THEN will be mandatory in block IF statements.

The FORTRAN standards committee will complete the FORTRAN/76 definition within the next couple of months. In the meantime, the working document is well worth looking at.

The following (part of the committee's working document dated August 24, 1976) is a list of the known conflicts between FORTRAN/76 and the previous standard X3.9-1966 FORTRAN.

I/O

Reading into a Hollerith edit (field) descriptor in a FORMAT statement is prohibited in this standard.

A simple I/O list enclosed in parentheses is prohibited from appearing in an I/O list.

This requires that parentheses enclosing more than one I/O list item must mark an implied DO-loop. The restriction was imposed to eliminate potential syntactic ambiguities introduced by complex constants in list-directed output lists. As all the parentheses referred to are redundent, a program can be made conforming with this standard by deleting redundant parentheses enclosing more than one list item in an I/O list.

This restriction corrects what was thought to be an oversight in X3.9-1966.

Negative values for input/output unit identifiers are prohibited in this standard. X3.9-1966 did not prohibit them.

The range of a scale factor for E, D, and G output fields is restricted to reasonable values. X3.9-1966 had no such restriction, but did not provide a clear interpretation of the meaning of the unreasonable values.

The definition of an entity associated with an entity in an input list occurs at the same time as the definition of the list entity. X3.9-1966 delayed the definition of such an associated entity until the end of the input statement.

A sequential file may not contain both formatted and unformatted records. A published interpretation of X3.9-1966 specified that this was permitted.

A record must not be written after an endfile record in a sequential file. X3.9-1966 did not prohibit this, but provided no interpretation for the reading of an endfile record.

Following the E or D in an E and D output field, a + or - is required immediately prior to the exponent field. This improves compatibility with other American National Standards for numeric data interchange. X3.9-1966 permitted a blank as a replacement for + in the exponent sign.

On output, the F edit descriptor must not produce unnecessary leading zeros.

A processor must not produce a numeric output field containing a negative zero. X3.9-1966 required this if the internal value of a real or double precision datum was negative.

INTRINSICS

More intrinsic function names have been added and could conflict with the names of subprograms. These names are ACOS, ANINT, ASIN, COSH, DACOS, DASIN, DCOSH, DDIM, DFLOAT, DNINT, DPROD, DSINH, DTAN, DTANH, IDNINT, LEN, LOG, LOG10, MAX, MIN, NINT, SINH, and TAN.

An intrinsic function name that is used as an actual argument must appear in an INTRINSIC statement rather than

an EXTERNAL statement. Note that the intrinsic function class includes the basic external function class of X3.9-1966.

The units of the arguments and results of the intrinsic functions (and basic external functions) were not specified in X3.9-1966 and are specified in this standard. The range of the result has also been specified. These specifications may be different from those used on some processors conforming to X3.9-1966.

HOLLERITH

Hollerith constants and Hollerith data are not permitted in this standard. X3.9-1966 permitted the use of Hollerith constants in DATA and CALL statements, the use of non-character list items in formatted input/output statements with A edit descriptors, and the referencing of noncharacter arrays as formats. Note that the Hollerith edit (field) descriptor is permitted; it is not a Hollerith constant.

EQUIVALENCE

Only one-dimentional arrays may have a one-dimensional subscript in an EQUIVALENCE statement. X3.9-1966 permitted two-and three-dimensional arrays to have a one-dimensional subscript in an EQUIVALENCE statement.

TYPE

Redundant type specifications are prohibited in this standard. X3.9-1966 did not explicitly have such a prohibition.

SUBSCRIPTS

The value of a subscript expression must not exceed its upper bound. X3.9-1966 permitted a subscript expression value to exceed its upper bound if the maximum subscript value was not exceeded.

CONTINUATION

Columns 1 through 5 of a continuation line must contain blanks. A published interpretation of X3.9-1966 specified that columns 1-5 of a continuation line may contain any character from the FORTRAN character set except that column 1 must not contain a C.

END

A labeled END statement could conflict with the initial line of a statement in an X3.9-1966 standard-conforming program.

PORTABILITY

Because the collating sequence has not been completely specified, character relational expressions do not necessarily have the same value on all processors.

Character data, H edit descriptors, apostrophe edit descriptors, and comment lines may include characters that are acceptable to one processor but unacceptable to another processor.

No explicit requirements are specified for file names. A file name that is acceptable to one processor may be unacceptable to another processor.

Input/output unit numbers and unit capabilities may vary among processors.

If you have any questions or comments, call Roy Carlson at extension 7668 or drop by 50-454.

M175: Strobed Comparator

A new, ultrafast strobed voltage comparator has been designed, built, and evaluated in Monolithic Circuits Engineering. A strobed comparator makes comparisons only on command. This is different than the more familiar comparators which compare two inputs continuously.

Strobed comparators have unique advantages in clock-driven a/d converter applications, logic analyzer inputs, and digital test systems. Comparisons can be made much faster with less power dissipation than with conventional comparators. Aperture uncertainty is greatly reduced, which minimizes the need for sample and hold circuitry.

This particular realization is in a master-slave configuration to display the digital output for a full clock cycle. There are two complete comparators in each IC, driven by a common strobe input. Outputs are differential currents through common-base NPN buffers.

The M175 is one of the first products built using the new SHF III bipolar IC process. Samples of the M175 are available from the designer, Steven Wetterling, ext. 6283. New applications or requests for modified versions are welcome.

Comparison Decision Time	less than 500 ps
Strobe Maximum Repetition Rate (Period)	200 MHz (5 ns)
Input Bandwidth (as an amplifier)	greater than 800 MHz
Resolution	+5 mV or less
Input Range	+125 mV
Output	8 mA through either of two common-base buffer transistors
Power	12-volt supply 1.2 watts

Figure 1. Performance Characteristics of the M175 Strobed Comparator.

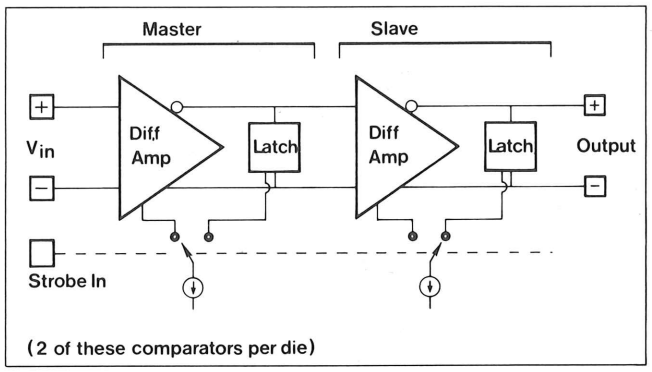


Figure 2. Block diagram of a strobed comparator.

DSP Video Series Planned

The M.I.T. Center for Advanced Engineering Study has developed a Digital Signal Processing course consisting of a set of video-tape lectures and a study guide. The lectures and study guide are companions to the text, "Digital Signal Processing" by A.V. Oppenhiem and R.W. Shafer. Dr. Oppenhiem is the lecturer in the tapes.

Tektronix is considering purchasing the lecture series for showing in the Technical Center Auditorium. The format of presentation will be similar to that of the TI microprocessor tape series of last winter. Tentatively, the course will start in January 1977, and will run for ten weeks.

The series of lectures and demonstrations begins with the definitions of discrete time signals and systems. Topics covered include difference equations, discrete time Fourier transforms, the z-transform, digital filter design and implementation, and the fast Fourier transform.

A survey is presently being conducted in order to determine the level of interest in the course at Tek. If you are interested in taking the course and have not been surveyed previously, contact Jim Smith of Integrated Circuit Engineering at extension 6210.

"CALL FOR PAPERS!"

If this interests you, give us a call (Technical Information, ext. 6071). We'll give you all the details you'll need (length and format of the paper, where and when to send it in).

The Society for Information Display International Symposium, is sponsoring a symposium (April 19-21, 1977) in Boston. They're asking for papers on terminals, graphics, human factors, display standards, and displays (flat-panel, CRT, projection, command and control). The program chairman first wants an abstract and a review summary (which can have illustrations), then the paper. The 35-to-40 word abstract and the 300-to-500 word summary are due December 13. By the time you read this, December 13 may seem too close to do anything. Let us know if you're interested, and we'll see if we can get the program chairman to extend the deadline a little.

IN PRINT...

In September, the **IEEE Transactions on Electron Devices** published a paper by Neil Gordon and Wesley Mickanin. The title of the paper is "Field-Enhanced Space-Charge-Limited Hole Currents in Thin-Oxide MNOS Varactors."

Neil Gordon joined Tektronix in September of this year; he works in Instrument Research. Wesley Mickanin joined Tektronix in June. Wesley works in Hybrid Circuits Engineering. If you would like a copy of the article, call the library at extension 5388. The article is in Vol. ED-23, No. 9, pages 995-997.

IN PRINT

In October, the **IEEE Transactions on Electron Devices** published a paper co-authored by Neil Gordon who works in Instrument Research. The title of the paper is "The Effects of Small-Amplitude Potential Changes on Non-equilibrium Minority-Carrier Charge Distribution in MIS Capacitors."

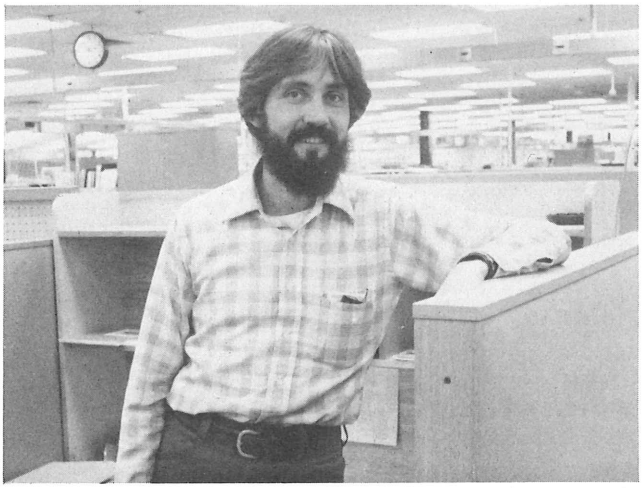
If you would like a copy of the article, call the library at extension 5388. The article is in Vol. ED-23, No. 10, pages 1144-1149.

IN PRINT

The October issue of **School Shop** contains an article written by Ralph Show, an instructor in the Education and Training Department. The title of the article is "Probing the Art of Probes." Written in a tutorial style, the article discusses choosing a probe, general probe theory, and the use of voltage and current probes. If you would like to have a copy, call Margit Pedisich, ext. 6386.

IEEE Approves Atlas As A Standard

In September, the IEEE Standards board approved ATLAS as a standard. ATLAS (the Abbreviated Test Language for All Systems) is a language used to define test specifications and procedures. ATLAS was developed by the avionics industry where it had international acceptance. ATLAS is now being used with automatic test equipment in other industries. Adoption of the language by IEEE will complement IEEE's instrumentation system standards.



If you have any comments or questions give Maris Graube a call at ext. 6234. Maris joined Tektronix in November. He will be the coordinator for all system interface projects . . . hardware, software, and firmware.

4051 APPLICATIONS LIBRARY NOW AVAILABLE

IDS has just announced the availability of a wide variety of user's programs in its new 4051 Applications Library.

New programs include Business Analysis, Sales Commission, Utilities and Graphics, to name a few.

Tek personnel who have written programs for the 4051 are urged to submit them to the 4051 Applications Library. Your program might be the one to help close a sale. In exchange for having a program included in the library, you may have a choice of 3 free programs.

New programs are continually being added to the library and abstracts will be published in each issue of the Applications Library Newsletter, a new IDS publication.

If you would like to have your name added to the mailing list for the Applications Library Newsletter, send your name and mailing station to A.L.N. 60-369.

Documentation instructions, submittal forms and order forms will be sent to those requesting them.

Logic Analyzer Presentation

On November 10, Dave Lowry presented a paper and slide show at the Mid-American Electronics Conference in Kansas City, Missouri. The title of the paper is "A Logic Analyzer Application." The subject of the paper was the use of a logic analyzer in troubleshooting an applications system. If you'd like a copy of the paper, give Dave a call at extension 6758 or drop by 39-155.

CALCULATOR INSURANCE

Tektronix is again offering insurance on hand-held calculators to Tek employees. The annual premium of $2.00 per hundred dollars of value covers a calculator from January 1, 1977 to January 1, 1978 through the Travelers Indemnity Company. The policy is available for calculators with a present retail value of $75 to $500. Calculators do not have to have been purchased through Tek in order to be insured. The enrollment period ends December 22. There is a $25 deductible applied to each claim.

For complete information and a schedule of premium charges, contact Nancy Mowlds, ext. 7679.

Editorial by Vern Johnson

Members of Service Support Staff want to encourage engineers to document everything unusual about new instruments. Of particular concern are operating modes or conditions that are normal for that instrument, but are not what a user would expect. The EIS is the best medium for this information since all field personnel have access to EIS's via microfiche. If you have any ideas or suggestions on this subject, call Vern Johnson on ext. 5767 or stop by 74-279.

OOPS!

In last month's Engineering News, on the first page, there was a simplified diagram of a braille-output adapter for Scientific Computer Center's line printer. The diagram is wrong. The elastic band should be between the hammer and the paper, not between the print-chain character and the paper. The way it's set up in the diagram, the line printer would produce nothing but a very worn elastic band. Thanks go to Charlie Montgomery for pointing out the error.

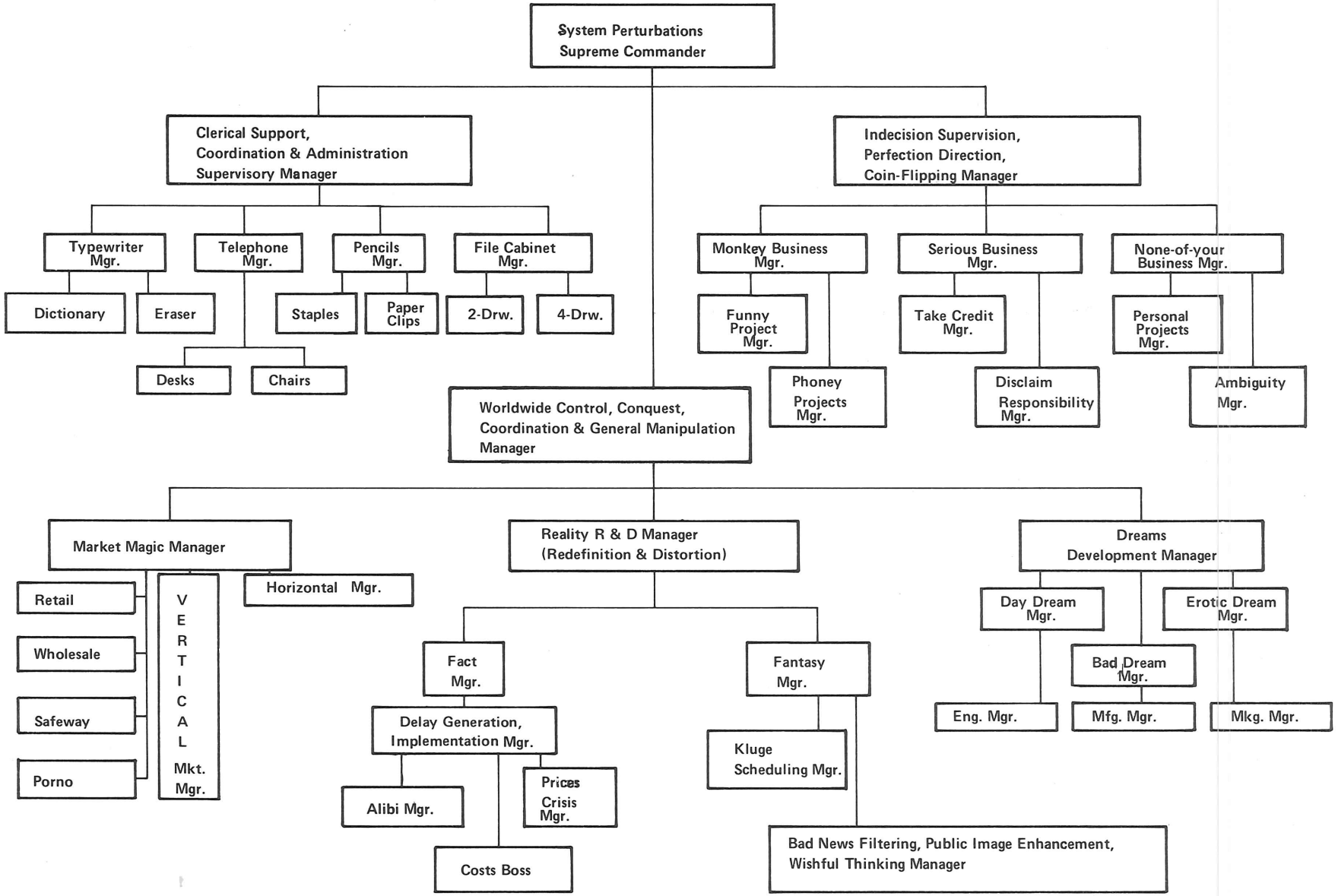
Second Engineering Forum

The topic of the second Engineering Forum, scheduled for late January, is A/D and D/A conversion. The purpose of every engineering forum is to give Tektronix engineers a chance to communicate their ideas to managers and to other engineers. If you would like to contribute to the January forum, Bob Nordstrom (50-316) and Mike Boer (58-79) invite you to submit a one-page description of your idea to them before December 14.

ORGANIZATION CHARTS

Due to the vast number of recent requests for organization charts, someone came up with a universal chart. This chart can be used for almost any company with more than 250 employees, and government bureaus with more than 60 people. To use this chart, just write appropriate names in applicable boxes.

(over)



DEPARTMENTAL LABOR STAFF

(6 Go-Fers, 3 Goats, 4 Illegal Aliens, 1 Kid with an H-P Calculator)

Maureen Key 60-553