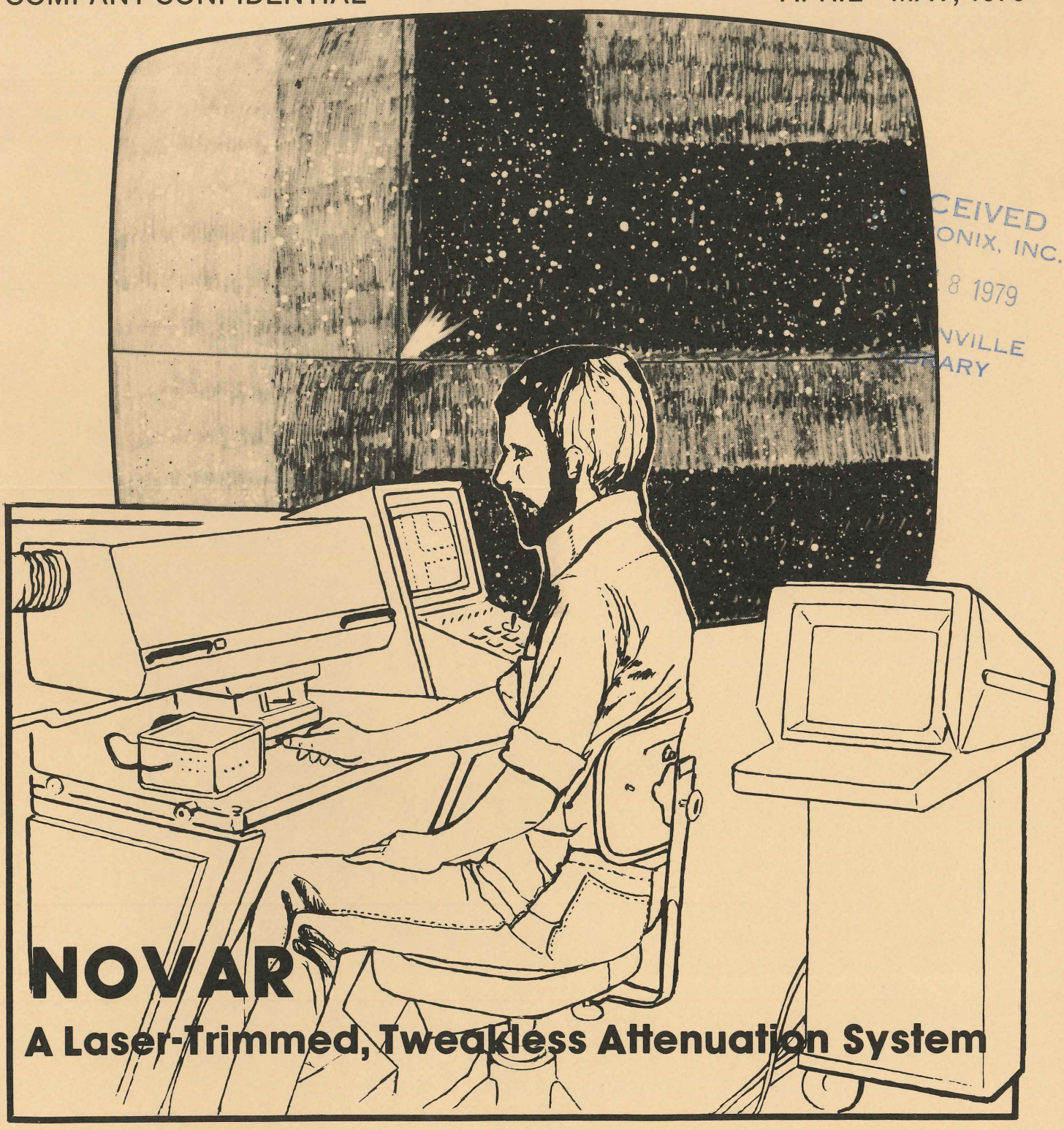
ENGINEERING NEWS

COMPANY CONFIDENTIAL

APRIL • MAY, 1979



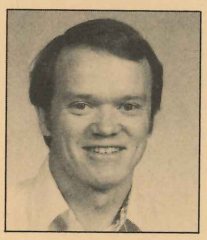
NOVAR

A Laser-Trimmed, Tweakless Attenuation System

NOVAR

A Laser-Trimmed, Tweakless Attenuation System

Ken Holland, Lab Scopes Engineering, ext. 7067 (Beaverton).



Des Murphy, High-Frequency Component Development, ext. 7033 (Beaverton).

John Stoops, High-Frequency Component Development, ext. 5289 (Beaverton).

TWEAKLESS ATTENUATORS

In 1976, High-Frequency Component Development began developing Novar, a tweakless attenuation system for the SC504 Oscilloscope. The attenuators in this system are functionally laser-trimmed, eliminating the need for any further calibration.

The SC504 design objectives placed severe demands on its attenuation system. Without sacrificing performance, the system had to be physically smaller, and have lower manufacturing cost than currently-used modular hybrid systems.

ADVANTAGES

As figure 1 shows, the Novar attenuation system is smaller and simpler than previously-used modular hybrid attenuation systems.

BACKGROUND

Until the late 1960's, high-impedance attenuators in Tektronix instruments were made with discrete components. Instrument bandwidths were low enough that designers needed to consider mainly the lumped parameter values of attenuator components. Attenuator switches had rotary-wafer structures that were bulky and frequently required significant front-panel space.

By the early 1970's, Tektronix instrument bandwidths were approaching 100 MHz. At that point, product designers had to begin considering the attenuator's distributed parameters. Another factor complicating design was component density: new product designs required more components in the same or smaller product enclosures. Designers were also aware that calibration was a significant element in the cost of attenuators.

New attenuator designs were needed that would bring higher bandwidths, smaller size, and lower costs.

By 1970, Tektronix engineers had designed modular hybrid attenuators that could be used as off-the-shelf attenuation system building blocks. These modular attenuators provided increased bandwidth, less hook, shorter product development cycles, and lower manufacturing costs. Since 1968, most Tektronix products requiring attenuator systems have used these modular attenuators.

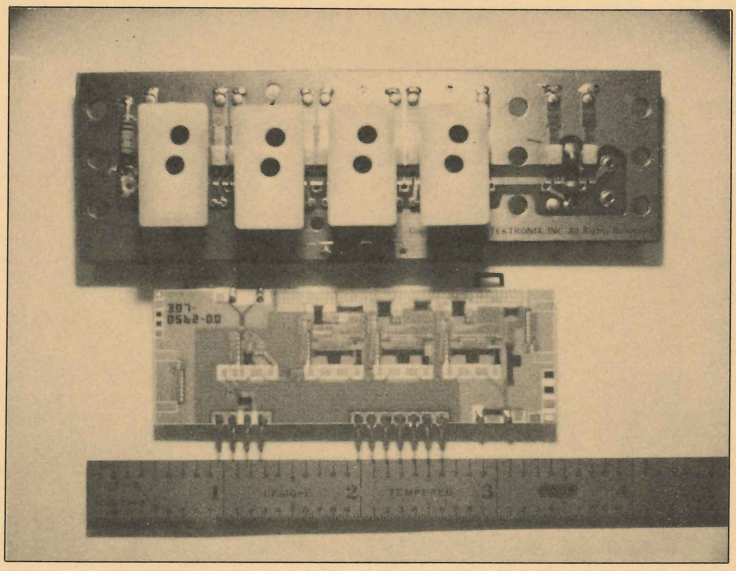


Figure 1. Compared to its predecessor - the hybrid modular attenuation system (top) - the Novar attenuation system (bottom) offers several advantages: lower manufacturing costs, lower weight, smaller size, and the fact that Novar doesn't require post-assembly calibration.

GLOSSARY

Attenuator - a voltage divider formed by resistors and paralleled capacitors.

Attenuation system - an assembly of attenuators and switches; provides a selection of attenuation values.

Blow-by - decreased attenuation at higher frequencies due to stray capacitance across an attenuator.

Hook - aberrations in attenuator step response due to frequency dependence of the capacitors' permittivity.

Lumped Parameters - description of a circuit in terms of a finite number of resistor, capacitor, or inductor elements.

Rolloff - an improperly low amplitude of the leading portion of a square wave due to improper balance of attenuator capacitors.

Novar attenuators cost less primarily because they don't require high-skilled labor for calibration.

A third advantage of Novar attenuators is that they don't have to be easily accessible (because they don't require post-assembly calibration). This removes a constraint on product package designers.

Several major technical hurdles had to be overcome to develop Novar: designing capacitors that didn't require post-assembly adjustment, developing capacitors on a stable thick film, developing a test fixture that enabled manufacturing people to precisely trim capacitors, and ensuring a stable electromagnetic environment for the attenuator.

TRIMMABLE CAPACITORS

Consider first the hurdle of designing capacitors that didn't require post-assembly adjustment.

Oscilloscope vertical input attenuation systems (typically having one megohm impedance) must provide precise voltage attenuation over a wide frequency range. As shown in figure 2, such an attenuation system consists of divider elements, each composed of a resistor and capacitor in parallel. Resistor and capacitor values must be known precisely.

Because all attenuators have some unknown stray capacitance, past attenuator designs used variable capacitors that manufacturing personnel adjusted after assembling the oscilloscope. These variable capacitors required as much as 15% of the time devoted to calibrating a product.

Variable capacitors are usually expensive, bulky, and unreliable. Further, adjusting the capacitors requires access to them. Thus, accessibility is a constraint for the product package designer.

Although Tektronix designers (using thick-film hybrid techniques) have miniaturized attenuators for wide-bandwidth applications, such designs still include some form of variable capacitor.

THICK-FILM TRIMMING

To avoid the need for variable capacitors, the High-Frequency Component Development (HFCD) group developed a unique thick-film-capacitor trimming technique.

Thick-film capacitors consist of two printed-and-fired conductive layers separated by a dielectric layer. Available laser-trimming equipment cannot trim thick-film capacitors using resistor-trim techniques

Continued on page 4

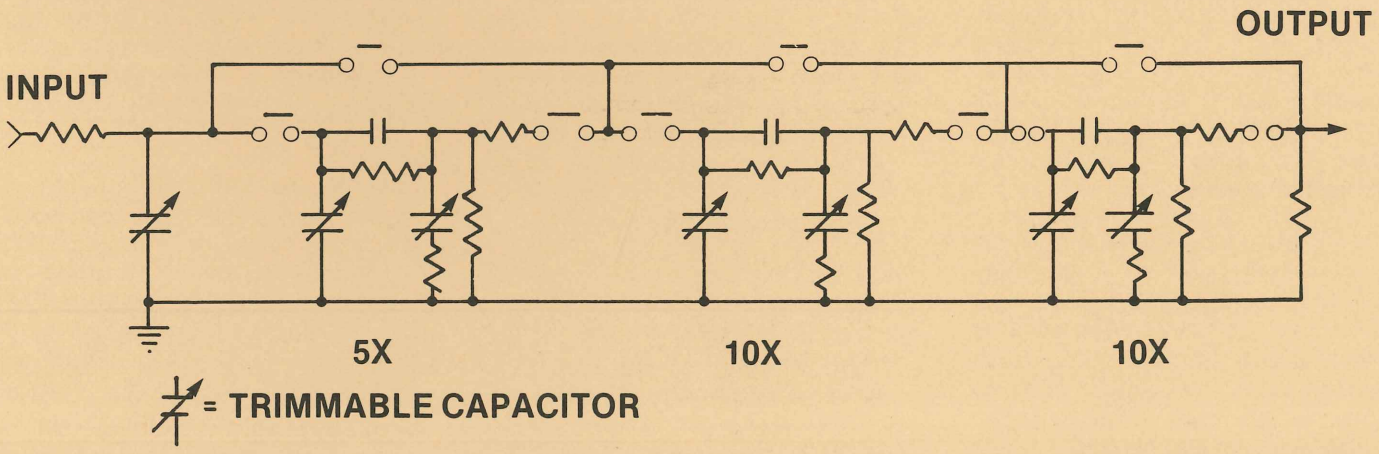


Figure 2. This SC504 80-MHz Oscilloscope attenuator is an example of an oscilloscope vertical input attenuation system.

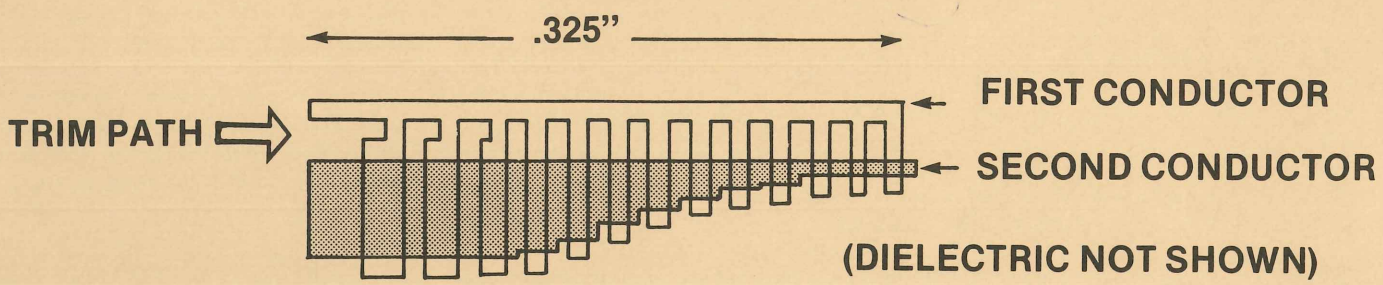


Figure 3. High-Frequency Component Development developed a technique to laser trim thick-film capacitors for the tweakless attenuation system. The beam cuts off segments from an array of capacitive segments. The value of each successive segment differs by a factor of 1.25. With such segmentation, several different combinations yield the same value.

Continued from page 3

because such techniques produce electrical shorts and unstable film in conductive areas. Instead, HFCD used a technique in which a laser beam cuts off a small segment from an array of capacitive segments. Figure 3 illustrates the technique.

One approach to capacitor array design consists of segments arranged in binary-weighted values of (for example) 16, 8, 4, 2, and 1 picofarad. This scheme has two drawbacks. First, the largest segment's capacitive value must be as accurately known as the value of the smallest section. This requires a very small tolerance for the largest section. Second, the trimming system must correctly predict the proper trim combination at the beginning of the trim process because only one combination of trimmed segments will yield a given value.

A further problem for the SC504 project was the accuracy required. For instance, a 20-picofarad capacitor had to be trimmed within 0.05 picofarad — a value smaller than the value of the smallest realizable segment.

To avoid such problems, the attenation system has a large number of segments, with each successive segment's value differing by a factor of 1.25. With such segmentation, several different combinations yield the same value. Tolerances smaller than the smallest segment's value are possible.

Because the segments are small, as much as one-third of the segment's capacitance comes from fringe fields. Therefore, each capacitor was designed with smaller dimensions than the usual capacitance-per-unit-area formula would dictate. Further, each pair of capacitor plates overlaps to eliminate altering capacitance due to normal printing misalignment.

A dynamic trimming program selects the combination of capacitor segments to be trimmed. The program starts by instructing the laser to cut a "predictor" segment, and then uses information from each trim to determine which segment will be cut next. Thus, the trim program obtains a precise end value without requiring extremely precise segment values.

THE FIXTURE

Trimming attenuators with sufficient accuracy and measuring the response of stressed attenuators required rolloff (or overshoot) measurements accurate to 0.1%. Such accuracy, in turn, required a special measurement fixture.

HFCD designed a measurement fixture (see figure 4) that differentially compares the output of the tested attenuator with the output of an attenuation standard. A voltage-step drives both attenuators. The peak value of the difference signal is directly proportional to the rolloff amplitude. The signal is positive for an overcompensated attenuator (an overshoot condition) and negative for an undercompensated (rolled-off) attenuator.

The signal then passes through an analog signal gate to a dual-polarity peak detector. The peak detector outputs a dc level directly proportional to the overshoot or rolloff of the tested attenuator.

The signal gate between the differential amplifier and the peak detector blocks the detector response to the falling edge of the input voltage step. The gate has a slight delay to allow for the difference between the dc attenuation values of the tested attenuator and the standard attenuator.

There were several problems in designing the fixture: designing a differential amplifier having high common-mode rejection for higher frequencies, and designing a high-speed analog gate with low gating transients.

For the standard attenuator, a low-impedance resistive attenuator was the best choice because a low resistance ensures that transients caused by parasitic capacitance in the standard attenuator are much shorter than the transients associated with the tested attenuator and will settle out during gate delay.

In designing the fixture, the third and most difficult problem was

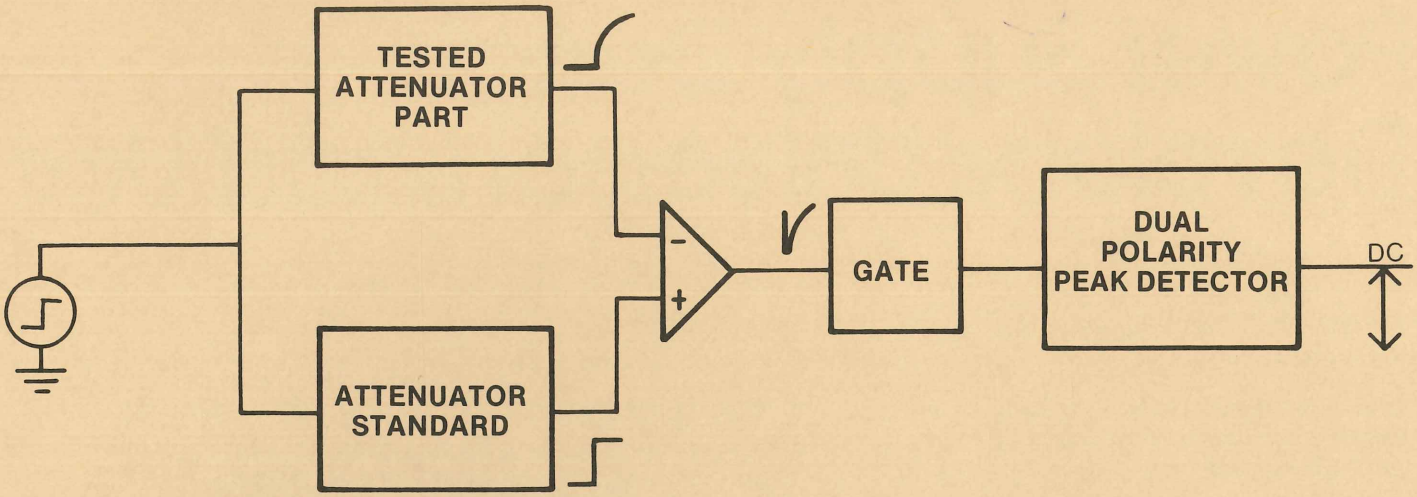


Figure 4. The trim-fixture circuit.

duplicating the instrument's capacitive environment. The fixture must duplicate the blow-by and stray capacitance produced in the instrument environment. The solution was to trim the attenuators to specified offset values to compensate for small discrepancies between the product and fixture environments.

ENVIRONMENTAL STABILITY

Matching the fixture and SC504 capacitive characteristics required close attention to placement of electromagnetic interference shields in the fixture. Signal blow-by from input to output is extremely sensitive to shield position and to the shape and spacing of the signal-leads that connect the fixture to the tested attenuator.

During attenuator measurement, the fixture simulates the instrument environment. However, during trimming, laser-head movement across the device disturbs the fixture's capacitive environment. Trimming the attenuator to an overshoot offset value compensates for the laser-head's presence.

FOR MORE INFORMATION

The Novar attenuation system offers many cost and performance advantages. For more information about Novar applications, call Des Murphy on ext. 7033.

ACKNOWLEDGEMENTS

The authors gratefully acknowledge the assistance of Kevin Clark (High-Frequency Component Development), Al D'Silva (Ceramics Engineering), Ken Hoggatt (Ceramics Engineering), Jim Keski (Ceramics Engineering), Gary Reed (High-Frequency Component Development), Ron Roden (Electronic Services), Janice Shelton (Ceramics), Dave Smithhisler (High-Frequency Component Development), and Moira Tan (High-Frequency Component Development). □

REVIEWERS NEEDED

Engineering News articles are becoming more technical and more detailed and that trend will continue. Although most articles are written and edited for a general engineering audience, only technical specialists can effectively review the content of very complex articles.

Engineering News publishes articles written by engineers and scientists in all the disciplines found at Tektronix. Examples include electrical engineering, mechanical engineering, chemistry, chemical engineering, materials research, human factors, and aspects of marketing and manufacturing of direct interest to the Tektronix engineering and scientific community.

If you are interested in reviewing a rough draft article in your specialty, call ext. 6795 or write to D.S. 19/313. □

T&M PUBLICITY RENAMED

T&M Publicity has a new name: Technical Marketing Communications (TMC). The new name reflects the group's special concerns: disseminating technical information both within and outside Tektronix; and serving the engineering and scientific communities inside Tektronix with editorial and graphics assistance.

For more more information about TMC's services, call ext. 6795 or drop by 19-313. □

Power Supply Design Develops Universal Load Unit

David Leatherwood, Power Supply Design (Technical Support), ext. 5412 (Beaverton).

Brian Mattson, Power Supply Design (Technical Support), ext. 5412 (Beaverton).

Ira Pollock, TM 500 Engineering (formerly with Power Supply Design).

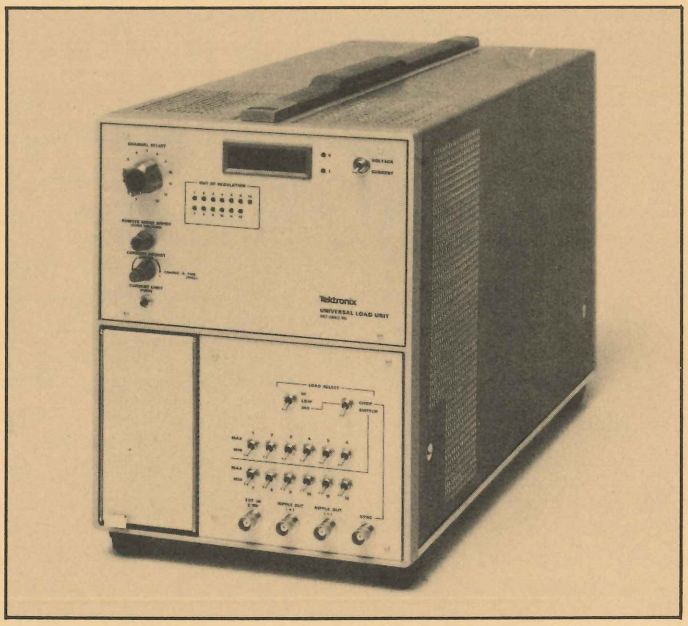
Testing switching power supplies in the field or in manufacturing often presents a major problem. For proper operation, most switching supplies need to be loaded, but appropriate loads are not always readily available. Without loads, the power supply may become unstable, lose regulation, go into overvoltage, produce excess ripple, or simply fail to start altogether.

Power Supply Design has developed a Universal Load Unit that manufacturing and field people can use to test power supplies in Tektronix products. The Universal Load Unit, designed to support the 7912AD and 7612D supplies (the most complex supplies developed to date), is truly universal within the limits of 350 volts, 25 amps, and 500 watts total input power.

To enable servicers to remove power supplies from their host instruments, many power supplies have modular construction. The Universal Load Unit takes advantage of this modularity by directly accessing each power supply output and testing its operation over its full range.

OPERATION

The unit makes single- and multiple-output power supply testing easier by measuring output



Universal Load Unit

CHANNEL	V_{MAX}	I_{MAX}	POLARITY
1, 2	50V	25A	+
3, 4	100V	10A	+
5, 6	150V	2A	+
7, 8	50V	25A	−
9, 10	100V	10A	−
11, 12	150V	2A	−
13	350V	(10 WATT MAX)	+

Channels 1 - 2 are active cells, while cell 13 is a passive (resistive cell).

Table 1. The Universal Load Unit provides 13 channels. Channels 1 - 12 are active cells; channel 13 is a passive (resistive) cell.

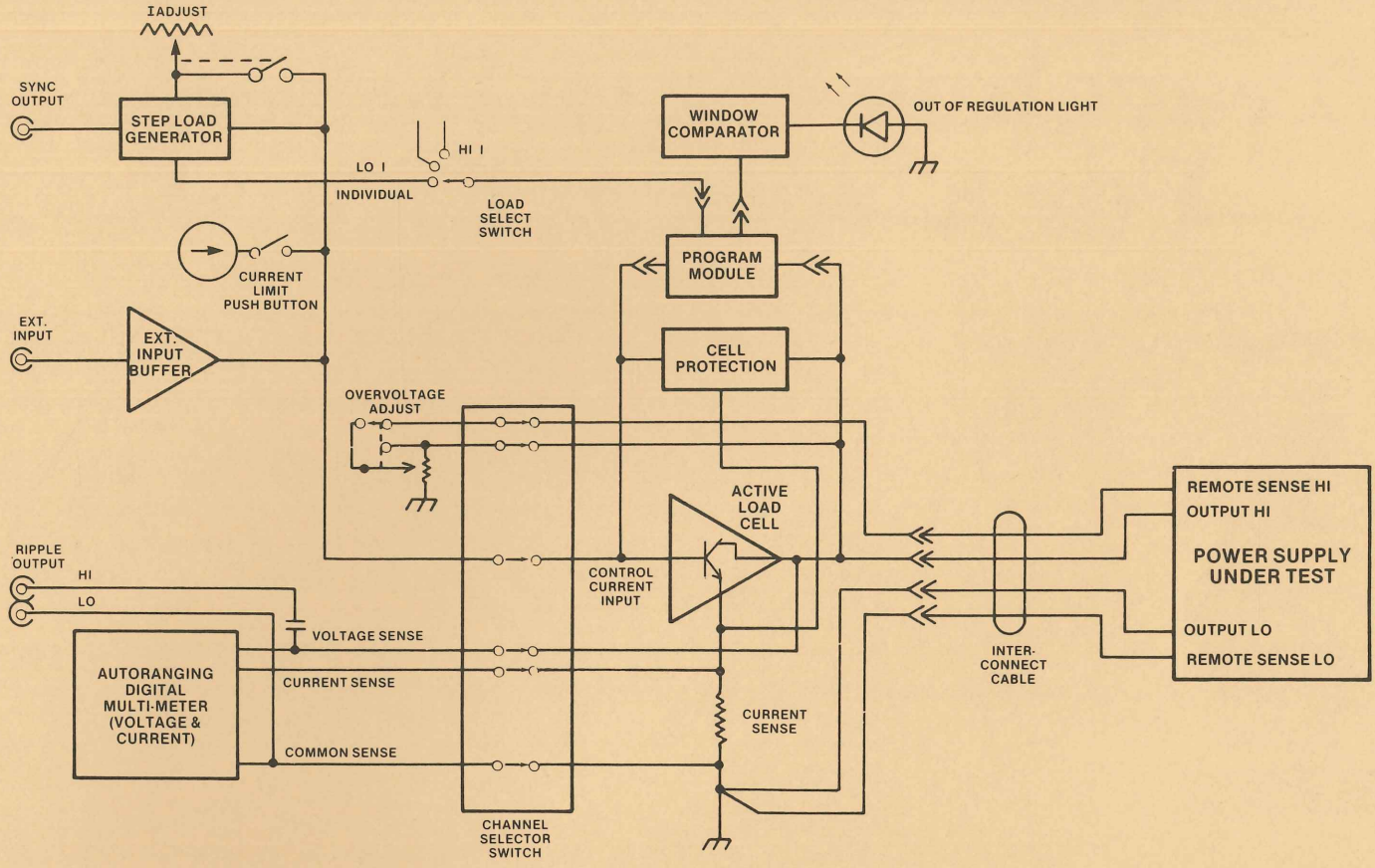


Figure 1. As shown in this Universal Load Unit block diagram, the active load cell uses transistors instead of resistors to load a power supply output. A Universal Load Unit operator can program these active load cells to simulate a variety of loads. Programming is performed with internal resistors mounted on removable program modules. Each power supply model requires a unique program module and cable set.

voltage regulation under varying loads. An operator can simultaneously load the 12 active and one passive channels. The plug-in module can program the active channels for either constant-current or constant-resistance operation.

Also, by using a front-panel switch, the operator can connect any channel to an internal four-and-a-half-digit front panel meter that measures voltage or current. For transient-response testing, the Universal Load Unit has a pulse generator that can step current in the active channels. A set of front-panel, comparator-driven lights indicates if a supply is out of regulation.

Refer to figure 1. With front-panel toggle switches, an operator can control a set of resistors mounted in a 7000 series plug-in and thereby select high or low current levels. The resistors in the plug-in also program nominal voltage and tolerance of the comparators.

As shown in table 1, there are six groups of active channels, with two channels in each group. Each channel can dissipate 100 watts, but there is a 500-watt limit for the entire unit. All channels are referenced to ground.

APPLICATIONS

For manufacturing personnel, the Universal Load Unit will save time in measuring power supply operating parameters such as output voltage, regulation, current limit, crow-bar voltage, and transient response.

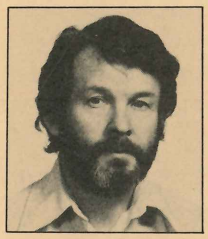
The unit makes fault isolation easier by enabling field service personnel to electrically separate a power supply problem from one in the main instrument.

AVAILABILITY

The Universal Load Unit is now in the evaluation phase and will be available to in-house users in period 003. The part number is 067-0883-00; in-house cost will be about $1000. □

PATENT RECEIVED

Traveling Wave Deflector For Electron Beams



Alvin B. Christie, Display Device Engineering, ext. 5400 (Beaverton).

Ronald E. Correll, Display Device Engineering, ext. 6857 (Beaverton).

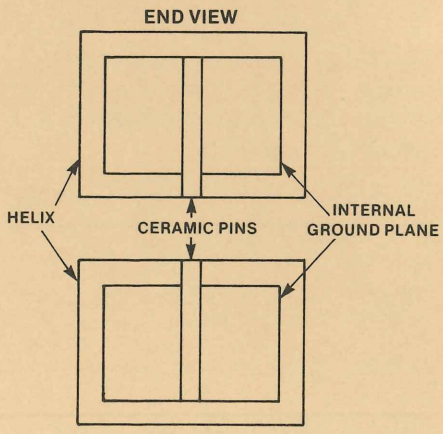
At high frequencies (100MHz and higher), solid plate crt electron-beam deflection systems have a serious disadvantage: the beam-deflecting signal can change while the electron beam passes through the deflecting field. This produces deflection on the screen that does not truly follow the input signal.

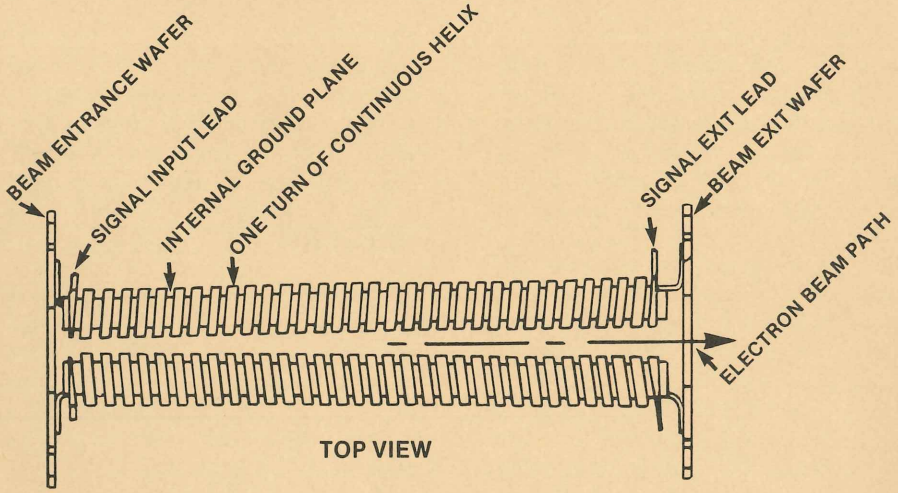
To overcome this deflection problem, we use a "traveling wave deflector" that is merely a delay line having a longitudinal phase velocity matching the electron beam velocity. To control deflection factor and aberrations in the electron beam, each element in the delay line must be precisely aligned. In addition, Manufacturing personnel must electrically tune these deflectors to match them to the driving circuitry.

The patented traveling wave structure shown here overcomes some of the problems of existing deflection systems. The deflector consists of a pair of helices each of which has flat surfaces adjacent to the electron beam axis. The surfaces adjacent to the beam are brazed to ceramic support pins that maintain a precise alignment to the beam.

The internal ground plane and helix dimensions determine deflector impedance. The dimensions are easily controlled in manufacturing. This eliminates tuning the deflector to match the driving circuitry.

The helix pitch and circumference match the input signal end-to-end propagation time to the transit time of the electron beam passing through the deflector. □





GPIB Poster

This month's issue includes a special center spread (see reverse) showing the ASCII (American Standard Code for Information Interchange) character set and its octal, hexadecimal, and decimal equivalents. Also included is IEEE 488 (GPIB) information.

The GPIB Documentation Committee (under the direction of the Digital Products Coordination Group) developed the chart from one originally produced by the Signal Processing Systems Documentation Group.

Send suggestions for improving the usability of the chart (or corrections) to George Dunn, D.S. 19-313.

(To remove the chart, pry up staples and pull out chart.)

ASCII & IEEE 488 (GPIB) CODE CHART

B7 B6 B5 / BITS / B4 B3 B2 B1	Ø Ø Ø	Ø Ø 1	Ø 1 Ø	Ø 1 1	1 Ø Ø	1 Ø 1	1 1 Ø	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER CASE	
Ø Ø Ø Ø	0 NUL 0 0	20 DLE 10 16	40 SP 20 32	60 0 30 48	100 @ 40 64	120 P 50 80	140 ` 60 96	160 p 70 112
Ø Ø Ø 1	1 GTL SOH 1 1	21 LLO DC1 11 17	41 ! 21 33	61 1 31 49	101 A 41 65	121 Q 51 81	141 a 61 97	161 q 71 113
Ø Ø 1 Ø	2 STX 2 2	22 DC2 12 18	42 " 22 34	62 2 32 50	102 B 42 66	122 R 52 82	142 b 62 98	162 r 72 114
Ø Ø 1 1	3 ETX 3 3	23 DC3 13 19	43 # 23 35	63 3 33 51	103 C 43 67	123 S 53 83	143 c 63 99	163 s 73 115
Ø 1 Ø Ø	4 SDC EOT 4 4	24 DCL DC4 14 20	44 $ 24 36	64 4 34 52	104 D 44 68	124 T 54 84	144 d 64 100	164 t 74 116
Ø 1 Ø 1	5 PPC ENQ 5 5	25 PPU NAK 15 21	45 % 25 37	65 5 35 53	105 E 45 69	125 U 55 85	145 e 65 101	165 u 75 117
Ø 1 1 Ø	6 ACK 6 6	26 SYN 16 22	46 & 26 38	66 6 36 54	106 F 46 70	126 V 56 86	146 f 66 102	166 v 76 118
Ø 1 1 1	7 BEL 7 7	27 ETB 17 23	47 ' 27 39	67 7 37 55	107 G 47 71	127 W 57 87	147 g 67 103	167 w 77 119
1 Ø Ø Ø	10 GET BS 8 8	30 SPE CAN 18 24	50 (28 40	70 8 38 56	110 H 48 72	130 X 58 88	150 h 68 104	170 x 78 120
	11 TCT	31 SPD	51	71	111	131	151	171

1 Ø 1 Ø	12 LF A 10	32 SUB 1A 26	52 * 2A 42	72 : 3A 58	112 J 4A 74	132 Z 5A 90	152 j 6A 106	172 z 7A 122
1 Ø 1 1	13 VT B 11	33 ESC 1B 27	53 + 2B 43	73 ; 3B 59	113 K 4B 75	133 [5B 91	153 k 6B 107	173 { 7B 123
1 1 Ø Ø	14 FF C 12	34 FS 1C 28	54 , 2C 44	74 < 3C 60	114 L 4C 76	134 \ 5C 92	154 l 6C 108	174 ¦ 7C 124
1 1 Ø 1	15 CR D 13	35 GS 1D 29	55 – 2D 45	75 = 3D 61	115 M 4D 77	135] 5D 93	155 m 6D 109	175 } 7D 125
1 1 1 Ø	16 SO E 14	36 RS 1E 30	56 . 2E 46	76 > 3E 62	116 N 4E 78	136 ^ 5E 94	156 n 6E 110	176 ~ 7E 126
1 1 1 1	17 SI F 15	37 US 1F 31	57 / 2F 47	77 UNL ? 3F 63	117 O 4F 79	137 UNT _ 5F 95	157 o 6F 111	177 RUBOUT (DEL) 7F 127
	ADDRESSED COMMANDS	UNIVERSAL COMMANDS	LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES OR COMMANDS	

KEY

octal 25 PPU — GPIB code

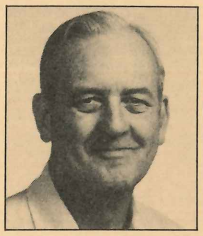
NAK — ASCII character

hex 15 21 — decimal

GRAPHIC DESIGNER: ANDREA FOWLER 1979

From ENGINEERING NEWS and SOFTWARE NEWS

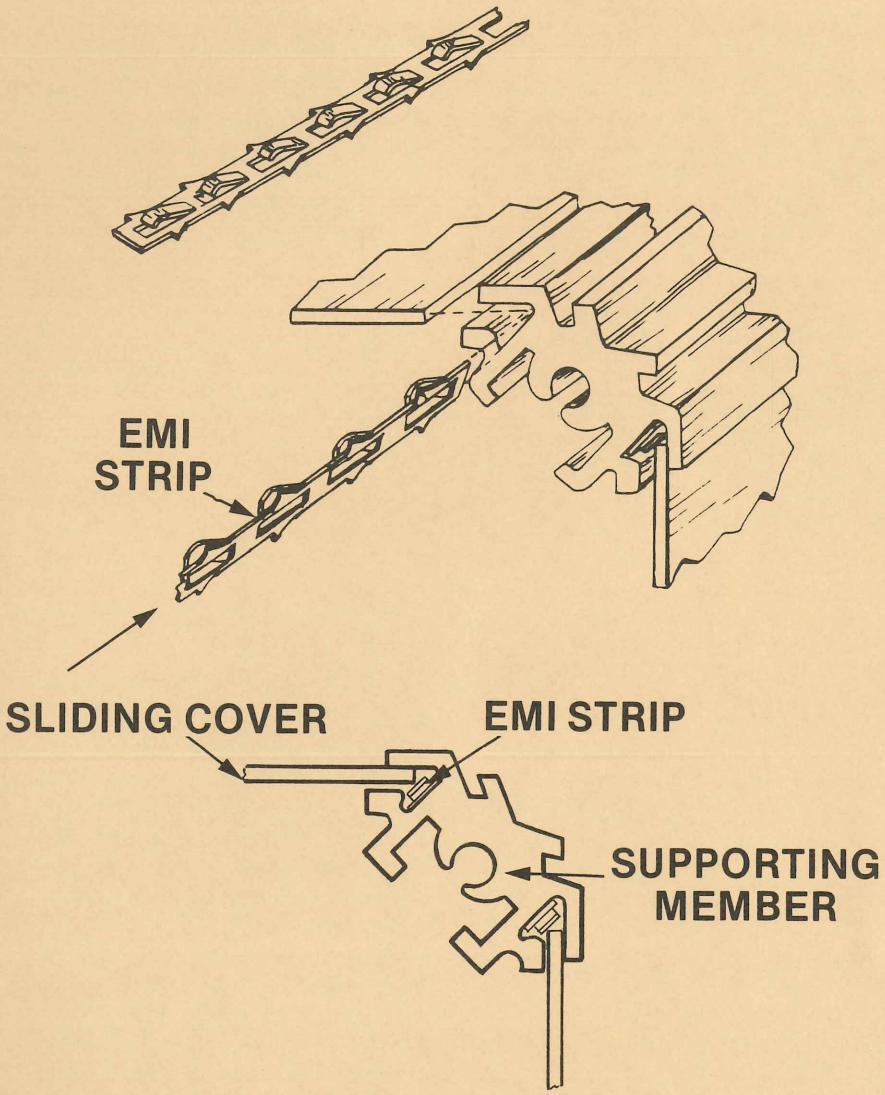
PATENT RECEIVED
EMI SHIELD DEVICE



Leon A. Prentice, Display Device Engineering, ext. 7045 (Beaverton).

This patented device is an electromagnetic interference (EMI) gasket for electronic instruments that have sliding access covers. The EMI gasket consists of a strip of metal that has two sets of spring contacts. As shown in the illustrations, the first set positions the device in a supporting-member groove, and the second set contacts the edge of the sliding cover.

EMI tests show this gasketing provides 38dB attenuation at 1GHz. □



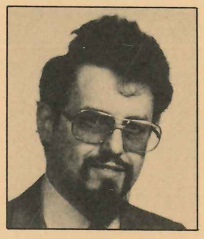
GPIB: PROBLEMS/QUESTIONS/ANSWERS???

The Digital Products Coordination Group has a consulting service for engineers who

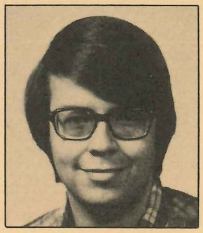
- need help with a GPIB problem,
- have trouble setting up a GPIB system,
- have a valuable GPIB idea,
- have solved a GPIB problem other engineers might be facing.

For more information, call Steve Joy on ext. 5285 or drop by 58-526. □

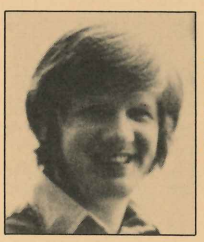
PATENT RECEIVED
Keyboard Circuit



Jack Arthur Gilmore, Graphic Computing Systems, ext. 2567 (Wilsonville).



Richard Allen Springer, Graphic Computing Systems, ext. 2535 (Wilsonville).

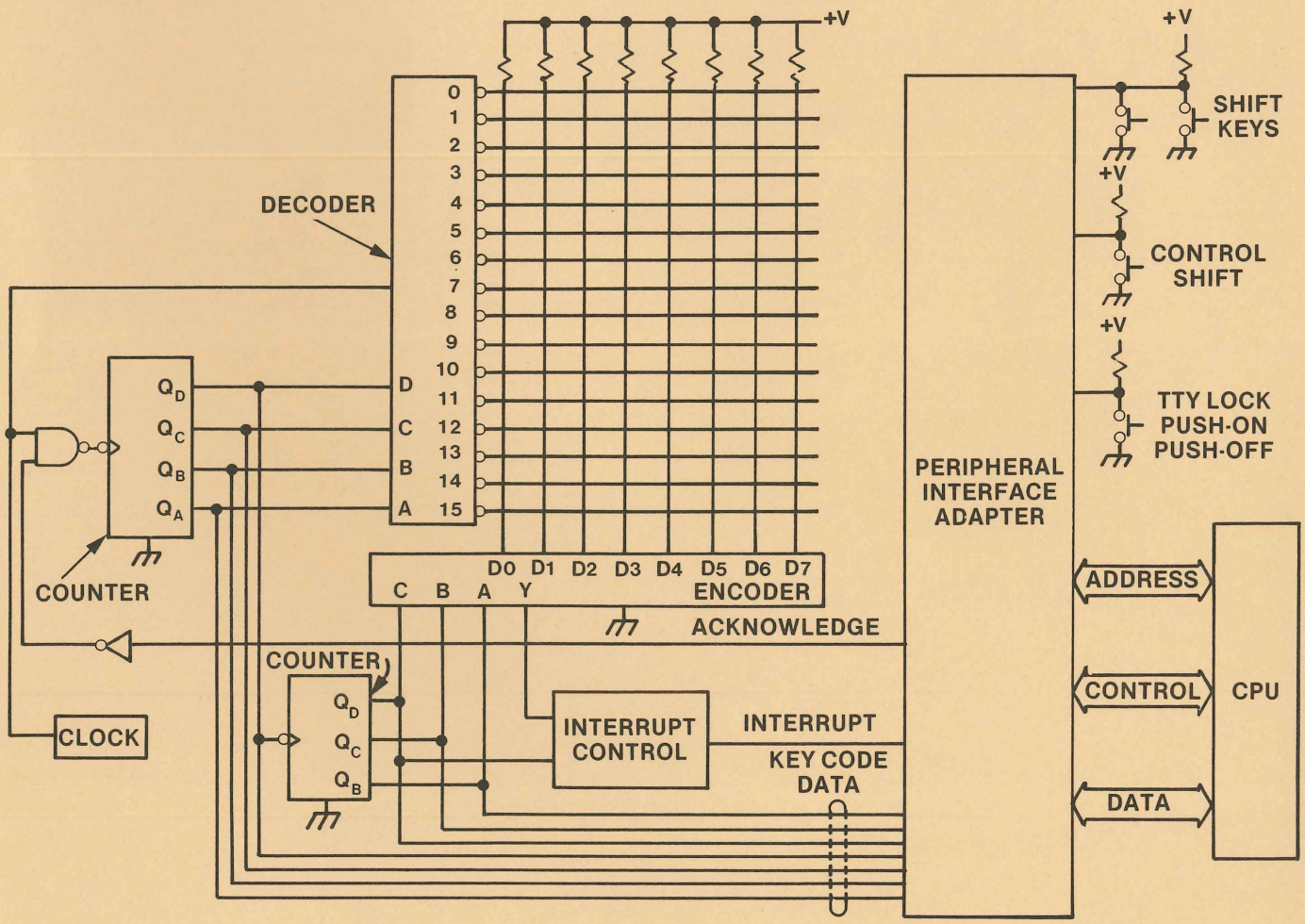


Jack Duane Grimes, Graphic Computing Systems, ext. 2558 (Wilsonville).

John Laurence Melanson, formerly with Graphic Computing Systems, has left the company.

Conventional keyboard systems have momentary-contact keys scanned by counters which stop when a key is pressed and start when a key is released. Such systems require complex circuitry for parallel data entry. Further, some systems have high error rates. For example, depressing two keys simultaneously may produce an error. Key bounce (the vibration resulting from the key making and breaking contact) and pressing three adjacent keys also may produce errors.

The keyboard circuit shown here eliminates these errors. In this simplified keyboard, the system clock sequentially scans each key and sends parallel key code data to an input port. Working with firmware, a flip-flop pair assures only valid data is sent to the microprocessor (thus providing double-entry and key-bounce protection). The firmware also provides N-key rollover (so that



each key does not have to be released to detect the next key and auto repeat (holding down any key will cause that key to be entered several times after a short pause) with a variable repeat rate. The shift, control, and TTY lock buttons provide information to the firmware to expand the keyboard functions to eight modes.

Interrupt Control ignores the first key depression. This eliminates the possibility that noise could trigger a key code. If Interrupt Control's next keyboard scan again detects the key code, then Interrupt Control interrupts the microprocessor (rewrite). The microprocessor processes the key code and immediately releases Interrupt Control to continue scanning the keyboard. □

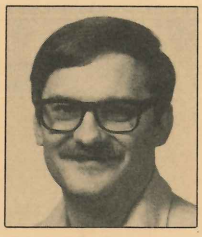
IN-HOUSE 4051 RESOURCES

The April 1979 **Software News** carried "4051 In-House Support," by Larry Gagliani (Microprocessor Applications Support, SCC).

The article details in-house resources for 4051 Computing Terminal users. Topics discussed include: Graphic Computing System's 4051 applications library, Microprocessor Applications Support's user area, and rom packs (such as COMMPACK, extended BASIC, and 4051R07, a one-dimensional array manipulator), a 4051-based eprom programmer, and facilities for duplicating rom pack firmware.

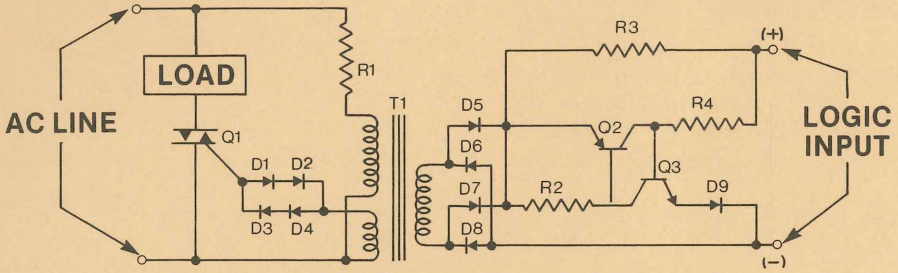
For a copy of the article, call ext. 6795 or write to d.s. 19-313 and ask for the April 1979 **Software News**. To add your name to the **Software News** mailing list, fill out the coupon on the inside back page of this issue. □

PATENT RECEIVED
ELECTRIC SWITCH



David E. Moeckli, Power Supply Design, ext. 6184 (Beaverton).

Robert E. White, Power Supply Design, ext. 5412 (Beaverton).



Alternating current flowing to and from front-panel power switches has caused interference problems for sensitive circuits in some products. As design alternatives, these front-panel power switches were replaced with other devices. These devices were a source of other problems associated with rods and relays. Rods are difficult to assemble and difficult to manufacture within mechanical tolerances, and relays (including solid-state relays) require an additional line-isolated power source.

The patented line power switch circuit shown here does not require an additional power source, thereby allowing a passive front panel switch or computer control. The circuit also features zero crossing turn-on and turn-off which reduce electromagnetic interference. The circuit is compatible with most logic device families, including TTL, DTL, RTL, CMOS, MOS and switch closure devices. Further, this circuit offers small size (about 1.5 x 2.5 x .9 inches), light weight (about an ounce), electrical isolation (Underwriters Laboratories accepted this switch in two Tektronix instruments), and isolated line trigger information.

As shown in the diagram, with line current applied, R1 provides power to T1 and limits the current. D1-D4 compensate the Q1 gate's wide voltage specification range. (If the design uses a triac with a smaller gate voltage range, D1-D4 are not necessary.) D5-D8 rectify the ac control signal from T1. Q2 and Q3 form a silicon-controlled rectifier (SCR). D9 makes the circuit compatible with various logic device families by shifting logic input level requirements.

With the logic input shorted (low), the Q2-Q3 SCR turns off at the next ac-line zero crossing. T1 then supplies power to the gate of Q1, turning it on every ac-line half-cycle. Removing the short turns on the SCR formed by Q2, Q3 through R3. This diverts T1's power from Q1's gate to the Q2-Q3 SCR. Q1 then turns off at the next zero crossing. □

THE RISKS IN DESIGNING WITH LSI

William Broderick (Microprocessor Design Lab national program manager), Los Gatos, California field office.

This is the first of a two-part article. The second part will discuss ways system designers can reduce the risks discussed here.

The rapidly increasing functional density of LSI chips has brought many benefits to electronic product designers. Examples are single-chip crt and floppy-disk controllers. Moreover, emerging linear LSI (combining both analog and digital circuitry) is greatly simplifying systems design. These advancing technologies appear to be shifting hardware/software usage trade-offs towards hardware. This article addresses pitfalls in relying too heavily on these new complex chips at the expense of software requirements.

A PRICE TO PAY

Despite the benefits of LSI technology, system designers must pay a price. For example, system designers should become aware of the assumptions that LSI chip designers make. Not recognizing those assumptions means system designers risk system failures because of erroneous or incomplete understanding of chip functions.

FAULTY SPEC SHEETS

System designers carefully examining vendor spec sheets often discover that the sheets don't specify some pin-level logic parameters. In other cases, spec sheets specify only the lower limits of a parameter and give no maximum timing value.

MEMORY CONTROL FUNCTION OF A POPULAR 8-BIT MICROPROCESSOR

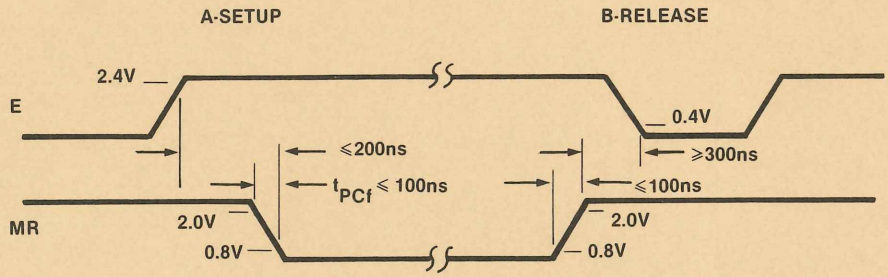


Figure 1. This waveform diagram, taken from an eight-bit microcomputer data sheet, offers an example of a data sheet error that can adversely affect a circuit design. The discontinuity symbol indicates Memory Ready (MR) can be held to a low level indefinitely. However, a later sheet says the Memory Ready signal can be held to a low level for only 10 microseconds (the internal registers of the chip are dynamic and require a refresh within 10 microseconds).

LSI DESIGN ENVIRONMENT

Fractionalized design responsibility and committee trade-offs between conflicting LSI design needs explain why vendor spec sheets don't specify some logic functions and parameter limits.

Until a few years ago, a single engineer oversaw the work of other LSI chip designers and therefore was responsible for an entire chip. This senior engineer thought through parameter limits and state logic interdependence, made trade-offs between functions, and (more importantly) examined and understood the consequences of changing internal state logic.

Teams design today's LSI chips. Each design team member has an assigned area of chip real estate, and design committees make the trade-offs between functions. The chips are now too complex for one person to completely understand, so committee members must reach compromise decisions. Faults that arise from interdependent, but specialized design areas can escape the committee's notice.

ERROR TYPES

There are several types of design faults resulting from committee design and trade-off decisions: "sneak" errors, applications oversights, misleading data sheet implications, leave-it-to-software chip designs, and just plain data sheet errors.

SNEAK ERRORS

Sneak errors arise from the fractionalized design approach required for very complex LSI. One design group may require a minimum time for a memory-ready signal but may not care what the

maximum time duration is. Defining maximum time duration for the memory-ready signal may be left to a second design group which may not actually define the time until long after the first design team has completed its work. In the meantime, a third design group may go ahead and define a maximum memory-ready time but fail to notify the other design groups. Frequent design reviews do minimize this source of errors.

APPLICATION OVERSIGHTS

The complexity and versatility of LSI chips makes it impossible for LSI designers to anticipate all applications for a given chip.

For example, LSI designers intended USART (Universal Synchronous/Asynchronous Receiver/Transmitter) chips to be used for bidirectional control of serial communications. Nevertheless, system designers can easily adapt a USART chip to control serial magnetic device data lines (in magnetic tape cassette units, for example). This is a popular, low-cost way to interface input/output logic to cassette units.

However, some USART devices have indeterminate data in internal registers (typically the synch register) after power-up. A system designer must add software that clocks-out the indeterminate data to make sure the register is cleared (RESET does not clear these registers). Unfortunately, the data sheets don't warn the user that these synch registers are not cleared at power up.

In data communications applications, clock pulses usually precede valid data to clear input registers in the receiving device before the receiving device begins reading data. However, with data transfer from serial tape cassettes, clock pulses and valid data usually coincide. If they are not coincident, there are usually other design problems. In such cases, the systems designer must find some other way to clock USART synch registers in order to clear them after RESET (that is, before they receive valid data). System designers must then write input/output programs to clear these internal USART registers by generating programmed clock leads after power-up. This is another example of adding unplanned-for software.

The power-down situation that occurs between a USART and a popular single-chip eight-bit microcomputer provides another example of LSI designer applications oversight. Adding a dedicated-controller function to a chip is the fastest growing area of microcomputer applications. Unfortunately, the LSI chip designers assumed the controller always shares a power supply with the USART.

One common application of this controller chip and USART can cause problems. If the USART interfaces to a separate power supply, and if power to the single-chip controller board is turned off, the controller's serial input/output line becomes a short to ground for the USART's 2.2 milliamp drive. Because the manufacturer did not specify that condition, many system designers have had to ask their supplier for replacement controller chips when they were debugging the interface to a USART that has a power supply separate from the single-chip controller.

IMPLIED CAPABILITIES

A third source of grief for system designers is spec sheets that imply capabilities that the chip doesn't have. For example, a floppy-disk controller chip which "supports up to four drives" (according to its spec sheet), has only enough register and status logic to keep track of two (not four) disk drives at any one time.

An older example of implied but non-existent capability is the use of the word "index" in early 8080 microprocessor literature. Minicomputers, and some other microcomputers produced at the time, did have index registers (storage devices that determine operand addresses). The 8080 "index" registers were not used in the traditional way. System designers coming from mini-computer environments were easily mislead, when they assumed "index" registers meant the same for early 8080's that it meant in other microcomputers.

LEAVE IT TO SOFTWARE

Some LSI designers have a "leave-it-to-software" attitude that can cause problems for system designers. An example is the family of floppy-disk controller chips which return a status report of either "no deleted sectors have been found during a multisector read operation" or "one or more deleted sectors have been passed over during the read operation." With such chips, the system designer must develop software that determines how many sectors have actually been transferred to RAM. The system designer must write extra software to determine the number of transferred sectors by analyzing the ending address after the DMA completes direct memory access transfer. Writing code to determine the number of transferred sectors doesn't take much system design time, but this unplanned code is another example of the price that system designers must pay for the LSI designer's "leave-it-to-software" attitude.

DATA SHEET ERRORS

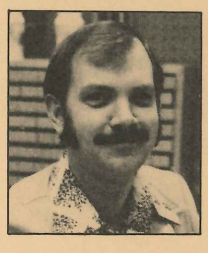
Data sheet errors have always been with us. In microprocessor-based products, these errors can be very expensive. System designers may discover these errors only when they are programming new product applications for older products. Then, the update severely impacts the installed software ROM base in the product out in the field.

The data sheet for an eight-bit microcomputer frequently used in data communications applications provides an example of this kind of error. Refer to figure 1. The discontinuity symbol $\int\!\!\int$ indicates that the Memory Ready (MR) signal can be held to a low level (Not Ready) indefinitely. A later data sheet says the Memory Ready signal can be held to a low level for only 10 microseconds (the internal registers of the chip are dynamic and require a refresh within 10 microseconds). □

PATENT RECEIVED

"SLEWED-EDGE" SCOPE SWEEP CALIBRATOR

Edward Joseph Cleary, TM500 Engineering, ext. 1775 (Walker Road).



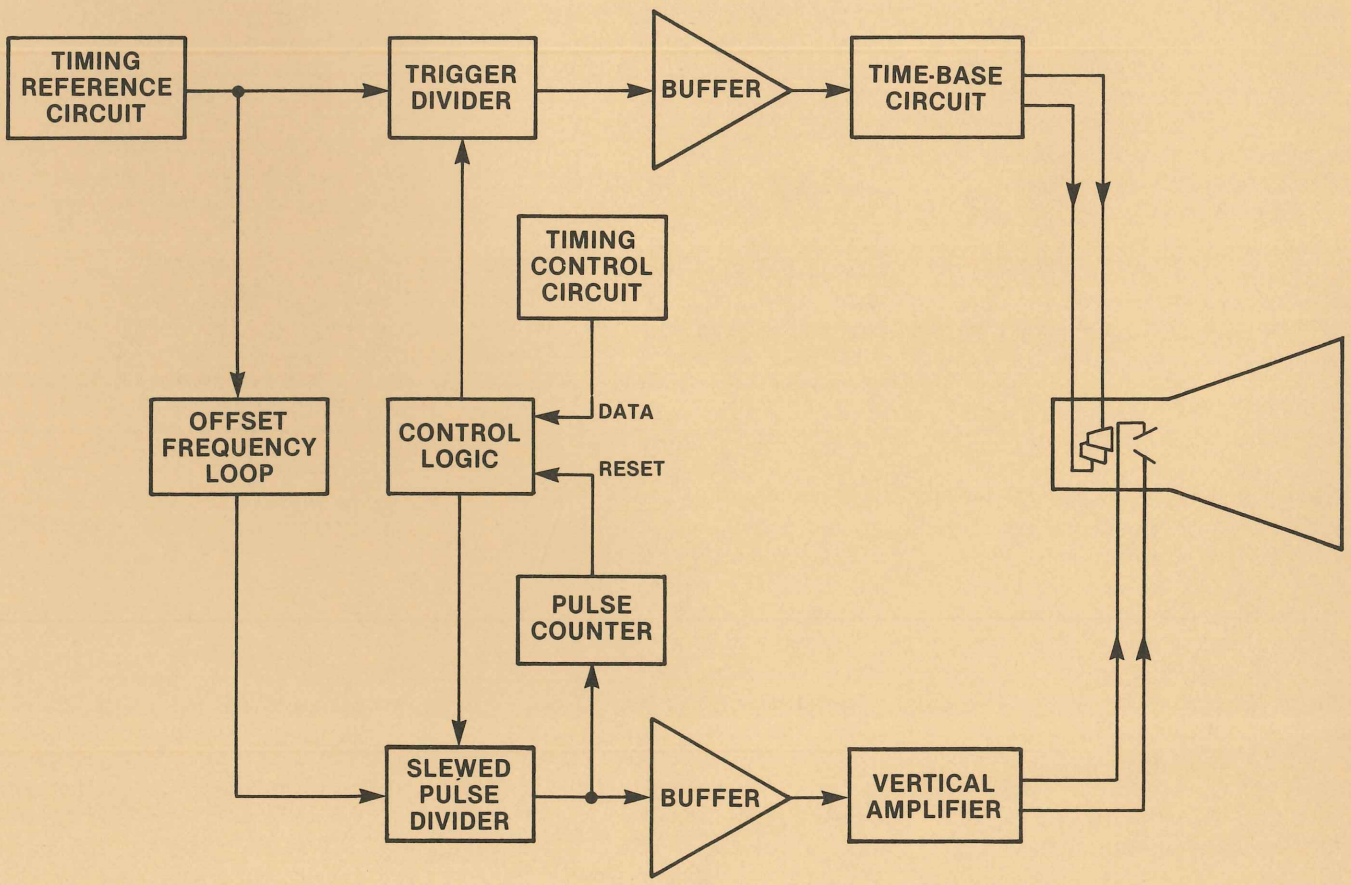
Michael G. Reiney, Logic Analyzer Engineering, ext. 1699 (Walker Road).

The traditional method of calibrating the time-base axis of a measurement instrument, such as an oscilloscope, is applying a signal with known frequency characteristics to the scope's vertical axis. Typically, a separate device generates this signal which may be precise markers, square waves or sine waves. To provide a reasonably accurate sweep rate, the operator performing the calibration adjusts time-base circuits for timing and linearity.

Calibration of present-day time bases (in oscilloscopes having 100 to 200 megahertz bandwidths and 1 to 0.5 nanosecond per division time-base sweep rates) is difficult because vertical amplifier channels can not pass 1 to 2 gigahertz calibration signals.

The patented circuit shown here repetitiously slews the leading edges of incrementally-delayed successive pulses across a screen.

This novel sweep calibration method doesn't require displaying signals such as sine waves that have frequencies far higher than the oscilloscope can handle. □



Technical Standards Announces New Publications

Technical Standards has announced six new standards publications.

Metric Laws and Practices in International Trade defines metric import requirements for many countries. To borrow a copy or for more information, call ext. 7976.

U.S. Standards Activities is a research paper that Vaughn Weidel (Product Safety) wrote. The paper describes American National Standards Institute and Underwriters Laboratories activities, and proposed federal control of voluntary standards associations. For a copy, call Vaughn Weidel on ext. 7357.

Product Safety and Loss Prevention, a booklet published by the National Safety Council, describes common sources of product liability, a product safety and product loss-prevention program, key elements of the Consumer Product Safety Act, and identification data required by CPSA. For more information, call ext. 7976.

Symbols and Practices for Schematic Diagram Drafting (Drafting Standard 062-2476-00) identifies reference designations and graphic symbols that should be used to document electrical and electronic parts and equipment. This standard is based on the work of an ad hoc committee that included representatives from each Test and Measurement manuals group. The standard includes the most frequently-used American National Standards Institute Y32.2-1975 symbols as well as symbols used by Tektronix but not included in the ANSI standard. For a copy, call Reprographics on ext. 5577.

Finish Standard (part number 062-2868-00) describes standards for etch, chromate and lacquer used on aluminum. This standard replaces F-209. For a copy, call Reprographics on ext. 5577.

Components Standard (part number 062-3751-00) describes reel packaging of axial lead components for automatic insertion. For a copy, call Reprographics on ext. 5577.

FOR MORE INFORMATION

For more information about standards, call Carol Whitmore (Technical Standards) on ext. 7976. ☐

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Hobby Fair III Announced For July

The Engineering Activities Council has announced that it will sponsor Hobby Fair III in July, 1979. Hobby Fairs are exhibits of engineering and G-job projects. Hobby Fair I (1977) and Hobby Fair II (1978) included only microprocessor projects, but Hobby Fair III is open to engineering projects in all disciplines.

Because exhibit space is limited, the Engineering Activities Council will select participants from among applicants.

If you would like to exhibit a project at Hobby Fair III, fill out the coupon below and mail it to Elske Cordell, 50-389. Applications must be in by June 1, 1979.

Technical Marketing Communications has published reports describing Hobby Fair I and II. For copies, call ext. 6795 and ask for Forum Report 6 and Forum Report 11. □

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Ext. _____, D.S. _____

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If you have questions about displaying your project, call Elske Cordell, ext. 6098 (Beaverton).

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Why EN?

Engineering News serves two purposes. Long-range, it promotes the flow of technical information among the diverse segments of the Tektronix engineering and scientific community. Short-range, it publicizes current events (new services available and notice of achievements by members of the technical community).

Contributing to EN

Do you have an article or paper to contribute or an announcement to make? Contact the editor on ext. 6795 or write to 19-313.

How long does it take to see an article appear in print? That is a function of many things (the completeness of the input, the review cycle and the timeliness of the content). But the *minimum* is six weeks for simple announcements and about ten weeks for major articles.

The most important step for the contributor is to put the message on paper so that the editor will have something with which to work. Don't worry about organization, spelling and grammar. The editor will take care of those when he puts the article into shape for you.

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