7854 Diagnostic Troubleshooting
Using 067-0911-00 & Up Diagnostic Test Interface

Service Manual

Tektronix
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WARNING

THIS MANUAL CONTAINS SERVICING INSTRUCTIONS FOR USE BY QUALIFIED SERVICE PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING UNLESS YOU ARE QUALIFIED TO DO SO.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

7854
DIAGNOSTIC TROUBLESHOOTING USING 067-0911-00 & UP DIAGNOSTIC TEST INTERFACE SERVICE

For Qualified Service Personnel Only

INSTRUCTION MANUAL

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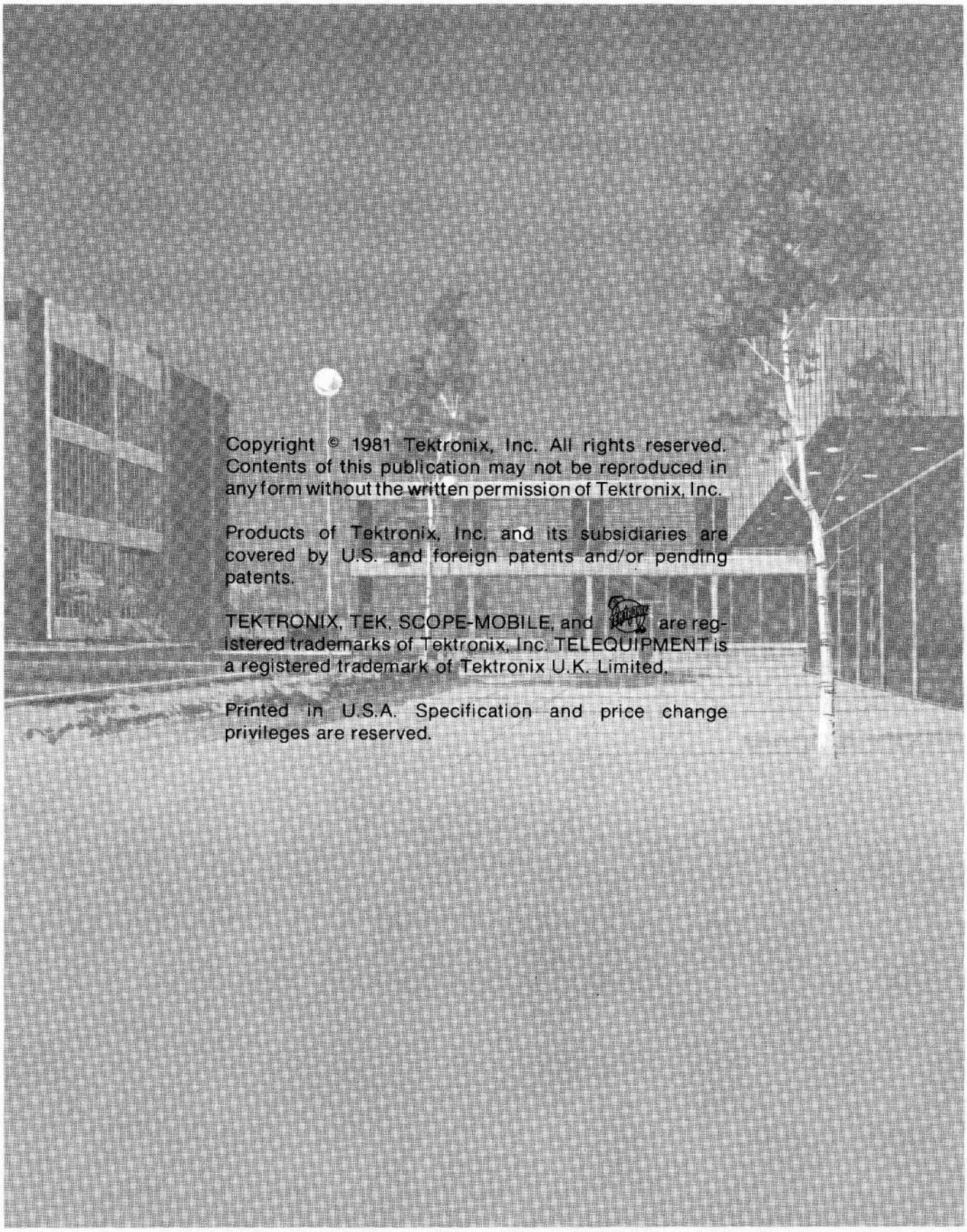

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LIST OF ILLUSTRATIONS

The illustrations in section 10 are located near their associated diagrams on the foldout page.

LIST OF TABLES

SAFETY SUMMARY

The general safety information contained in this summary is for servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL


Static-Sensitive Devices.


This symbol indicates where applicable cautionary or other information is to be found.

AS MARKED ON EQUIPMENT.


DANGER—High voltage.


Protective ground (earth) terminal.


ATTENTION—refer to manual.

WARNINGS

POWER SOURCE

This product is intended to operate in a mainframe connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the mainframe power cord is essential for safe operation.

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the mainframe power cord. To avoid electrical shock, plug the mainframe power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the mainframe power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs anad controls that may appear to be insulating), can render an electric shock.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gasses unless it has been specifically certified for such operation.

067-0911-XX DIAGNOSTIC TEST INTERFACE

The TEKTRONIX 067-0911-XX Diagnostic Test Interface facilitates testing and troubleshooting of the "smart" portion of the 7854 Oscilloscope. By providing the interface link necessary to enable the operator to control or exercise specific portions of circuitry from a terminal or Microlab I Keyboard, the 067-0911-XX permits thorough and specific testing of the 7854. The above illustration shows the 067-0911-XX Diagnostic Test Interface in a typical configuration for testing the 7854 Oscilloscope.

GENERAL INFORMATION

This section contains a basic description of the Diagnostic Manual package for troubleshooting the 7854 Oscilloscope. It includes basic information about the philosophy of diagnostic troubleshooting, general information about signature analysis and related test equipment and how to effectively use this and related manuals.

PURPOSE OF THIS MANUAL

This manual is meant to provide the information necessary for the user of the Diagnostic Test system to efficiently test and troubleshoot the digital portion of the 7854 Oscilloscope. The manual contains information about how the components of the test system fit into the 7854 architecture to facilitate testing, descriptions of the test system commands and the use of each, as well as specific test procedures for troubleshooting the 7854 and the test system itself.

PURPOSE OF THE DIAGNOSTICS-WHAT THEY WILL AND WILL NOT DO

The diagnostic procedures described in this manual are meant to isolate and correct problems primarily in the digital section of the 7854 oscilloscope. To determine if a digital problem exists, the instructions for using the 067-0912-00 Analog Test Card given in the Maintenance section of the 7854 Service Manual should be followed. If it is determined that a malfunction in the digital portion of the 7854 is present, performing the following diagnostic procedures will isolate the malfunction to a small block of circuitry or, in many instances, to the device at fault.

The following troubleshooting procedures should only be performed by qualified service personnel with an understanding of microprocessor-based system architecture and conventional digital troubleshooting techniques. The system overview description given in Section 6, Theory of Operation, of this manual and Section 3, Operator Interface With The Diagnostic System should be thoroughly understood before attempting to perform any of the following diagnostic procedures.

In general, the operating firmware (firmware that controls how the system operates at any time) incorporated in the 7854 Diagnostic Test system tests many functions of the 7854 Oscilloscope with little or no user interaction. Other procedures require more extensive user-system interaction and may require the use of other test equipment as well. The Debug Commands, are available for isolating problems in areas not thoroughly exercised by the other diagnostic routines. The Debug Commands provide ways to look at particular blocks of memory and excercise specific devices. A much more thorough understanding of the 7854 architecture is required to use the Debug Commands and will probably not be required for normal service of the instrument. The Diagnostic System also generates various "canned waveforms" and special operating modes useful for the calibration of the 7854 Oscilloscope.

DO YOU HAVE THE CORRECT LEVEL OF DIAGNOSTIC TEST EQUIPMENT AND DOCUMENTATION FOR YOUR INSTRUMENT?

Although the function of the 7854 Oscilloscope as a whole will not change, it is expected that certain modifications to improve performance and reliability will occur. These changes to individual boards in the digital portion of the 7854 may result in signatures and 067-0961-XX diagnostic firmware requirements that vary from instrument to instrument, depending on date of manufacture.

In light of this possibility, each instrument has a Service Identification Tag attached to its rear panel as shown in Figure 1-1. The tag identifies the versions of the Diagnostic Firmware and Signature Tables required to perform the diagnostics on the instrument. This version number is more fully described in the Signature Table Version Locator matrix at the front of the Signature Table manual.

HOW TO USE THIS MANUAL PACKAGE

The information necessary for troubleshooting the digital portion of the 7854 Oscilloscope consists of several individually part numbered documents.

This document, "7854 Diagnostic Troubleshooting Using 067-0911-XX Diagnostic Test Interface" is the principal manual and is bound in a 3-ring binder to enable insertion of the other support documents at their appropriate locations. Each insertion point is indicated by a full page tab with explanatory information on each.

The supplementary manual "7854 Signature Analysis Tables Using 067-0911-XX Diagnostic Test Interface" (Part number 070-2922-XX), should be inserted behind the "Signature Tables" tab. It is a history document and will contain all information published in all earlier Signature Table documents. The first version of this document you obtain should merely be inserted at the

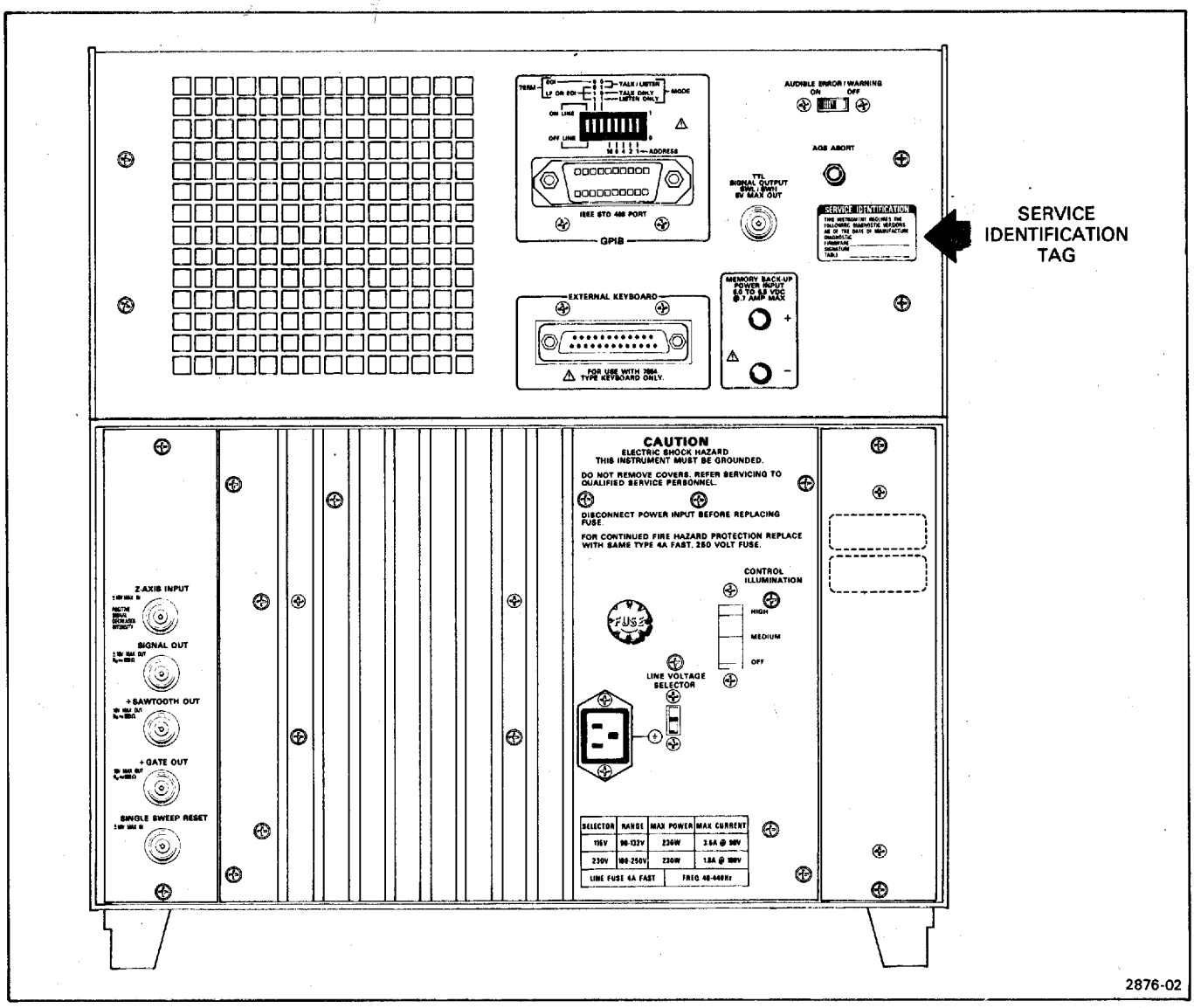

Figure 1-1. Service Identification Tag.

indicated point in this manual. If, at a later date, updated Signature Tables are obtained, the earlier version of said document should be discarded and the new one inserted in its place. This policy will minimize the possibility of error and will ensure that your diagnostic manual package is in its most current and most usable form. Manuals and Data sheets for diagnostic related hardware should be inserted behind the Supplementary Documents tab.

The "Test Procedures for 7854 Diagnostic Troubleshooting Using 067-0911-XX Diagnostic Test Interface" (Part numbers 070-2875-00 and 070-3887-00) contains the flowchart test procedures for troubleshooting the 7854 Oscilloscope in two volumes and should be used with the Signature Tables mentioned above.

After all documents have been properly inserted and the Test Procedures Manuals have been obtained, the diagnostic package is complete and ready to use. The purpose of each section of the diagnostic manual package and its use with other related sections follows:

Section 1, General Information, contains introductory information to familiarize the diagnostic user with philosophy of intent of the diagnostic hardware, firmware and its supporting documentation. It explains the use of the diagnostic package and gives a general description of Signature Analysis for those that may be unfamiliar with this troubleshooting technique.

Section 2, 7854 Diagnostic Troubleshooting Procedures, contains the bulk of the setup and test

equipment information used in troubleshooting the digital portion of the 7854 Oscilloscope. A list of diagnostic test equipment is given along with its installation and setup procedures.

Section 3, Operator Interface With the Diagnostic System, gives general information concerning input to/output from the diagnostic system. It covers general command entry from the RS-232 compatible terminal and MicroLab I and the ways system information is presented to the user from each.

Section 4, Command Dictionary, contains comprehensive information about the invocation and use of each of the Diagnostic and Debug/Utility commands. The intent of each command and a detailed description of its execution is given in this section. The test procedures given in section 2 implement specific capabilities of each of the Diagnostic commands to perform a general troubleshooting procedure. Understanding the intent of each of these Diagnostic commands as well as command execution is necessary to efficiently troubleshoot the 7854 Oscilloscope.

The Debug/Utility commands are of a more general form and not implemented in the test procedures of section 2. These commands however become extremely useful in isolating faults when the test procedures of section 2 indicate a fault in a general block of circuitry or memory. The Command Dictionary explains how these may be used.

Section 5, 067-0911-XX Specification contains the information defining the electrical and mechanical characteristics of the 067-0911-00 Diagnostic Test Interface (consists of 3 boards).

Section 6, 067-0911-XX Theory of Operation, is intended to show how the hardware and firmware of the 067-0911-00 Diagnostic Test Interface operates as part of the larger diagnostic system. This section contains detailed circuit descriptions of 067-0911-00 hardware and more general architectural information relating the 067-0911-00 to the 7854 Oscilloscope (device under test) and the other required test equipment (MicroLab I and 067-0961-00 Diagnostic Memory Board).

Section 7, The 067-0911-XX Self Test, describes the diagnostic command relating to testing the hardware and firmware of the 067-0911-00. This test description is similiar to those given in Section 4, Command Dictionary, but relates only to the testing of the 067-0911-00 Diagnostic Test Interface.

Section 8, 067-0911-XX Maintenance, provides the information necessary to properly maintain the 067-0911-00 Diagnostic Test Interface.

Section 9, 067-0911-XX Replaceable Electrical Parts , contains part numbering information necessary to ensure proper replacement of a defective electrical component.

Section 10, 067-0911-XX Diagrams and Circuit Board Illustrations, contains the schematics and board-layout dollys required for troubleshooting and maintaining the 067-0911-00 Diagnostic Test Interface. These schematics and dollys should be used in conjunction with the Self Test flowchart in section 2 (behind Test Procedures tab) and with the 067-0911-00 Theory of Operation in Section 6.

Section 11, 067-0911-XX Replaceable Mechanical Parts List, contains the part numbers required to ensure proper replacement of a defective mechanical part on the 067-0911-00 Diagnostic Test Interface (3 boards).

The Signature Tables tab marks the point where Signature Tables should be inserted. Signature Tables are individually tabbed according to version. These version numbers correspond to the Signature Table Version numbers marked on the Service Identification tag of various 7854 Oscilloscopes (depending on date of manufacture). *The Signature Table version should be determined from the Service Identification tag on the rear panel of the 7854 under test. The Signature Table Version Locator at the beginning of the Signature Tables manual should be referenced each time an instrument is serviced to ensure use of the proper level of Diagnostic Firmware (067-0961-XX) and the proper version of supporting Test Procedures, and Signature Tables.*

The Supplementary Documents tab marks the point of insertion of the manuals and data sheets for the other diagnostic hardware either required or helpful when troubleshooting the 7854 Oscilloscope. These include: 067-0961-0X Diagnostic Memory Board, 067-0912-00 Analog Test Board (optional) and the 067-0913-00, 067-0914-00 and 067-0915-00 Extender Boards (all optional).

The Test Procedures Manuals (two volumes contain the flowcharted test procedures for troubleshooting the 7854 Oscilloscope. In many instances, flowcharts require more than one page for a given test. In such instances, Figure 1-2 illustrates how the flowcharts may be used in a continuous fashion, keeping pertinent information readily accessible. Comments to clarify the intent of specific steps on each flowchart fall just to the right of that step.

RELATED DOCUMENTS

In addition to this manual, other documents, which may provide information helpful to the diagnosis of faults in the 7854 Oscilloscope are the 7854 Service, 7854 Operators, Microlab I and the Sony/Tek 308 Operators manuals. Manuals and data sheets for the 067-0912-00 Analog Test Card, 067-0961-XX Diagnostic Memory Board and the 067-0913-00, 067-0914-00 and 067-0915-00 Extender Boards (which should be inserted behind the Supplementary Docuements tab in this manual when received) may also contain information useful when performing the diagnostic procedures given in this manual.

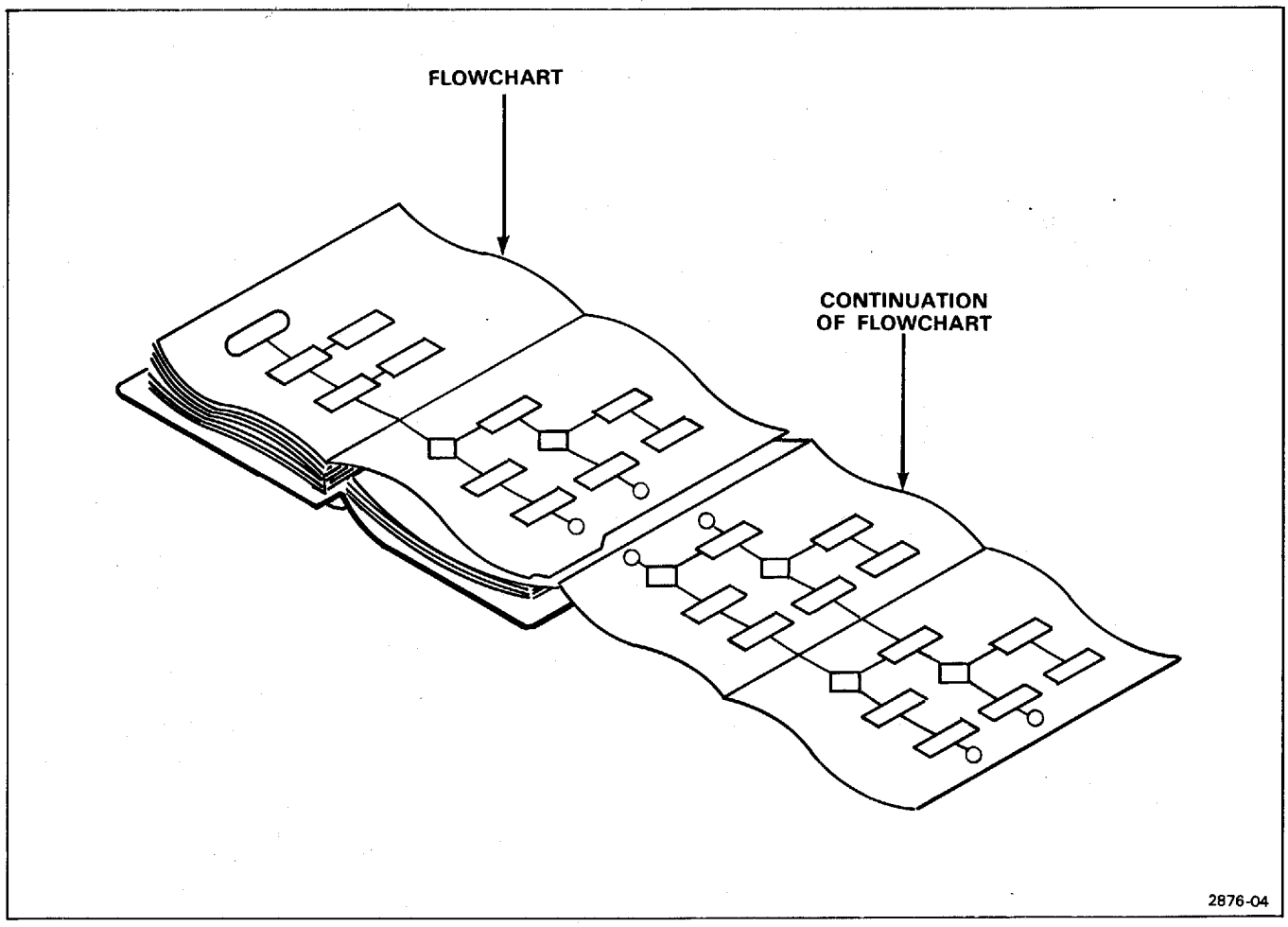

Figure 1-2. Using the Pullout Flowcharts.

SIGNATURE ANALYSIS BACKGROUND INFORMATION

Signature analysis is a troubleshooting method for isolating faults, usually to component level, in complex logic circuits. Signature analysis testing relys on stimulating circuit nodes in a repeatable and predictable fashion. The manner in which the circuit nodes are excercised is relatively unimportant, as long as the events at the node under test are repeatable. For example, a microprocessor system can easily be made to repeatedly increment through its address field, excercising a good portion of the instruments circuitry. Or, in most cases, excercise routines stored in ROM can be almost as easily retrieved and run to exercise circuitry.

Once a means of exercising the board as been implemented, actual signatures at circuit nodes may be taken. Individual signatures are taken over a specific number of system clock cycles (gate time), determined by how the signature analyzer is electrically connected into the system. The actual signature is presented to the user as a 4-digit "hexadecimal-like" number and is a numerical representation of the generally complex sequence of events occurring at the node under test. Individual signatures may be composed of the characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, C, F, H, P and U.

The signatures taken at various nodes are compared to "signature tables" containing known good signatures for the test nodes. (All signatures for these diagnostic procedures were taken with a Sony/TEK 308 Data Analyzer. Use of other signature analyzers may result in meaningless signatures.) An incorrect signature indicates a problem. Bad signatures can be traced back (in terms of data flow) to the point of error in much the same way a bad waveform can be traced back to its source in analog circuitry.

An important difference in analog signal tracing and digital signature tracing should be noted. In analog signal tracing, many clues to a fault may be picked up by watching for deviations from the desired waveshape

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(clipping, oscillations, power supply noise, etc.). In signature tracing however, subtle differences in signatures from those desired mean nothing. A wrong signature is wrong and that's generally all that can be determined from it.

There are several cases where certain wrong signatures may provide clues, however. A signature of 0000 may be an indication that a test node is shorted to ground (0000 is the "ground" signature). Likewise, a node with a faulty signature the same as the V_{cc} signature may be shorted to the positive supply. When two or more nodes have the same bad signature, they may also be shorted together.

Signature analysis may be used in configurations other than that described above, but are not implemented in the diagnostics for the 7854 Oscilloscope. Many technical articles are available on the subject of Signature Analysis and should be referred to if more specific information is desired.

7854 DIAGNOSTIC TROUBLESHOOTING PROCEDURES

This section contains the installation instructions for setting up the diagnostic test equipment for troubleshooting the 7854 Oscilloscope. An understanding of how to interface with the diagnostic system and the syntax and function of specific commands is required for efficient troubleshooting of the 7854. Information on these topics is provided in Section 3, Operator Interface With The Diagnostic System and Section 4, Command Dictionary and should be read before attempting the procedures given in this section.

GETTING STARTED

Several versions of test procedures may exist for any given board within the digital section of the 7854. If this condition exists, it is imparative that the proper procedure, signature tables and diagnostic firmware (067-0961-XX) be used. The SERVICE IDENTIFICATION tag on the rear of the instrument indicates which version of Diagnostic Firmware and Signature Tables should be used for your instrument. The Signature Table Version Locator matrix at the beginning of the Signature Tables is a master reference to ensure that the proper combination of diagnostic procedures, firmware and signature tables is used. This matrix should be referenced each time an instrument is serviced to assure that only the proper procedures are attempted.

All signature table versions are individually tabbed. Any later versions of a given test procedure flowchart fall immediately behind the original. Tabs and notes on the individual flowcharts must be observed carefully to ensure use of the proper procedure.

In these procedures, any time a component is removed, reinstalled or replaced it is assumed that power has been turned off prior to and reapplied after that step is performed.

If, by performing the procedures, it is determined that a component is defective, the procedures given in the Maintenance section of the 7854 Service Manual should be followed to replace the part. Due to the complexity of the boards used in this instrument, these procedures should be strictly adhered to.

A portion of the firmware contained in the 067-0961-XX Diagnostic Memory Board generates waveforms suitable for calibration of the 7854 Oscilloscope. This portion of the diagnostic package may be used with no other test equipment required. For information on using the 067-0961-00 Diagnostic Memory Board for calibration purposes only, see "Using the Calibration Firmware" later in this section.

INSTALLATION

A list of the equipment required to perform the diagnostic test procedures contained in this section is given in Table 2-1. Figure 2-1 illustrates the general test equipment setup. Connect the equipment as follows:

1. Connect the display terminal to the MicroLab I using the RS232 connector on the side of the MicroLab I. (Refer to connector diagram on underside of MicroLab I for connector identification.)

2. Open MicroLab I front dust cover.

3. Insert the 067-0911-XX Interface Board (A3), component side down, into the lower track of the MicroLab I.

4. Close the MicroLab I dust cover.

5. Connect the 2 cables from the 067-0911-XX Cable Terminal Assembly (A1) to connectors J2 and J3 on the 067-0911-XX Interface Board. (The blue stripes on the cables should go to the left. The cables are marked with 'Connect to J2' and 'Connect to J3'.)

INITIAL CONTROL SETTINGS

The only control setting required to initially set is the MicroLab 1 baud rate jumpers to match the baud rate of the terminal in use (or vice-versa). The jumpers are located at the left-front corner of the MicroLab I Main Interconnect Board just behind the dust cover. Refer to the MicroLab I manual for further information

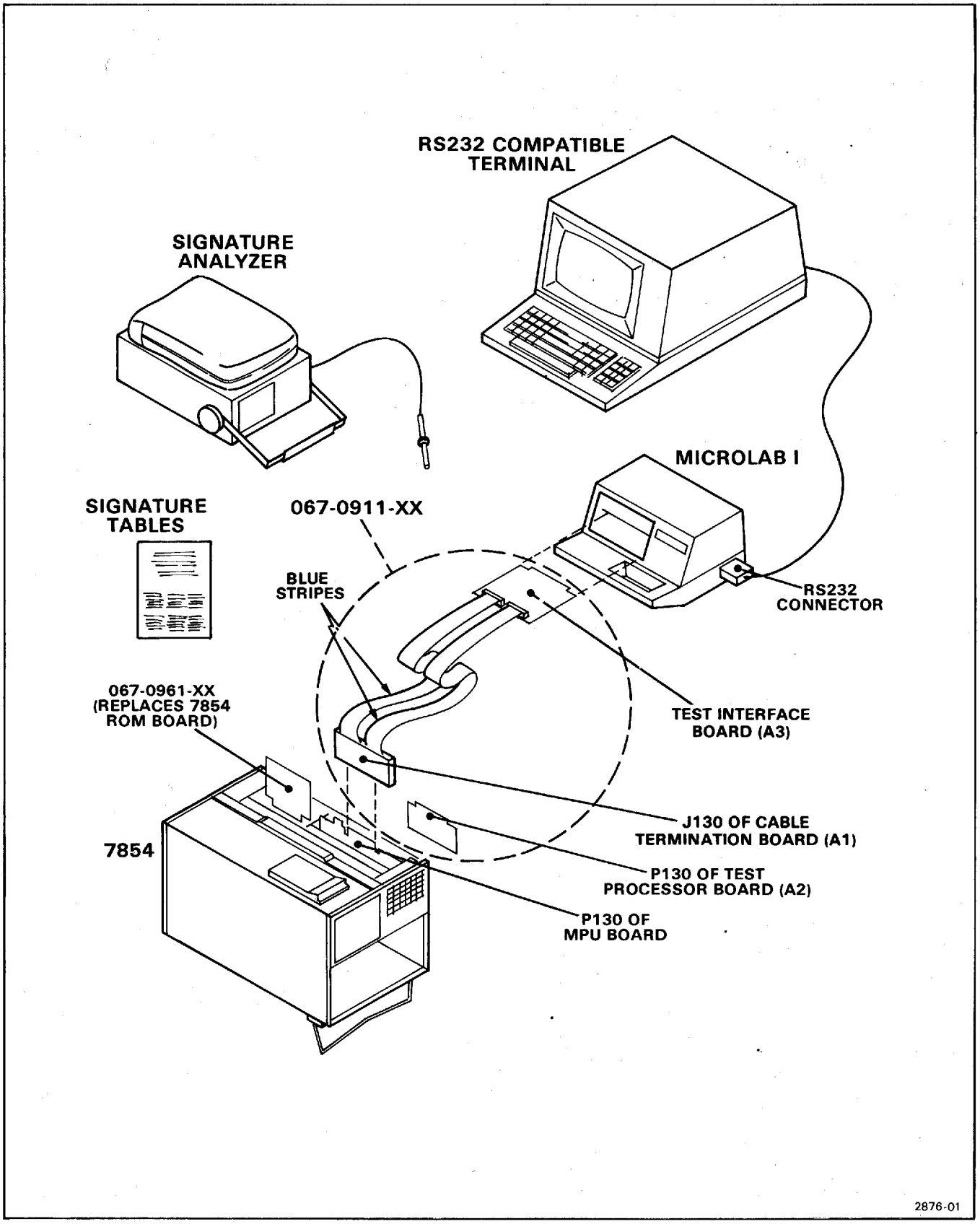

Figure 2-1. Diagnostic Test Configuration

TABLE 2-1
Diagnostic Test Equipment

Description	Purpose	Examples of Applicable Test Equipment
067-0911-00 Diagnostic Test Interface*	To provide interface between the 7854 Oscilloscope and the MicroLab I mainframe. Provides certain firmware routines and test facilities.	TEKTRONIX 067-0911-00 Diagnostic Test Interface.
067-0961-XX Diagnostic Memory Board	To provide firmware diagnostic routines for complete testing of the digital section of the 7854 Oscilloscpe.	TEKTRONIX 067-0961-XX Diagnostic Memory Board (must be matched to instrument under test; see the Service Identification tag on the back of the 7854 Oscilloscope).
067-0892-XX MicroLab I Mainframe	To provide interface between the 067-0911-00 Diagnostic Interface and the RS232-compatible terminal. Provides a display of certain test data as well as limited keypad input compatibilities to the test system.	TEKTRONIX MicroLab I Mainframe.
RS232-Compatible Display Terminal, 300-2400 Baud	To provide most of the user/machine interface for diagnostic operations. Provides display of test data and system operating messages as well as keyboard input to the diagnostic system.	TEKTRONIX 4000-series Computer Display Terminals, RS232 compatible.
Signature Analyzer	To take required signatures in those procedures involving signature analysis techniqes.	SONY-TEKTRONIX 308 Data Analyzer.
Oscilloscope; 15 MHz Band-Width Dual Trace	To provide for real-time examination of 7854 Oscilloscope test waveforms.	TEKTRONIX 7704A Oscilloscope.
GPIB Controller	To exercise GPIB circuitry.	Electronics Corporation Model 4810 Bus Fault Analyzer.
067-0912-00 Analog Test Card	To isolate faults to either the analog or digital portion of the 7854 Oscilloscope. Provides minimal digital control functions so analog portion of instrument will operate.	Tektronix 067-0912-00 Analog Test Card.
067-0913-00 067-0914-00 067-0915-00 Multi-Pin Extender Boards	To extend digital boards for troubleshooting purposes.	TEKTRONIX 067-0913-00, 067-0914-00, 067-0915-00 Extender Boards.
7B87 Time Base	To provide internal and external digitizing clocks to the 7854.	TEKTRONIX 7B87 Time Base.

*** NOTE: The 067-0911-XX Diagnostic Test Interface consists of 3 board assemblies; Cable Termination Assembly A1 (with cables), Test Processor Board A2 and Interface Board A3.**

TABLE 2-1 (CONT)
Diagnostic Test Equipment

Description	Purpose	Examples of Applicable Test Equipment
7000-Series Time Base	To provide various sweep functions.	TEKTRONIX 7B92 A Time Base.
Signal Standardizer	To provide know value analog inputs to the digitizer system for functionality checks.	TEKTRONIX 067-0587-02 Signal Standardizer
Jumper Wires (several)	To short various pins together for test purposes.	Short wires with TEKTRONIX 003-0624-00 clips attached.

TERMINAL TURN-ON PROCEDURES

Turn on procedures for the diagnostic system vary with the display terminal used in the test setup. For all Tektronix 4000-series terminals with the exception of 4050-series instruments, the following turn-on procedure applies:

1. Set the rear-panel baud rate switch to 2400.
2. Turn on the terminals power switch.
3. Press the TTY Lock key to allow the terminal to input upper-case characters only.

If a 4050-series terminal is to be used, Option 01 is required. Turn-on for 4050-series graphic display terminals is as follows:

1. Turn on the terminals power switch. Wait a few seconds, then press the HOME PAGE key.
2. Press the SHIFT key and USER DEFINABLE key number 16 simultaneously. (This locks out the local echo feature of 4050-series terminals.)
3. Press the TTY Lock key to allow the terminal to print only upper case characters.
4. Type: CALL "RATE", 2400,0,2 to set the RS-232 baud rate to 2400.
5. Type: CALL "TERMIN" to set the instrument to terminal mode. The status indicators will shift between I/O and BUSY.

NOTE

To avoid system lockup when powering up 4050-series terminals, the MicroLab I must remain off until steps 1 through 5 above have been performed. In the event of system lockup, turn off all test equipment and perform the turn-on procedure in the proper order.

DIAGNOSTIC INTERFACE SELF TESTS

Before beginning any of the 7854 Oscilloscope diagnostic tests, a verification of the Diagnostic Interface/MicroLab I system should be performed as follows:

1. Install the 067-0911-XX Test Processor Board-A2 into J130 of the 067-0911-XX Cable Termination Board-A1 (see figure 2-1).
2. Turn the MicroLab I power on. The 067-0911-XX power-up test will be performed automatically.
3. Type ST<CR> on the terminal keyboard to initiate the remainder of the self test. The rest of this test does not run automatically. Refer to the description of The 067-0911-XX Self Test in Section 7 of this manual for specific information concerning user interaction with this test.

   If the test is not performed satisfactorily or if an error message appears, refer to the 067-0911-XX Self Test procedure at the end of this section and to the 'ST' command description in section 7.

If the test is performed satisfactorily, the Diagnostic Interface/MicroLab I system is working properly. Turn off the MicroLab I power and remove the 067-0911-XX Test Processor Board from J130 of the 067-0911-XX Cable Termination Board and set it aside. (The 067-0911-XX Test Processor Board is only used to test the Diagnostic Interface/MicroLab I system and will not be used when testing the 7854 Oscilloscope.)

WHICH TESTS DO I NEED TO RUN?

Prior to performing any detailed testing of the digital portion of the 7854 Oscilloscope, any problem should be isolated to a functional section of the instrument. This is done primarily through a self-test feature designed into the 7854's power-up routine firmware. This feature provides that, each time power is applied to the 7854, a self test sequence is automatically performed. The status of the various functional blocks within the oscilloscope is denoted on the various front-panel indicators upon completion of the sequence. These power-up tests are not all-inclusive but are meant to provide an indication as to where a fault may lie. The sequence of the power-up test is as follows.

Step 1: When power is applied the following indicators will light: POWER, selected positions of the A and B TRIGGER SOURCE switches, and all selected indicators on the plug-in units. The following indicators will remain off for approximately three seconds after power-up; all positions of the VERTICAL and HORIZONTAL MODE switches, all intensity indicators, and all red, front panel (measurement keyboard) and Waveform Calculator indicators.

Step 2: All positions of the VERTICAL and HORIZONTAL MODE switches, all INTENSITY indicators, and all red front panel and Waveform Calculator indicators will now light.

Step 3: A fault condition found through any of the four tests is indicated with the lights of the VERTICAL and HORIZONTAL MODE switches. Fault condition codes are listed in Table 2-2.

If a fault code occurs, press any button of the VERTICAL or HORIZONTAL MODE switches and the self-testing will continue.

Troubleshooting procedures for each board in the digital portion of the 7854 can be found later in this section.

TABLE 2-2
Self-Test Fault Codes

VERTICAL MODE Indicator Status	HORIZONTAL MODE Indicator Status	Circuitry With Fault
All lights on.	B light on.	RAM
All lights on.	CHOP light on.	ROM
All lights on.	CHOP and B lights on.	Real time Clock
All lights on.	ALT light on.	Display

Step 4: Successful completion of the self tests is indicated by the issuance of the audible warning tone (if the rear panel AUDIBLE WARNING switch is ON), and the extinguishing of all red indicators, the Stored Int and A Intensity indicators, all VERTICAL MODE lights except LEFT, and all HORIZONTAL MODE switch lights except B. In addition, if the READOUT intensity control is set to at least midrange, the message **SELF TEST COMPLETE**, will be displayed on the crt.

Refer to the Maintenance section of the 7854 Service Manual if an analog problem appears to be present.

POWER-UP PRESET CONDITIONS

After successful completion of the processor self tests, several parameters of the 7854 are set to predetermined conditions (only when using 7854's normal ROM). These power-up conditions are:

CRT DISPLAY mode ..... Set to SCOPE
Program Mode ..... Set to EXECUTE
Program Memory ..... Cleared
VERTICAL MODE ..... Set to LEFT
HORIZONTAL MODE ..... Set to B
Stored Waveform Display ..... Not displayed; set to VECTors
P/W (Points/Waveform) ..... Set to 512
Stack Registers ..... Cleared to 0
OPW (Operational Waveform) ..... Set to 0
All waveform memory points ..... Set to the zero value (center horizontal graticule line)
VZR (Vertical Zero Reference ..... Set to 0 (all waveform memories)
Vertical Scale Factor ..... Set to 1 (all waveform memories)
Vertical Scale Factor Unit ..... Set to V (all waveform memories)
Horizontal Scale Factor ..... Set to 1 (all waveform memories)
Horizontal Scale Factor Unit ..... Set to S (all waveform memories)
Constant Registers ..... Set to 0
TTL Output ..... Set HIGH
rsv control flags ..... Set ON

If the 7854 power up test is completed successfully, but a fault is still suspected within the digital portion of the instrument, it is time to make use of the diagnostic capabilities of the 067-0911-XX system. Turn off the 7854 Oscilloscope and perform the steps given on the INITIAL TESTS" flowchart.

USING THE CALIBRATION FIRMWARE

Part of the firmware contained on the 067-0961-XX Diagnostic Memory Board produces waveform and character information that may be displayed on the crt of the 7854 Oscilloscope for a separate Display calibration procedure. This procedure is included in the 7854 Service manual. (Early manuals do not have this procedure.)

With 067-0961-XX Diagnostic Memory Board installed in the 7854 without any other test equipment attached and with the calibration keyboard overlay in place, the calibration displays may be invoked from the 7854 front-panel keyboard as described below. With the remainder of the test equipment connected as shown in Figure 2-1, use of the calibration firmware is initiated by typing CA <CR> on the terminal keyboard. Invocation of the individual calibration displays now follows identically to the "stand-alone" configuration mentioned above. These individual displays are invoked as follows (refer to Figure 2-2, Keyboard Overlay or to the overlay itself for keynames):

SCOPE—Causes realtime waveform to be displayed. Press SCOPE key to invoke.

STORED—causes stored waveform to be displayed. Press STORED key to invoke.

BOTH—causes both the stored and realtime waveforms to be displayed. Press BOTH key to invoke.

DOT—sets the display to dot mode for matching specific points to the crt graticule. Press DOT key to invoke.

VECT—sets the display to vector mode for adjusting vector display circuitry. Press VECT key to invoke.

128, 256, 512, 1024—sets waveform resolution to the corresponding number of points. Press either 128, 256, 512 or 1024 key to invoke.

LED—sounds the audible warning (if rear panel AUDIBLE ERROR/WARNING switch is on) and lights all front-panel indicators for functionality check. Press LED key to invoke. Press any other key to terminate.

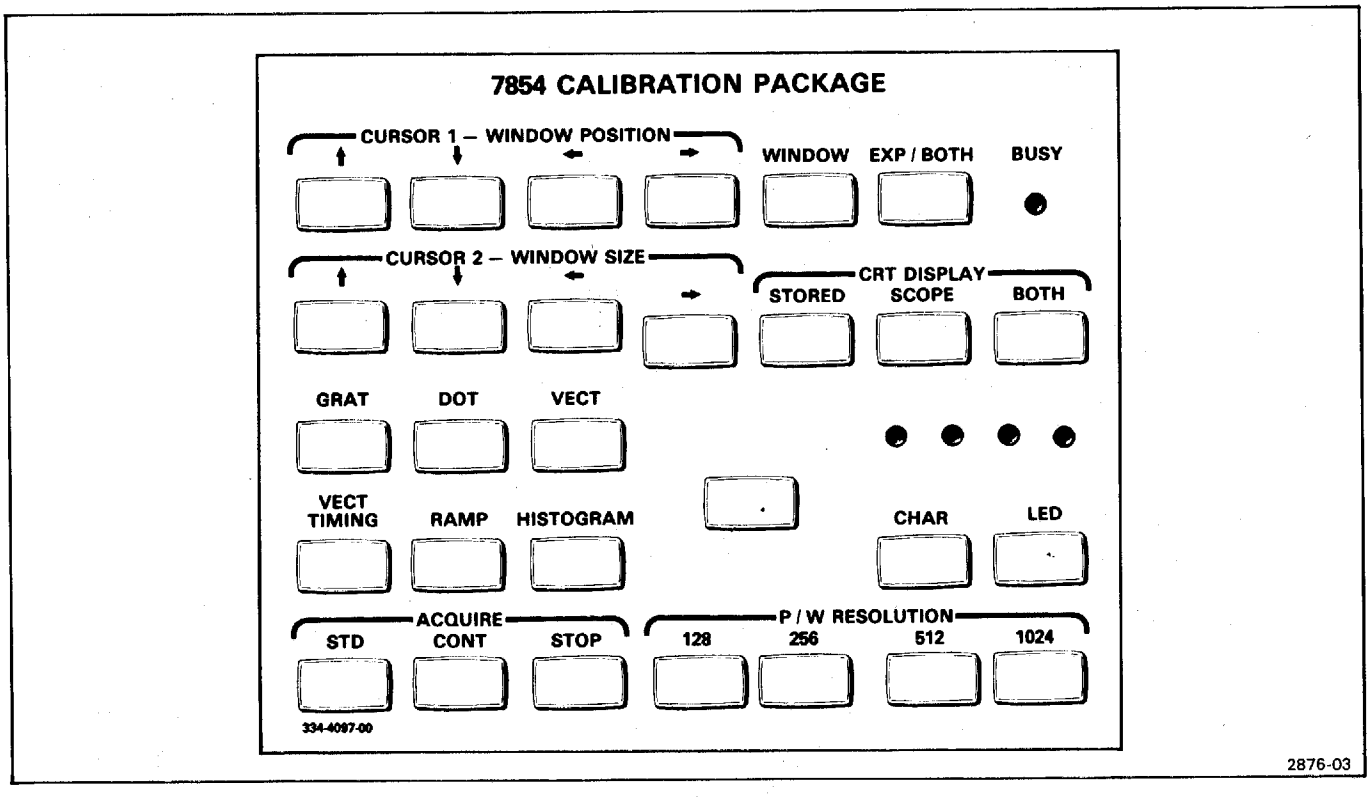

Figure 2-2. Keyboard Overlay.

CHAR—causes a full-screen display of characters as they are sequentially read from the display systems character ROM. Used to check proper writing of each character and for setting alphanumeric readout boundries. Press CHAR key to invoke.

SAMP—generates a histogram showing how many times each horizontal point is sampled. Press the SAMP key to invoke.

GRAT—generates a display similar to the crt graticule. In VECTor mode, the display should be superimposed on the graticule. In DOT mode, dots should appear at each intersection of the graticule lines. Press GRAT key to invoke.

RAMP—generates a 45 degree ramp containing 512 points for checking display linearity, gain and centering. Press the RAMP key to invoke.

VECT TIMING—generates a rectangular waveform subdivided into four smaller rectangles for adjustment of the 7854 vector display circuitry. In VECTor mode, the display should be super-imposed on crt graticule lines. In DOT mode, dots appear on crt graticule lines. Press VECT TIMING key to invoke.

STD ACQUIRE—performs one complete standard acquire cycle for observing signals applied to oscilloscope inputs. Non-acquired points are held offscreen (7854 firmware interpolates points into waveform). Press STD ACQUIRE key to invoke.

CONT ACQUIRE—performs a continuous acquisition of signals applied to oscilloscope inputs for adjusting portions of the display circuitry. Press CONT ACQUIRE key to invoke.

STOP ACQUIRE—terminates a continuous acquisition. Press STOP ACQUIRE key to invoke.

WINDOW (ON/OFF)—either enables or disables a display window that may be moved to any location on the crt display. Area inside window is magnified to full screen and displayed as continously updated stored information. CONT AQR must be invoked for the window to be functional. In addition, the READOUT intensity control must be on for the window to be visible. Press WINDOW (ON/OFF) (after pressing CONT AQR) to invoke.

EXP/BOTH—displays either expanded display only or expanded display, realtime display and expansion window all simultaneously. The expansion WINDOW must have been previously invoked. Press EXP/BOTH key to invoke other display format.

CURSOR 1—POSITION ↑, ↓, ←, and → moves expansion window on crt. Press POSITION ↑, ↓, ←, or → to move window in desired direction.

CURSOR 2—SIZE ↑, ↓, ←, and → moves cursor 2 with respect to cursor 1 resulting in a change in size of the expansion window. Cursor 2 may "cross over" the position of cursor 1 in either the horizontal or vertical direction. Press SIZE ↑, ↓, ← or → to change window size.

Blue Key—no function assigned.

OPERATOR INTERFACE WITH THE DIAGNOSTIC SYSTEM

This section contains the basic operator interfacing techniques required to use the 067-0911-XX Diagnostic Test Interface system for troubleshooting the 7854 Oscilloscope. Operator interface may be via the 7854, MicroLab I or RS232-compatible terminal. Each is more fully described below.

INTERFACE VIA THE 7854

Upon power up of the 7854 Oscilloscope (with normal 7854 ROM installed), various front-panel indicators may remain illuminated. If indicators other than the B INTENSITY, LEFT VERTICAL, RIGHT HORIZONTAL and TRIGGER SOURCE lights stay on, the power up diagnostics have detected a fault in the digital portion of the oscilloscope. The error codes corresponding to faults detected during the power-up test are given in table 3-1. For a more complete description of the 7854 power-up test, refer to 'Which Tests Do I Need To Run?' in section 2 of this manual.

TABLE 3-1
Self-Test Fault Codes

VERTICAL MODE Indicator Status	HORIZONTAL MODE Indicator Status	Circuitry with fault
All lights on	B light on	RAM
All lights on	CHOP light on	ROM
All lights on	CHOP and B lights on	Real-time clock
All lights on	ALT light on	Display

Other diagnostic tests or procedures may require the operator to install plug-ins and change various mode settings of both the plug-ins and the 7854 Oscilloscope. These installation and setup instructions are given at the appropriate point in the individual test procedures. In addition, use of the Calibrate (CA) command requires the operator to press most of the keys on the 7854 front-panel keyboard. Further information about user interaction via the 7854 with specific Diagnostic System commands may be found in the Command Dictionary, Section 4.

INTERFACE VIA THE TERMINAL

The RS232-compatible terminal is the primary means of user interaction with the Diagnostic System. The Diagnostic System presents system power-up status information, command prompts, error codes, data resulting from command execution as well as some informational type data to the user via the terminal crt. Most of command entry to the Diagnostic System is via the terminal keyboard.

Initially, upon power up of the system, a sign-in message and a power up message are displayed on the terminal crt. (Remember that 4050 series terminals have a special turn-on procedure outlined in the Installation instructions given in section 2.) After the power-up message, a system prompt (>) will be displayed indicating that the system is waiting for the user to enter a command. Commands are entered according to the syntax and parameter guidelines given in the Command Dictionary, Section 4.

In addition to command entry to the diagnostic system via the terminal, execution of a diagnostic routine may be terminated from the terminal keyboard. Pressing the ESCape key will return the test sequence to the TEK-DCL operating system from execution of most commands. Return to the operating system is indicated by a system prompt (>) at the left of the crt screen. New commands may now be entered.

ESCape will also cancel any command typed until entered with a carriage return. BACKSPACE and RUBOUT may be used to correct typing errors when entering commands.

When using 4050-series and other 'storage' terminals, the display will dim after a period of no input via the keyboard. To refresh the display without causing any interaction with a command that may be waiting for keyboard input, press either of the SHIFT keys. Pressing the HOME PAGE key will clear the crt display.

Operating system messages to the user vary with the command being executed. Refer to the specific command descriptions given in Section 4, Command Dictionary. Error messages that may be encountered are explained in the appropriate flowchart test procedure and in the Error Message Table at the end of this manual.

MICROLAB I FRONT-PANEL INTERACTION

User interaction with the test system via the MicroLab I is by a front-panel display and keyboard. Depending upon the test being run, the MicroLab I will display certain

types of system status and error information to the operator. These status and error messages are explained in the Command Dictionary, Section 4.

In addition, certain of the diagnostic commands require the operator to press certain MicroLab I front-panel keys at specific points in the test procedures. These instances are also indictated in the Command Dictionary and at the required points in the test procedures.

Pressing the RESET key on the MicroLab I will return the test sequence to the TEK-DCL operating system and will clear the system from a locked up condition. Anytime the RESET key is pressed however, the test sequence must be restarted from the beginning by inputting the command via the terminal keyboard.

The SPECIAL key, when pressed, will usually return the 7854 to its "SCOPE" mode for observing realtime waveforms. In order to return to the diagnostic system after pressing the SPECIAL key, either the MicroLab I RESET key or the terminals ESCape key must be pressed.

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COMMAND DICTIONARY

This section describes the set of troubleshooting commands available to aid in the location of defective components on the digital boards of the 7854 Oscilloscope. These commands are designed to be used in conjunction with the troubleshooting trees, signature tables, schematics and circuit descriptions located in other sections of this manual package. The following commands are resident in the basic operating system (TEK-DCL) PROM's and the 067-0961-XX Diagnostic Memory board.

DEBUG/UTILITY COMMANDS

This part describes the set of troubleshooting commands that may be used in conjunction with the Diagnostic Commands (during 7854 Oscilloscope maintenance operations) to assist in locating malfunctions. The following commands are resident in the basic operating system (TEK-DCL) PROM's and may be used in any test configuration.

INDEX TO DEBUG/UTILITY COMMANDS

BK [BREAKPOINT]

The Breakpoint command initiates a breakpoint interrupt in the 7854 Oscilloscope microprocessor operations when certain conditions occur at a specified memory location. When the interrupt occurs, the status of the microprocessor and its register values are displayed on the diagnostic terminal screen (see Table 4-1).

This command is invoked whenever the BK, [Access Code], [Condition Code] [Address Code], and <CR> is entered on the diagnostic terminal. The parameters Access Code, Condition Code and Address Code are defined in the following paragraphs.

NOTE

The parameters must be entered in the sequence [Access Code] [Condition Code] [Address Code] with space or comma delimiter separation.

ACCESS CODE

The Access Code allows operator selection of any of the four access types for which the breakpoint is to occur to the specified memory location [address].

1. AL = all accesses.
2. RE = read accesses only.
3. WR = write accesses only.
4. FE = all fetches.

CONDITION CODE

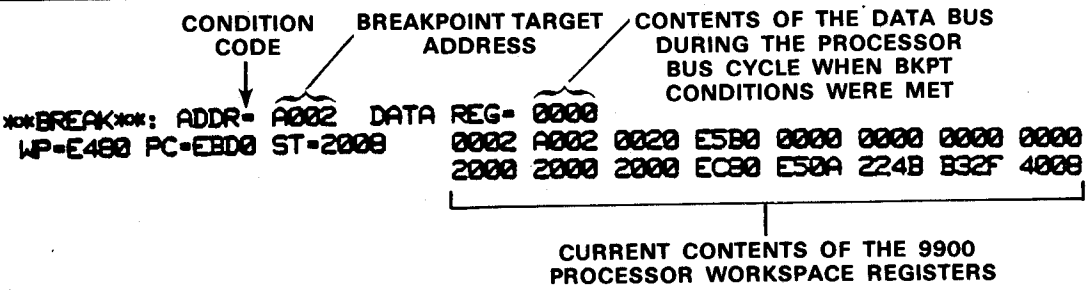
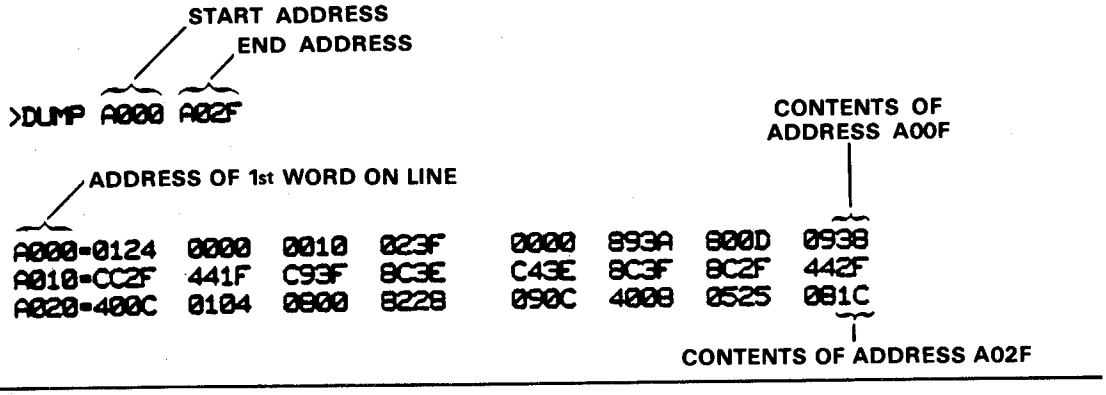
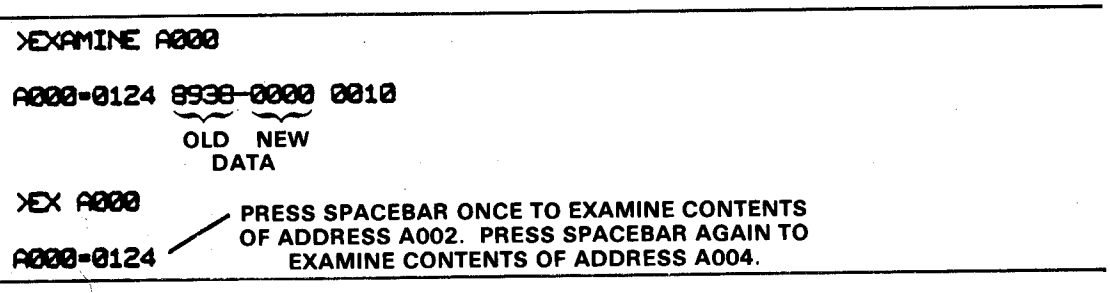
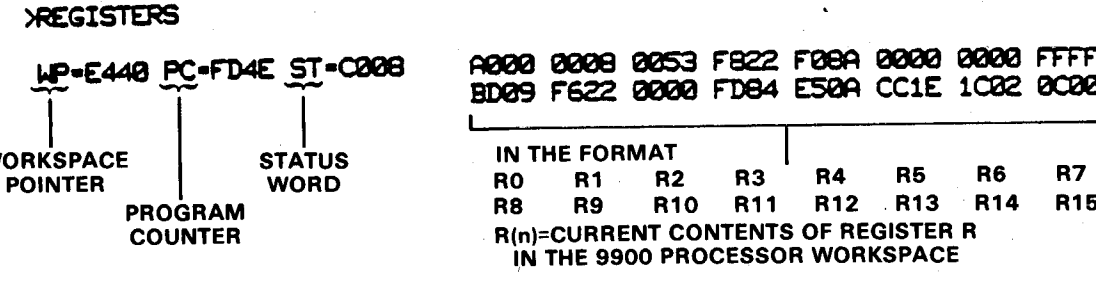
The Condition Code allows operator selection of the conditions to be compared with the specified breakpoint address. The three conditions are:

1. EQ = equal to breakpoint address.

NOTE

Break on any address is allowable, however, a breakpoint set on address 000A or 000C (the terminal interrupt vector) will cause unpredictable results.

Table 4-1
Examples of Diagnostic Terminal Printout of
Various Debug Commands

COMMAND	EXAMPLE
BREAKPOINT	
DUMP MEMORY	
EXAMINE	
LIST BREAKPOINT	
REGISTERS	

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2. GR = greater than the breakpoint address but less than address E380.

NOTE

When the maskable RAM on the 911 Interface Board (A3) is enabled, the "GR" breakpoint will not function in the address range of 9800 through 9FFF.

3. LE = less than the breakpoint address but not less than address 8000.

ADDRESS CODE

The Address Code represents the hexadecimal address at which microprocessor executions are to be interrupted when breakpoint conditions are met.

NOTE

If a breakpoint command is entered for non-allowed addresses, the command will set up the registers with the appropriate values but will ignore the breakpoint.

CB [CLEAR BREAKPOINT]

The Clear Breakpoint command clears any breakpoint previously set by a Breakpoint command. This command is entered at the terminal keyboard and has no output response back to the terminal.

NOTE

To verify the Breakpoint has been cleared, type 'LB' <CR> (LIST BKPT). The terminal should respond with 'BK NOT SET'.

This command is invoked whenever CB <CR> is entered on the diagnostic terminal. There are no operational parameters applicable to this command.

DU [DUMP MEMORY]

The Dump Memory command allows the operator to display the contents of one or more lines of memory beginning at a specified address. The contents of one line of memory (8 words) may be displayed by entering a starting address only. The contents of one or more lines of memory is displayed by specifying a beginning and ending address (see Table 4-1).

This command is invoked whenever DU [start address] <CR> (to display one line of memory only) or DU [start address] [end address] <CR> (to display one or more lines of memory) is entered on the diagnostic terminal.

The diagnostic terminal will print [start address] [contents] of one line (8 words) for any number of lines specified by an ending address (see Table 4-1).

The [start address] is printed for the location of the first word of each line only.

NOTE

The ending address is optional and need not be specified. If it is specified, it must be greater than the beginning address. If no parameters are specified, the Dump command will display one line starting at the current program counter location if the Dump or Examine command has previously been invoked, otherwise the execution will be in error. Any memory address can be displayed by this command.

EX [EXAMINE MEMORY]

The Examine command allows for examining memory locations in both the 7854 Oscilloscope firmware and the 911 firmware. In addition to allowing examination of the contents of any of the selectable RAM locations, the command also allows those contents to be changed to any desired value. The accessible memory locations are A000-DFFF for the 7854 RAM, E400-E7FF for the 911 RAM, and 9800-9FFF for the 911 RAM (maskable) and E000 - E3FF for 7854 and 067-0911-00 hardware registers.

NOTE

'Write only' registers, when written to, will produce an 'ERROR 10' message on the diagnostic terminal.

This command is invoked whenever EX [address] <CR> is entered on the diagnostic terminal.

The [address] is the memory location to be examined.

NOTE

If no address is entered, the address accessed is an arbitrary number. The diagnostic terminal will print the specified [address] [contents] (of the address). The contents of each address appear as two hexadecimal digits.

The routine will zero-fill the address entered if less than four digits are entered.

The following entries provide display and altering functions within the Examine command:

Space Bar—Displays the contents of the next address.

Line Feed—Moves the display cursor to the next line, displays the current address and its contents.

Return or ESC—Terminates the command. Memory locations altered before pressing the ESC or RETURN key remain altered.

RUB OUT—Moves the display cursor to the next line, displays the previous address and its contents.

When the contents of memory is altered, a hexadecimal data string replaces the current data. The system displays a hyphen between the new and the old data in the following format: [memory location] = [old data] - [new data] (see Table 4-1).

GO [GO]

The Go command allows the operator to begin execution of a program at a specified memory location, and is designed as a debug aid in isolating various faults. This command is invoked whenever GO [address] <CR> or GO <CR> is entered on the diagnostic terminal.

If GO <CR> is entered, program execution resumes at the point just prior to the point at which the operator pressed the <ESC> key, or at the point that a diagnostic command suspends operation. ("Halt on Error" option.)

NOTE

The address is an optional parameter that may be entered when using the GO command. If this optional address parameter is not entered, the routine will default to the address stored when the last terminal ESC key was pressed. If the address is in the range of E800-EFFF the correct half of the bank-switched memory will also be restored. If the escape key is pressed twice and the operator types GO <CR> the command will be lost and the results will be unpredictable. Should this occur, the RESET key on the MicroLab I front panel must be pressed to restart the system.

HE [HELP (COMMAND MENU)]

The Help command lists all of the valid commands available in the TEK-DCL system. The list is displayed on the diagnostic terminal screen.

This command is invoked whenever HE <CR> is entered on the diagnostic terminal.

The list of commands displayed by the use of the Help command depends upon the diagnostics system configuration being used. If the 7854 Oscilloscope is connected to the 911 and its 7854 ROM card is installed, or the 911 Test Processor Board (A2) is connected to the 911, only the commands resident in the basic operating system will be displayed. If the 961 Diagnostic Memory Board is installed in the 7854 Oscilloscope instead of the normal ROM card and the oscilloscope is connected to the 911, the entire set of diagnostic commands as well as those resident in the basic operating system (TEK-DCL) will be displayed as follows:

7854 DIAGNOSTIC SYSTEM COMMANDS

BK	[BREAKPOINT]
CB	[CLEAR BREAKPOINT]
EX	[EXAMINE MEMORY]
DU	[DUMP MEMORY]
GO	[GO]
LB	[LIST BKPT STATUS]
RE	[REGISTERS]
HE	[HELP (COMMAND MENU)]
RO	[ROM CHECKSUM]
ST	[SELF TEST]
RS	[ROM S/A]

067-0961-XX COMMANDS

BB	[RAM BATTERY BACKUP]
CA	[CALIBRATE]
CL	[CONTROL LOGIC]
CR	[CRU UTILITY]
DG	[DIGITIZER]
DS	[DISPLAY]
GP	[GPIB]
MP	[MPU, SIG, ANAL.]
RA	[RAM TEST]
SE	[SET PARAMETERS]
TI	[REAL TIME CLOCK]

LB [LIST BREAKPOINT STATUS]

The List Breakpoint command informs the operator of the current status of the breakpoint register. It allows the operator to verify the breakpoint is set and also what conditions will cause the breakpoint interrupt to occur.

This command is invoked whenever LB <CR> is entered on the diagnostic terminal.

RE [REGISTERS]

The Register command allows the operator to display the contents of the 7854 Oscilloscope 9900 microprocessor workspace pointer, program counter, status register and the (16) general purpose registers (see Table 4-1). This command is designed for debug situations in which specific processor information is useful.

This command is invoked whenever RE <CR> is entered on the diagnostic terminal.

There are no operational parameters applicable to this command.

DIAGNOSTIC COMMANDS

The following diagnostic commands have been devised specifically for troubleshooting the hardware (digital only boards) of the 7854. These commands are resident in the 067-0961-XX Diagnostic Memory Board and the 067-0911-00 Operating Systems (TEK-DCL) PROMs.

Each command initiates a test sequence for troubleshooting a particular function. An index of the Diagnostic Commands followed by detailed descriptions and invocation procedures for each, is given following the Set Parameter Selection and Invocation information.

'SET' PARAMETER SELECTION AND INVOCATION

The Set Parameters are a group of commands used to assign specific troubleshooting characteristics to a particular diagnostic command. All of the functions are operator selectable, and once set, will not change from diagnostic-to-diagnostic.

The Set Parameters applicable (if any) to a particular diagnostic command are listed and defined at the beginning of that particular command description.

SE ST (Set Status) <CR>—This command identifys the parameter in force, if any.

SE CL (Set Clear) <CR>—This command clears all parameters in force.

SET [Parameter]—This command actually sets the desired parameter. Up to 4 parameters may be set in any order.

The Set Parameters are:

LB (Loop on Batch)	NP (No Loop on Pass)
NB (No Loop on Batch)	HE (Halt on Error)
LE (Loop on Error)	NH (No Halt on Error)
NL (No Loop on Error)	DI (Disable Error Message)
LP (Loop on Pass)	ND (Re-enable Error Messages)

INDEX TO DIAGNOSTIC COMMANDS

BB [BATTERY BACKUP]

The Battery Backup command provides the means for checking the operation of the battery backup circuitry.

This diagnostic is run whenever BB <CR> is entered on the diagnostic terminal.

NOTE

The Battery Backup command requires that a backup battery be connected to the 7854 Oscilloscope, and requires some manual operator intervention.

Once invoked, the routine loads a 1k-word block from TEK-DCL PROMS (locations F000-F7FF) into the 7854 RAM. The terminal will then print the message: 'RAM IS LOADED'

The operator then interrupts the 7854 power momentarily (with the battery backup connected).

Upon second execution of the command BB <CR>, the memory within the MicroLab I mainframe is checked to determine that this is the second execution of the command BB.

The contents of RAM locations A000-A7FF are then compared with the 1K-word block to determine that the data was held in memory during power interruption.

Depending on the above results the diagnostic terminal prints:

```
BATTERY BACKUP VER 1.0
TEST [PASSED]
       FAILED
```

CA [CALIBRATION]

The Calibration command allows invocation of a firmware package to aid calibration of the waveform acquire and display functions of the 7854 Oscilloscope. Those calibration procedures are contained in the 7854 Oscilloscope Service Manual.

The 7854 Calibration Package may be invoked in any one of the following 3 ways:

NOTE

The 067-0961-XX must have been installed.

1. Automatically upon power up of the 7854, if the 7854 Diagnostic Interface (067-0911-XX) is not connected to the 7854 under test.

2. Manually, by typing CA <CR> on the diagnostic system terminal.

3. Manually, by pressing the key marked 'SPECIAL' on the MicroLab I front panel.

When the Calibration Package is invoked by typing CA <CR> on the diagnostic system terminal, the terminal responds with the following message:

```
7854 CALIBRATION PACKAGE
PRESS <ESC> TO EXIT
```

Once invoked, the calibration package runs independent of the 067-0911-XX/MicroLab I system. All operator interaction is performed via the 7854 front-panel keyboard. See Figure 4-1 for calibration function designations for front-panel keypads of the 7854. The Calibration Package may be interrupted and control returned to the TEK-DCL Operating System by pressing the <escape> key on the diagnostic terminal.

CALIBRATION SUBROUTINE FUNCTIONS

NOTE

All of the following subroutines are called up via the 7854 front-panel keyboard.

STD AQR—(Standard Acquire) acquires repetitive real-time waveforms with readout and stores result in waveform memory. This subroutine does not interpolate off-screen undefined points into the waveform.

CONT AQR—(Continuous Acquire) Continuous acquisition.

NOTE

Once memory space is full, new points will overwrite previously acquired points.

STOP AQR—(Stop Acquire) Stops the continuous acquire function.

STORED Mode—Displays the digitized waveforms only.

SCOPE Mode—Displays the realtime waveforms.

BOTH Mode—Displays the realtime and the stored mode display.

128, 256, 512, 1024—Allows selection of acquire and display resolution to the specified number of points per waveform as indicated on the pushbutton.

GRAT—Displays a graticule and draws vectors over the graticule lines and places dots at the intersections. This function is used to aid positioning of dot and vector displays.

NOTE

The resolution keys (128, 256, 512, 1024) will not affect the display resolution of the grat function (set to 512 p/w).

DOT—Causes the digitized waveform to be displayed in dot mode.

VECT—Causes the digitized waveform to be displayed in Vector mode.

VECT TIMING—Displays a waveform containing both long and short vectors. Assists in adjusting vector length.

NOTE

This waveform is displayed with 512 points per waveform resolution only. The resolution keys have no effect on this function.

@

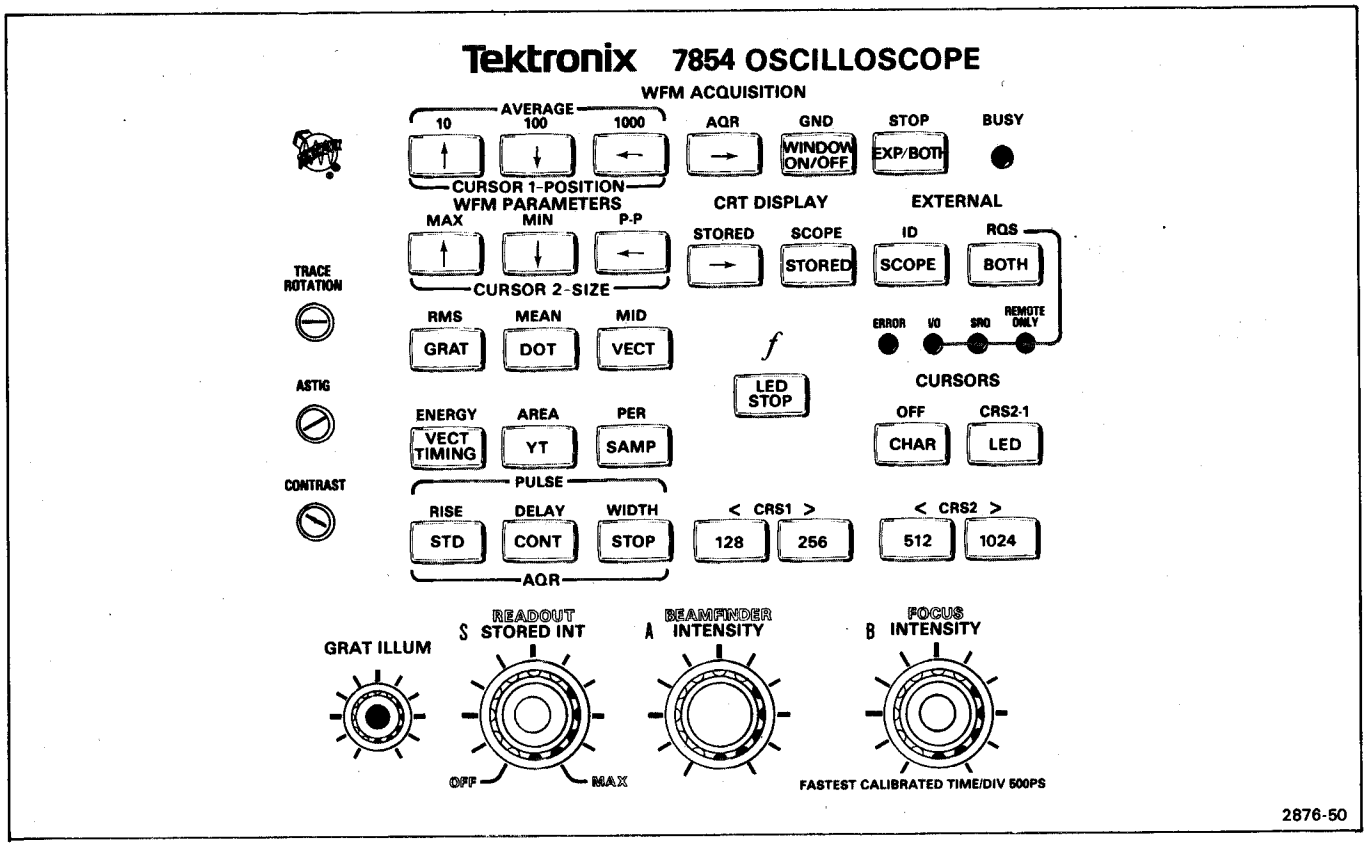

Figure 4-1. 7854 Front Panel Button board nomenclature with 067-0961-XX Diagnostic Memory board installed.

YT—Displays a ramp containing 1024 points. The ramp is generated by incrementing the 10-bit display word in the LSB.

NOTE

Since the least significant bit of the display word is always 0, some of the display hardware may not be exercised.

SAMP—Creates a histogram showing the number of times each point in the waveform has been sampled and acquired. The acquisition is terminated automatically when the histogram goes beyond the top of the screen.

To terminate the histogram function, press any other key on the 7854 front panel.

WINDOW ON/OFF
EXP/BOTH
CURSOR 1—(WINDOW) POSITION ↑↓← →
CURSOR 2—(WINDOW) SIZE ↑↓← →

NOTE

Continuous acquire must be running for these keys to work.

These keys allow for magnification of a selectable portion of a continuously acquired waveform. The [WINDOW ON/OFF] key displays a window which delineates a portion of the waveform that is then expanded to full screen. If the window is currently displayed, pressing the [WINDOW ON/OFF] key disables the window feature. The expanded waveform display is disabled while the window is being changed, but the display is updated once the cursor positioning keys are no longer being slewed.

The window can be positioned using the CURSOR 1—(WINDOW) POSITION positioning keys (the window size is unchanged.) The window size and shape is determined by the CURSOR 2—(WINDOW) SIZE positioning keys.

Both the stored and expanded waveforms are normally displayed. To display only the expanded waveform, press the [EXP/BOTH] key. Press the [EXP/BOTH] key again to switch back to displaying both the stored and expanded waveform.

NOTE

The window cannot be manipulated by use of the cursor keys if the EXP/BOTH key was used to show the expanded waveform only.

LED—Turns on the front-panel LED's, the mode switch lights, the 'S', 'A', and 'B' lights. The speaker will emit a continuous tone (audible ERROR WARNING switch on the rear panel must be ON).

Pressing any other 7854 front-panel key will deactivate the speaker and lights.

This function is used for testing front panel LED's, mode lights and speaker.

CHAR—Fills the display with characters (16 lines with 40 characters each). This key is used to position the character display and to check character quality.

CL [CONTROL LOGIC]

The Control Logic command allows the invocation of a complete set of diagnostic, troubleshooting, and fault isolation routines for the 7854 Oscilloscope Control Logic circuits (A26—Control Logic board). The command consists of a linked set of subtests that may be called individually or in a predefined sequence.

Some of the Control Logic subtests are shared with the Display command. Those subtests are identified in the subtest descriptions.

NOTE

The Control Logic diagnostic package requires functionality of the 7854 Oscilloscope MPU Board (A27) and RAM Board (A28). Proper operation of these two boards is assumed and the Control Logic diagnostics make no effort to verify such.

The Control Logic diagnostic object code resides on the 067-0961-XX Diagnostic Memory Board. Therefore, it is necessary that the 7854 Oscilloscope A31-ROM Board be removed and the 067-0961-XX board installed. If the operator attempts to invoke the Control Logic diagnostics without having done so, the TEK-DCL systems will ignore the CL command and report an Error 06 on the Terminal screen.

The Control Logic diiagnostic can be invoked by either of two methods.

1. Type 'CL' <CR> on the diagnostic terminal to run all ten subtests consecutively beginning with subtest 01.

2. Type 'CL [Subtest Number]' <CR> to skip any number of consecutive subtests beginning with subtest 01.

   For example, type 03 for [subtest number] and the control logic diagnostic begins the routine at subtest 03 (skippping subtests 01 and 02) and continues through subtest 10.

If the diagnostic terminal responds with the message '**ERROR 06', check that the 067-0961-XX Diagnostic Memory board is properly installed and functional. No response or a response other than listed above indicates a failure of either the 7854 MPU board or the 067-0911-00 Diagnostic Interface.

After printing the message 'Control Logic [Version], the Control Logic diagnostic will print the message '7B80 and 7B87 INSTALLED?' Setup the timebases as shown in Table 4-2.

The subtests for the Control Logic diagnostics package are listed in Table 4-3 and defined functionally in the paragraphs that follow.

SET PARAMETERS

The external Set Parameters for the Control Logic diagnostic are defined as follows:

NOTE

For invocation of Set Parameters, refer to Set Parameter invocation procedure at the beginning of this section.

HE (Halt on Error)—When an error is detected in a subtest, the subtest reports an error message on the diagnostic terminal screen and returns to the TEK-DCL operating system. The operator may then restart the diagnostic at the point where the error was detected by entering GO <CR> at the diagnostic terminal keyboard.

LE (Loop on Error)—When an error is detected in a subtest, the subtest reports an error message on the Terminal screen, then enters the troubleshooting loop defined for that subtest. The HE option will override the LE option.

Table 4-2
Timebase Setup Conditions for Control Logic Diagnostic

CONTROL	TIMEBASE	
	*A	**B
TIME/DIV	0.2 ms	0.2 ms
MAG	X1	X1
TRIGGERING	AUTO	AUTO
	AC	AC
	INT	INT
ACQUIRE CLOCK		INTERNAL

*** Timebase A - 7B80 or equiv.**
****Timebase B - 7B87**

@

LB (Loop on Batch)—The control logic diagnostic routine, upon completing Subtest 10 (A-Word/B-Word Interaction Subtest), returns to the subtest specified by the beginning subtest identifier parameter (or to Subtest 01. If no parameter has been entered), rather than returning to the TEK-DCL operating system. Further, any subtests that require operator intervention (such as scope loops) are skipped.

DI (Disable Error Messages)—This option is not implemented.

LP (Loop on Pass)—A subtest enters its associated signature analysis or scope loop if the subtest can detect no errors in its fault detection mode of operation.

01—READOUT ACQUIRE DMA

This diagnostic module verifies that the Readout Acquire DMA channel is able to execute memory write cycles to the proper areas of the 7854 RAM space. The test does not check for correctness of data, only that data was written in the proper areas and formats.

The Readout Acquire DMA subtest is run unconditionally whenever either the Control Logic Diagnostic command (CL) or the Display Diagnostic command (DS) is invoked.

Once invoked, this subtest clears all memory from the 7854 RAM space reserved for acquisition of plug-in readout data (DF00-DF9E). The subtest then enables the DMA channel, pauses for 100ms (to allow the DMA channel to operate), then shuts off the DMA channel and reads the addresses from the 7854 RAM memory. If the addresses have been properly written, the terminal will print '01 RO ACQ DMA PASSED' and proceed to the next subtest or if failure occured print '01 RO ACQ DMA FAILED' then (1) proceed to the next subtest, (2) return to the diagnostic operating system, or (3) enter the troubleshooting routine as signaled to the operator through the message 'SCOPE LOOP #1', 'PRESS ANY KEY TO EXIT'.

The Set Parameters described earlier in this command description (CL) determine the above sequence.

Table 4-3
Control Logic Diagnostic Subtests

PRINTOUT WHEN INVOKED			REMARKS
NUMBER	DIAGNOSTIC TERMINAL	MICROLAB I	
01	RO ACQ DMA	A26-01	*Readout acquire DMA channel tests.
02	A-WORD LOAD	A26-02	Read/write test of A-word parallel load capability.
03	DSY DONE INT	A26-03	Display done interrupt generator test.
04	DIG CLOCK	A26-04	Digitizer clock generator scope loops.
05	DIG SWEEP CTR	A26-05	Digitizer sweep counter/acquire done interrupt circuits test.
06	DIG DMA CONTROL	A26-06	Digitizer DMA request generator test; control circuitry scope loop.
07	DIG ADDR GEN-INT	A26-06	Internal clock mode digitizer address generator test.
08	DIG ADDR GEN-EXT	A26-08	External clock mode digitizer address generator test.
09	AWRD INTERACTION	A26-09*	Display and control logic A-Word interaction test.
10	AWRD/BWRD INTERACTION	A26-10	*Display and control logic A-Word/B-Word interaction test.

*** Shared with Display command.**

Scope Loop

This scope loop enables the Readout Acquire DMA channel, then pauses to await a terminal keyboard interrupt. ('PRESS ANY KEY TO EXIT')

NOTE

All bus activity for this test is generated by the Readout Acquire DMA Channel only.

The DMA (Direct Memory Access) control circuitry (schematic 26) receives a stream of BRRO pulses (Bus-Request Readout) and, in response, generates a stream of DMA cycles with bus grant directed to the RO-ACQ DMA channel (eq. BGRO active).

The RO-ACQ DMA channel address generator on the A29-Display board (schematic 31) continously cycles through addresses 0DF00H through 0DF9EH while running this routine.

02—A-WORD LOAD

This diagnostic subtest verifies the parallel load and data readback functions of the A-Word Register on the A26-Control Logic board. It does not verify the counting function of the register.

The A-Word Load diagnostic subtest is run unconditionally whenever the Control Logic Diagnostic (CL) is invoked.

Once invoked, this subtest sets the A-Word register to 0000H and verifies that the A-Word register was cleared. Then each bit pattern beginning at 0002H is loaded, and read individually to insure data integrity. If all values from 0000H through 0FFFEH are successfully loaded and read back, the terminal will print '02 A-WORD LOAD PASSED' and proceed to the next subtest or, if failure occurred print '02 A-WORD LOAD FAILED' then (1) proceed to the next subtest, (2) return to the Diagnostic Operating System (TEK/DCL) or (3) enter the troubleshooting routine as signaled to the operator through the following message: 'SIG ANAL LOOP ENTERED' and 'PRESS [GO] KEY TO EXIT'. (The [GO] key is located on the MicroLab I front panel.) The Set parameters described earlier in this command description (CL) determine the above sequence.

The signature analysis loop is described by the following algorithm:

```
BEGIN
        GENERATE S/A START PULSE
        SET WDATA = 0000H
LOAD    COPY WDATA INTO A-WORD REGISTER
        COPY A-WORD REGISTER INTO RDATA
        INCREMENT WDATA BY 2
        IF WDATA NOT EQUAL TO ZERO THEN GO TO LOOP
        ELSE GENERATE S/A STOP PULSE
END
```

The sequence is repeated until the operator presses the GO key. Refer to the appropriate troubleshooting flowchart/signature tables located in Section 2.

03—DISPLAY DONE INTERRUPT GENERATOR

This diagnostic subtest verifies the functionality of the interrupt generator in all display points-per-waveform settings as well as in the forced interrupt mode (via the STPDSY CRU line).

The Display Done Interrupt subtest is run unconditionally, whenever the Control Logic Diagnostic (CL) is invoked.

Once invoked, this subtest performs two functions, (1) the subtest resets then pulses 'STPDSY' to force set the Display Done Interrupt and (2) initiates transitions on all bits of the A-Word register, then checks that an interrupt occurs in each of the four display points-per-waveform settings. (Shifting bit pattern 0001H through the A-Word Register).

If the Display Done Interrupt is received a total of 5 times (once in each of the 5 modes), the terminal will print '03 DSY INTERRUPT PASSED' and proceed to the next subtest or if failure occurred print '03 DSY INTERRUPT FAILED' and (1) proceed to the next subtest, (2) return to the diagnostic operating system (TEK-DCL) or (3) enter the troubleshooting routine as signaled to the operator through the following message 'SIG ANAL LOOP ENTERED' and 'PRESS [GO] KEY TO EXIT'.

The Set parameters described earlier in this command description (CL) determine the above sequence.

The signature analysis loop is described by the following algorithm:

```
BEGIN
        DISABLE ALL INTERRUPTS
        GENERATE SA START PULSE
        RESET DISPLAY DONE INTERRUPT FLIP FLOP
        PULSE 'STPDSY' TO FORCE SET
        DISPLAY DONE INTERRUPT FLIP FLOP
        RESET DISPLAY DONE INTERRUPT FLIP FLOP

        SET INITIAL DISPLAY-MODE WORD P/W SETTING
LOOP:   LOAD DISPLAY-MODE WORD WITH P/W SETTING
        SHIFT A SINGLE HIGH BIT THROUGH THE A-WORD
        REGISTER
        (causing transition on all A-Word bits)

        RESET DSY DONE INTERRUPT FLIP FLOP
        SET DISPLAY-MODE WORD TO NEXT P/W SETTING
        IF ALL P/W SETTINGS NOT DONE THEN GOTO 'LOOP'
        ELSE GENERATE SA STOP PULSE
END
```


@

The above sequence is repeated until the operator presses the [GO] key.

Refer to the appropriate troubleshooting flowchart/signature tables in Section 2.

04—DIGITIZER CLOCK

This diagnostic module is used for checking the digitizer burst clock generator on the A26-Control Logic board. The routines may also be used for verifying some 7854 Interface board circuitry since the operation of this module is affected by the A11-Main Interface board and the 7B87 timebase (Acquire Clock).

The Digitizer Clock subtest is run whenever the CL is invoked, providing the following conditions are met:

1. The timebase prompt '7B80 AND 7B87 INSTALLED? Y' must have been answered with 'Y' (for yes), and a 7B87 must be installed with controls set as shown in Table 4-2 to continue the Digitizer Clock test routine; otherwise the terminal will print the message: 04 DIG CLOCK SKIPPED.

2. The LB (Loop on Batch) set parameter must not have been selected.

NOTE

Set parameters are listed earlier in this command description.

Once invoked, this subtest generates six scope loops. The scope loops check the internal clock mode and the four resolution settings of the external clock mode consecutively. Refer to Table 4-4 for A26-Control Logic board register settings defined for the individual scope loops.

Individual scope loops run until a terminal key is pressed, at which time the next routine is run. After the sixth stimulation routine is exited, the Digitzer Clock subtest is complete and the Control Logic diagnostic proceeds to the next subtest.

Table 4-4
Acquire Word Register (U1820) Settings

SCOPE LOOP	MODEWORD	
	DISPLAY	ACQUIRE
1	0000H	0000H
2	0000H	1000H
3	0000H	1100H
4	0000H	1200H
5	0000H	1300H
6	0000H	2800H

05—DIGITIZER SWEEP COUNTER/ACQUIRE DONE INTERRUPT

This diagnostic module verifies the functionality of the digitizer sweep counter and acquire done interrupt request generator (diagram 25).

NOTE

All waveforms checked in subtest 04—Digitizer Clock must be correct before proceeding to this subtest.

This subtest checks for the ability of the sweep counter circuitry to detect and count a single sweep and may be used to verify some 7854 A11-Main Interface board circuitry since operation of this module is affected by the A11-Main Interface board and the 7B87 timebase.

The Digitizer Sweep Counter subtest is run whenever the CL is invoked, providing the following conditions are met: the timebase prompt '7B80 AND 7B87 INSTALLED? Y' must have been answered 'Y' (yes), and the 7B80 and 7B87 must be installed and setup as per Table 4-2, otherwise the test will be 'SKIPPED'.

If the above conditions were met, the diagnostic terminal prints the message:

REMOVE BRDIG JUMPER'
'PRESS ANY KEY TO CONTINUE'

Once invoked, this subtest presets and initializes the subject circuits and tests for the resultant interrupt for each of the following modes: A TIMEBASE INT CLOCK, B TIMEBASE INT CLOCK and B TIMEBASE EXT CLOCK. In each instance, the sweep counter is preset and the hardware initialized to count timebase sweeps in the appropriate mode. The subtest then delays to await an acquire-done interrupt.

A Timebase, Int Clock Subtest

The subtest first sets up the A26-Control Logic board to acquire a waveform using the A-Timebase in the internally generated digitizer clock mode. The digitizer sweep counter is preset to a value of one. The acquire function is enabled and the diagnostic pauses to wait for an acquire done interrupt. If the interrupt occurs, the routine continues to the next test phase. Otherwise, the test is considered FAILED and the remaining test phases are skipped.

B Timebase, Int Clock Subtest

In the second test phase, the routine sets up the A26-Control Logic board to acquire a waveform using the B-Timebase in the internally generated digitizer clock mode. The digitizer sweep counter is preset to a value of one. The acquire function is enabled and the routine pauses to wait for an acquire done interrupt. If the interrupt occurs, the routine continues on to the third test phase; otherwise, the test is considered FAILED and the final test phase is SKIPPED.

B Timebase, Ext Clock Subtest

In the third and final test phase, the routine sets up the A26-Control Logic board to acquire a waveform using the B-Timebase (7B87) in the external clock mode. The digitizer sweep counter is preset to a value of one and digitizer target memory is set to be the block of RAM from address 0C000H through 0C07FH. The acquire function is then enabled and the routine pauses to wait for an acquire done interrupt. If the interrupt occurs (and thus the interrupt has occurred in all modes of operation) the test is considered PASSED; otherwise the test is considered FAILED.

In all phases of the test the breakpoint mechanism of the 067-0911-XX 7854 Diagnostic Interface is used to confirm or deny the existence of the acquire done interrupt. If this subtest failed, one of the following messages will appear on the terminal:

05 DIG SWEEP CTR'
'A TIMEBASE, INT CLK FAILED'

indicates that no acquire done interrupts were received in A-Timebase, internal clock mode.

05 DIG SWEEP CTR'
'A TIMEBASE, INT CLK PASSED'
'B TIMEBASE, INT CLK FAILED'

indicates that no acquire done interrupts were received in B-Timebase, internal clock mode.

'05 DIG SWEEP CTR'
'A TIMEBASE, INT CLK PASSED'
'B TIMEBASE, INT CLK PASSED'
'B TIMEBASE, EXT CLK FAILED'

indicates that no acquire done interrupts were received in B-Timebase, external clock mode.

Depending on the state of the Set parameters, the Control Logic Diagnostic will report the failure as above and (1) proceed to the next subtest (2) return to the Diagnostic Operating System (TEK/DCL) (3) or enter the troubleshooting routine as signaled to the operator through the following messages: 'PRESS [GO] KEY TO EXIT' each scope loop, 'SCOPE LOOP #1 (#2, #3) A(B) TIMEBASE, INT (EXT) CLK.

The three scope loops exercise the digitizer sweep counter/acquire done interrupt circuitry in A-Timebase, internal clock mode (scope loop 1); B-Timebase, internal clock mode (scope loop 2) and B-Timebase, external clock mode (scope loop 3).

Table 4-5 shows the control logic register settings defining each of the 3 scope loops.

06—DIGITIZER DMA CONTROL

This diagnostic module verifies the functionality of the Digitizer DMA Control generator.

NOTE

For proper operation of this subtest, subtest 04-Digitizer Clock must have 'PASSED'.

This test will also aid checking interaction between the Control Logic and Digitizer board (sampler and A/D circuitry), and BRDIG channel of the 7854 DMA controller and timing generator circuitry.

This subtest is run whenever the Control Logic diagnostic command (CL) is invoked, provided the diagnostic terminal prompts are satisfied and the Set parameter LB (Loop on Batch) has not been selected. If any of the above conditions are not met the subtest will be 'SKIPPED' and the Control Logic diagnostic continues to the next subtest.

Table 4-5
Control Logic Register Settings for Acquire Done Interrupt Diagnostic

SCOPE LOOP #	MODEWORD			ADDRESS POINTER	
	*DISPLAY	**ACQUIRE	FRONT PANEL	AWRD	BWRD
1	0000H	27000H (Left Vert)	FF08H		
2	0000H	A700H (Left Vert)	FF01		
3	0007H	B700H (Left Vert)	FF01	C000	C000

* All display functions off
**Sweep count = 01

If the above conditions are met, the diagnostic terminal prints:

'REMOVE BRDIG JUMPER'
'PRESS ANY KEY FOR NEXT LOOP'

The operator must remove the jumper (if not done so in the previous subtest).

Once invoked, this subtest generates four scope loops. Each scope loop runs until a terminal key is pressed, at which time the next routine is run. As the fourth trouble-shooting loop is entered, the message: 'SCOPE LOOP #4' 'PRESS [AQS ABORT] TO EXIT' appears on the terminal. The subtest will remain locked in until the operator presses the AQS ABORT switch located on the rear panel of the 7854 Oscilloscope, at which time the terminal will proceed to the next subtest.

Table 4-6 shows the control logic register settings defining each of the 4 scope loops.

The first scope loop exercises the Digitizer DMA Control circuitry in internal clock mode with the DMA grant logic disabled.

NOTE

The 7854 Control Logic board under test will generate Digitizer DMA requests in internal clock mode but the requests will not be answered.

The Second Scope Loop exercises the Digitizer DMA Control circuitry in the External Clock Mode with the DMA grant logic disabled.

NOTE

The 7854 Control Logic board under test will generate Digitizer DMA requests in External Clock Mode but those requests will not be honored.

After completing Scope Loop #2, the Digitizer DMA Control Stimulation routines will print the messages:

'REPLACE BRDIG JUMPER'
'PRESS ANY KEY TO CONTINUE'

The third Scope Loop exercises the Digitizer DMA Control circuitry in Internal Clock Mode with the DMA grant logic enabled and full Digitizer DMA cycles progressing.

The fourth scope loop exercises the Digitizer DMA Control circuitry in External Clock Mode with the DMA grant logic enabled and full Digitizer DMA cycles progressing. This scope loop also checks the ability to abort ongoing externally clocked digitizing DMA cycles through use of the AQS ABORT pushbutton.

07—DIGITIZER ADDRESS GENERATOR—INTERNAL CLOCK MODE

This diagnostic module generates 5 stimulation loops to aid in verifying and troubleshooting the internal clock mode of the Digitizer Address Generator circuitry.

NOTE

For proper operation of this subtest, subtest 04—Digitizer Clock must have 'PASSED'.

Table 4-6
Control Logic Register Settings for Digitizer DMA Control Diagnostic

SCOPE LOOP #	MODEWORD		ADDRESS POINTER	
	*DISPLAY	**ACQUIRE	AWRD	BWRD
1	0000H	2000H (internal clock)		
2	0000H	3000H (external clock)		
3	0000H	A701H (internal clock) (B-timebase)	A000H	A000H
4	0000H	B701H (external clock) (B-timebase)	A000H	A000H

*** All display functions off**
****Acquire On.**

This subtest is run whenever the Control Logic diagnostic command CL is invoked, providing the diagnostic terminal prompts have been satisfied and the Set parameter LB (Loop on Batch) has not been selected.

If any of the above conditions have not been met the Digitizer Address Generator—Internal Clock Mode subtest will be 'SKIPPED'.

Once invoked, the subtest prints the message:

'PRESS ANY KEY FOR NEXT LOOP'
'SCOPE LOOP #1—INT CLK ONE WFM, 128 P/W'

then enters the first of 5 stimulation loops. Press any key to continue to the next loop.

Table 4-7 shows the Control Logic register settings which define the individual stimulation loops.

08—DIGITIZER ADDRESS GENERATOR—EXTERNAL CLOCK MODE

This diagnostic module generates 2 stimulation loops to aid in verifying and troubleshooting the external clock mode of the Digitizer Address Generator circuitry.

NOTE

For proper operation of this subtest (08), subtest 04—Digitizer Clock and 06—Digitizer DMA Controller must have 'PASSED'.

This subtest is run whenever the Control Logic diagnostic command CL is invoked, providing the diagnostic terminal prompts have been satisfied and the set parameter LB (Loop on Batch) has not been selected.

If any of the above conditions have not been met the Digitizer Address Generator—External Clock Mode subtest will be 'SKIPPED'. [08 DIG ADDR GEN—EXT SKIPPED].

Once invoked, the subtest prints the message:

'SCOPE LOOP #1—EXT CLK, ONE WFM, 1024 P/W'
'PRESS [AQS ABORT] TO EXIT'

This subtest will remain locked in until the operator presses the 'AQS ABORT' switch located on the rear panel of the 7854 oscilloscope, at which time the terminal will proceed to scope loop #2.

Table 4-8 shows the Control Logic register settings of the two scope loops.

09—A-WORD INTERACTION

This subtest checks interaction between the display circuits and the Control Logic A-Word Address Generator.

NOTE

For proper operation of this subtest (09), subtest 02 (A-Word Load) and 03 (Display Done Interrupt) must have passed.

Table 4-7
Control Logic Register Settings for
'Digitizer Address Generator—Internal Clock Mode' Diagnostic

SCOPE LOOP #	MODEWORD		ADDRESS POINTER		MODE (INT CLOCK)
	*DISPLAY	**ACQUIRE	AWRD	BWRD	
1	0000H	A701H	A800H	D000H	one wfm, 128P/W
2	0000H	A601H	A800H	D000H	one wfm, 256 P/W
3	0000H	A501H	A800H	D000H	one wfm, 512 P/W
4	0000H	A401H	A800H	D000H 024 P/W	one wfm,
5	0000H	AC01H	A800H	D000H	two wfms, 1024 P/W

*** All display functions off**
****Acquire on**

Table 4-8
Control Logic Register Settings for
'Digitizer Address Generator—External Clock Mode' Diagnostic

SCOPE LOOP #	MODEWORD		ADDRESS POINTER		MODE (EXT CLOCK)
	*DISPLAY	ACQUIRE	AWRD	BWRD	
1	0000H	B701H	A000H	B800H	128 P/W, one wfm
2	0000H	BF01H	A000H	A000H	128 P/W, two wfms

*** All display functions off**

This subtest is run whenever the Control Logic diagnostic command CL or Display diagnostic DS is invoked. The subtest does not require that timebases be installed in the mainframe.

Once invoked, this subtest initiates a stored waveform Y-T mode display cycle. The routine then checks for proper DMA cycles and address incrementing in all four points-per-waveform settings, then reports a PASS/FAIL message on the terminal.

The detailed description of the subtest follows:

1. The display board is reset and system interrupts are disabled. The start address for DMA target memory is set to be address OAOOOH while the stop address for display DMA target memory is initialized at OA7FFH, indicating a 1024 points-per-waveform display.

2. The 067-0911-XX breakpoint mechanism is set to trap on address OAOOOH, which is the first address in the display DMA target memory as defined for this cycle.

3. The A29-Display board and A26-Control Logic board modeword registers are set to perform a Y-T mode waveform display cycle with start-stop addresses and points-per-waveform resolution as set above. Breakpoint interrupts are enabled.

4. The display cycle is started and the diagnostic pauses for a set amount of time to allow the Y-T mode display cycle to occur.

5. The Display board circuitry is shut off and checks are made to determine whether a BKPT occurred during the last display cycle. A breakpoint would have occurred if, during the last display cycle, the A29-Display board/A26-Control Logic board DMA controller properly accessed the breakpoint target address. This SHOULD have happened so long as the BKPT target address is less than the current display stop address; it SHOULD NOT have happened if the BKPT target address is greater than the current display stop address. (if a BKPT did occur under these circumstances, it would indicate a points-per-waveform resolution error.)

6. The BKPT target address is incremented by a value of 09DH and the 067-0911-XX BKPT mechanism is set to trap on this new target address. Steps (3), (4), and (5) are repeated. This loop will continue until the BKPT target address becomes greater than the current stop address.

7. The current display stop address and points-per-waveform modeword preload are set to the next points-per-waveform value to be tested (512 P/W on the second pass, 256 P/W on the third pass, and 128 P/W on the fourth and final pass). The above test loop is repeated until all points-per-waveform modes are tested.

8. This test is considered PASSED if all conditions listed in step (5) are met on all passes through the test loop for all points-per-waveform settings. Otherwise, the test is considered FAILED.

If this subtest fails, one of the following messages will appear on the Diagnostic Terminal:

1. The message '09 AWRD INTERACTION FAILED—NO DMA OR—BAD DMA ADDRESS' indicates that no valid DMA cycles occurred when the display and control logic boards were started in a Y-T display cycle. This may be due to a failure of the Control Logic DMA controller/timing generator, the A29-Display board control logic, or a gross failure of the A26-Control Logic board A-Word register or Address Output buffers.

2. The message '09 AWRD INTERACTION FAILED—BAD DMA ADDRESS' indicates that at least one valid DMA cycle occurred in Y-T display mode but the most recent DMA cycle attempted was invalid. This is most likely due to a failure in the A-Word register incrementing logic.

3. The message '09 AWRD INTERACTION FAILED—P/W RESOLUTION ERROR' indicates that valid DMA

cycles have occurred, but the number of cycles detected and the target addresses for those DMA cycles are not appropriate for the P/W setting currently under test. For example, if the Display Modeword is set for a 512 point per waveform display, the 'P/W RESOLUTION ERROR' failure will occur if the 7854 under test attempts display DMA cycles from addresses greater than 512 words after the start address. This failure may be caused by a display modeword failure or an AWRD Register failure.

Depending on the Set parameters defined earlier in this command description the routine will (1) proceed to the next subtest (2) return to the diagnostic operating system (TEK/DCL or (3) enter the troubleshooting routine as signaled to the operator through the message:

'SCOPE LOOP #1 Y-T RAMP'
'PRESS ANY KEY TO EXIT'

The Control Logic and Display board register settings of the Y-T display cycles are as follows:

DISPLAY MODEWORD = 0804H	(Y-T MODE, DOTS, 1024 P/W)
ACQUIRE MODEWORD = 0000H	(all acquire functions off)
AWRD = preset to A000H	(indicates that memory A000H through A7FFH will be used as display data).

After the first display cycle, the scope loop pauses till either a real time clock interrupt (restarts the display board cycle) or a terminal keyboard interrupt (resets the Display and Control Logic boards then terminates the routine) is received.

NOTE

Use of the real time clock interrupt (rather than display done interrupt) insures that the display board will be periodically restarted, thus aiding troubleshooting of the Y-T display function.

10—A-WORD/B-WORD INTERACTION

This diagnostic subtest verifies (1) that the Display board is able to generate DMA requests and appropriate control signals for a single waveform X-Y display (2) the B-Word address register is capable of being selected, incremented, and gated onto the digitial system address bus to form a DMA address, and (3) the A-Word/B-Word multiplexer is functional.

This subtest is run unconditionally whenever either the Control Logic diagnostic CL or Display diagnostic DS is invoked.

The subtest does not require that timebases be installed in the mainframe.

The test proceeds automatically as follows (A-Word addresses are checked first):

1. The display board is set and system interrupts are disabled. The start address for DMA target memory is set up (address is OA000H for the A-Word test phase and OD800H for the B-Word test phase) while the stop address for the Display DMA target memory is set up for a 1024 P/W display cycle. (Address is OA7FFH for the A-Word test phase and ODFFFH for the B-Word test phase.)

2. The 067-011-XX breakpoint mechanism is set up to trap on the start address for display DMA target memory (OA000H or OD800H depending on the test phase).

3. The Control Logic and Display board modeword registers are set to perform an X-Y mode waveform display cycle with start/stop addresses and points-per-waveform resolution as set above. Breakpoint interrupts are enabled.

4. The display cycle is started and the diagnostic pauses for a set amount of time to allow the X-Y mode display cycle to occur.

5. The Display board circuitry is shut off and checks are made to determine whether a BKPT occurred during the last display cycle. A breakpoint would have occurred if, during the last display cycle, the Display board/Control Logic board DMA controller properly accessed the breakpoint target address. This SHOULD have happened so long as the BKPT target address is less than the current display stop address; it SHOULD NOT have happened if the BKPT target address is greater than the current display stop address. (If a BKPT did occur under these circumstances, it would indicate a points-per-waveform resolution error.)

6. The BKPT target address is incremented by a value of 09DH and the 067-0911-XX BKPT machanism is set to trap on this new target address. Steps (3), (4), and (5) are repeated. This loop will continue until the BKPT target address becomes greater than the current stop address.

7. The current display stop address and points-per-waveform modeword preload are set to the next points-per-waveform value to be tested (512 P/W on the second pass, 256 P/W on the third pass, and 128 P/W on the fourth pass). The above test loop is repeated until all points-per-waveform modes are tested.

8. The current test phase is considered PASSED if all conditions listed in step (5) are met on all passes through the test loop for all points-per-waveform settings. Otherwise, the test is considered FAILED.

9. After completing the above test sequence for A-Word register addresses, repeat the above for B-Word register addresses.

@

This subtest is considered 'PASSED' only if both test phases return passing results. Messages on the Diagnostic system terminal will appear as follows:

'10 AWRD/BWRD INTERACTION'
'A-WORD REGISTER ADDRESSES PASSED'
'B-WORD REGISTER ADDRESSES PASSED'

This subtest is considered FAILED if either test phase returns a failing result. If the subtest fails, one of the following messages will appear on the Diagnostic Terminal.

The message

'10 AWRD/BWRD INTERACTION
A-WORD REGISTER ADDRESSES FAILED-NO DMA OR-BAD DMA ADDRESS'

indicates that no valid DMA cycles occurred when the Control Logic and Display boards were started in an X-Y display cycle. This may be due to a failure of the Control Logic DMA Controller/Timing Generator, the Display board control logic, or a gross failure of the Control Logic board a-Word register or Address Output buffers.

The message

'10 AWRD/BWRD INTERACTION
A-WORD REGISTER ADDRESSES FAILED-
BAD DMA ADDRESS'

indicates that at least one valid DMA cycle occurred in X-Y display mode while checking A-Word addresses but the most recent DMA cycle attempted was invalid. This is most likely due to a failure in the address register incrementing logic.

The message

'10 AWRD/BWRD INTERACTION
A-WORD ADDRESSES FAILED-P/W RESOLUTION ERROR

indicates that valid DMA cycles have occurred, but the number of cycles detected and the target addresses for those cycles are not appropriate for the P/W setting currently under test. For example, if the display modeword is set for a 512 P/W display, the P/W RESOLUTION ERROR' failure will occur if the 7854 under test attempts display DMA cycles from addresses greater than 512 words after the start address. This failure may be caused by a Display modeword failure or an address register failure (AWRD or BWRD).

The message

'10 AWRD/BWRD INTERACTION
A-WORD REGISTER ADDRESSES PASSED
B-WORD REGISTER ADDRESSES FAILED-BAD DMA ADDRESS'

indicates that valid DMA cycles occurred for A-Word register addresses, but, while the test was checking B-Word register addresses, the most recent DMA cycle attempted was invalid. This may be due to an address register incrementing logic failure, or a failure in the A-Word/B-Word multiplexer.

The message

'10 AWRD/BWRD INTERACTION
A-WORD REGISTER ADDRESSES PASSED
B-WORD REGISTER ADDRESSES FAILED-P/W RESOLUTION ERROR'

indicates that a P/W resolution error was detected while checking B-Word register addresses.

Depending on the Set parameters described earlier in this command description (CL) the program will either conclude and return to the TEK/DCL operating system or enter the troubleshooting routine for the A-Word/B-Word interaction function (LE—Loop on Error).

Entry into the troubleshooting routine is signaled to the operator through the messages:

'SCOPE LOOP #1 X-Y RAMP'
'PRESS ANY KEY TO EXIT'

The scope loop consists of a continually repeated X-Y display cycle with memory data such that a fully functional 7854 would display a unit slope ramp on its crt screen while running the scope loop routine.

The Control Logic and Display board register settings which define this X-Y display cycle are as follows:

DISPLAY MODEWORD = 0825H	(X-Y mode, dots, 512 P/W)
ACQUIRE MODEWORD = OOOOH	(all acquire functions off)
A = preset to AOOOH	indicates that memory from A000H through A3FFH will be used as vertical display data.
BWRD = preset to DCOOH	indicates that memory from DC00H through DFFFH will be used as horizontal display data.

After the first display cycle, the scope loop pauses till either a real time clock interrupt (restarts the display board cycle) or a terminal keyboard interrupt (resets the Display and Control Logic boards then terminates the routine) is received.

NOTE

Use of the real time clock interrupt (rather than the display done interrupt) insures that the Display board will be restarted on a regular basis, thus facilitating troubleshooting of the X-Y display function.

Diagnostic Limitations

There is very close interaction between the Display Board and parts of the Control Logic Board. Because of this interaction, certain of the Control Logic subtests (those shared with the Display Board diagnostic routine) will test not only portions of the control Logic Board but also portions of the Display Board. In the event of subtest failure, it will not be obvious whether the failure was a Control Logic board failure or a Display Board failure. The troubleshooting procedures and stimulus routines for signature analysis or oscilloscope-based testing will enable the operator to determine which board is at fault and aid in isolating to the faulty component. The diagnostic routine alone will not be able to make the determination in such instances of interaction.

Control Logic Interface circuits (to the plug-ins) can be checked only indirectly. This testing requires the use of a known good 7B87 Time Base plug-in. This is dictated by the diagnostic strategy.

The DMA channel controller is only partially exercised by the current diagnostic version. For instance, the handling of simultaneous DMA requests is not checked.

Control Logic Diagnostic Exit Conditions

At the conclusion of Subtest 10 (A-Word/B-Word Interaction) or the troubleshooting routines associated with Subtest 10, the Control Logic Diagnostic is complete and it will prepare to return to the TEK/DCL Operating System. The following events will occur before the Operating System command prompt is received:

1. All Control Logic registers are returned to a reset state.

2. The Diagnostic Breakpoint mechanism is reset

3. The message—

   'DIAGNOSTIC COMPLETE'

is printed on the Diagnostic System Terminal.

If all the Subtests 01, 02, 03, 05, 09, and 10 reported a passing result, the message—

'A26-PASS'

appears on the MicroLab I front-panel display.

If any of Subtests 01, 02, 03, 05, 09, or 10 reported a failing result, the message—

'A26-FAIL'

appears on the MicroLab I front-panel display.

DG [DIGITIZER]

The Digitizer command allows invocation of a linked set of three subtests for checking the functionality, monotonicity, linearity and accuracy of the A/D circuitry of the 7854. It provides direct verification of functionality of the Digitizer DMA channel (A25-Digitizer and A26-Control Logic boards) and indirect verification of functionality of the display DMA channel (A26-Control Logic and A29-Display boards). The waveform digitizing circuitry resides primarily on the A25-Digitizer, A11-Main Interface, A19-Vertical Channel Switch and A26-Control Logic Boards.

NOTE

The Horizontal and Triggering subsystem may also affect the results of these subtests.

To invoke the Digitizer diagnostic, type DG [subtest no.] [accuracy limits] <CR>

[Subtest no.] The subtest specified will be the first test run followed automatically by the remaining subtests. Subtest 04 will be run only if called by the operator (not run automatically).

[Accuracy Limits] The operator may select either high [HI] or low [LO] accuracy limits.

The accuracy parameter allows the operator selection of PASS/FAIL limits. These limits are defined as follows:

limits (PASS)—The digitized value must be within 1% of desired value with no more than ten (10) bad points.

LO limits (PASS)—The digitized value must be within 1/2 division of desired value with no more than 100 bad points.

NOTE

If no parameters are selected, the routine begins running subtest 01 at the HI accuracy limit.

The subtests defined for the digitizer diagnostics circuits package are listed in Table 4-9 and defined functionally in the paragraphs that follow.

SET PARAMETERS

The external set Parameters for this diagnostic are as follows:

NOTE

For invocation of Set Parameters, refer to Set Parameter invocation procedure at the beginning of this section.

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HE (HALT on ERROR)—Upon error detection, the diagnostic terminal prints the appropriate error message then returns to the Diagnostic Operating System. The operator may restart the diagnostic at the point of failure by typing "GO <CR>" on the diagnostic terminal.

LE (LOOP on ERROR)—Upon error detection, the diagnostic terminal prints the appropriate error message then enters a stimulation routine for troubleshooting or calibrating.

LP (LOOP on PASS)—The diagnostic will enter its associated stimulation routine if the subtest does not detect error(s) in its fault detection mode of operation.

01—DIGITIZER ZERO VALUE SUBTEST

This diagnostic subtest checks the response (to a zero input) of the waveform acquisition signal path circuitry and the Digitizer board A/D circuitry. The zero input consists of equal voltages applied to the differential signal inputs of the vertical plug-in interface connector.

Table 4-9
Digitizer Diagnostic Subtests

Number	Mnemonic	Function
01	DIG ZERO VALUE	Checks zero level output of digitizer when acquiring a zero input COMM MODE signal from an 067-0587-0X Signal Standardizer plug-in.
02	DIG DC GAIN	Checks dc output levels of digitizer when acquiring a staircase waveform as generated by an 067-0587-0X Signal Standardizer plug-in.
03	DIG LINEARITY	Checks for monotonicity and linearity of the digitizer output when acquiring a ramp waveform as generated by a 7B92A plug-in (or equivalent) installed in a vertical plug-in compartment.
04	DIG TROUBLESOOTING	Causes a continuous acquire cycle to aid test/calibration of the vertical/horizontal pickoff channels, the vertical/horizontal samplers, and the digitizer. This subtest is not called in the default mode of operation for the Digitizer Diagnostic—it is called only through the invocation line "DG 04".

The digitizer zero value subtest is run whenever DG <CR> is invoked, providing the following conditions as stated in the Diagnostic Terminal prompt are met: (1) The plug-ins are set as per Table 4-10 and (2) the prompt SETUP PLUG-INS—PRESS 'C' TO CONTINUE, 'S' TO SKIP is answered 'C' and subtest 02, 03 or 04 was not chosen.

Once invoked, the subtest will run a 5 second acquire cycle to acquire and process data. After completion of the acquire cycle, statistics on the acquired point values are compiled and printed in hexadecimal notation. A total of 03C0 (hexadecimal) points are checked. A description of each statistic is provided as follows:

DESIRED:	0000	Indicates that the desired value for digitized points was 0000.
LIMITS:	MAX	Indicates the upper limit of acceptable values.
	MIN	Indicates the lower limits of acceptable values.
PTS OK		Indicates the number of points within the MAX and MIN limit value.
PTS HIGH		Indicates the number of points above the maximum limit value.
PTS LOW		Indicates the number of points below the minimum limit.
PTS NOT DIGITIZED		Indicates the number of points that were not digitized.

If the statistics are within accuracy limits set earlier, the diagnostic terminal prints '01 DIG ZERO VALUE PASSED'. If not within accuracy limits the terminal prints '01 DIG ZERO VALUE FAILED', and (1) proceeds to the next subtest, (2) returns to the Diagnostic Operating System, or (3) enters one of two stimulation routines. If the LE—Loop on Error option has been entered, the message 'TROUBLESHOOTING ('T') OR CAL ('C') LOOP? will appear on the diagnostic terminal.

Press 'T' and the routine shifts immediately to subtest 04—Digitizer troubleshooting Loop. Press 'C' and the subtest will be repeated for observing the affect of associated adjustments (Position, Offset).

If the user answers the prompt with a letter other than 'T' or 'C' the subtest will be terminated and the digitizer diagnostic will proceed to the next subtest.

02—DIGITIZER DC GAIN SUBTEST

This diagnostic subtest checks the response (to a staircase pattern input signal) of the waveform acquisition signal path circuitry and the digitizer board A/D circuitry.

Table 4-10
Digitizer Test Equipment
Setup Conditions

Subtest #	Mainframe Plug-In Compartment	Instrument	Control		Remarks
			Name	Setting	
01	LEFT VERT	067-0587-01,02 Signal Standardizer	Test Rep Rate	Trigger Gain Don't Care	
	RIGHT VERT	7B92A Timebase		Don't Care	
	B-HORIZ	7B87 Timebase	Time/div Triggering HOLDOFF Acquire Stop Delay	20 μs P-P AUTO, AC, INT Stable Display(Adjust) minimum	
02	LEFT VERT	067-0587-01,02 Signal Standardizer	Test Rep Rate	Vertical Gain 100 KHz	Position for zero line value at left edge of crt screen. extending at least 1 div, toward horiz. center screen. (Waveform need not cover entire screen).
	RIGHT VERT	7B92A Timebase			
	B-HORIZ	7B87 Timebase	Time/div Triggering HOLDOFF Acquire Stop Delay	20 μs P-P AUTO, AC, INT *STABLE Staircase Display minimum	*The condition of the trigg-ering and holdoff circuity of the 7B87 timebase is critical for a useable, meaningful display.
03	LEFT VERT	067-0587-01,02 Signal Standardizer	Test Rep Rate	Vertical Gain 100 KHz	**B trigger source connected to Left Vert 'trig out'.
	RIGHT VERT	7B92 Timebase	Time/div Triggering	20 μs EXT	Position the trace to pass through outer screen with nonlinear segments fully offscreen.
	B-HORIZ	7B87 Timebase	Time/div Triggering** HOLDOFF Acquire Stop Delay	20 μs P-P AUTO, AC, INT Stable Display(Adjust) minimum	+GATE OUT(7854 rear panel) to 7B92 EXT trig input.
04	LEFT VERT	067-0587-01,02	Same as 'failed' test conditions		

The Digitizer DC Gain subtest is run unconditionally when 'DG 02' <CR> is invoked, providing the following conditions as stated in the diagnostic terminal prompt are met: (1) the plug-ins are installed and set as per Table 4-10, and (2) the prompt 'SETUP PLUGINS—PRESS 'C' TO CONTINUE, 'S' TO SKIP' is answered 'C'.

Once invoked, the subtest will run a 5 second acquire cycle then print out statistics—'DESIRED, LIMITS, PTS OK, PTS HIGH, PTS LOW, PTS NOT DIGITIZED' for each step of the staircase waveform.

A description of each statistic is provided as follows:

DESIRED: Indicates the calculated desired value for the current step.

LIMITS: MAX Indicates the upper limit of acceptable values.

MIN Indicates the lower limit of acceptable values.

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PTS OK	Indicates the number of points within the MIN and MAX value limits. (The maximum number of points checked for each step is 0028 hexadecimal points)
PTS HIGH	Indicates the number of points above the maximum limit value.
PTS LOW	Indicates the number of points below the maximum limit value.

NOTE

All point counts are listed in hexadecimal notations.

After displaying statistics on all steps, the diagnostic will print the total number of points checked and found not digitized as follows:

PTS NOT DIGITIZED....

If the statistics are within the accuracy limits set earlier, the diagnostic terminal prints '02 DIG DC GAIN PASSED' and continues to the next subtest or prints (if the statistics are not within limits) '02 DIG DC GAIN FAILED', and (1) proceeds to the next subtest, (2) returns to the Diagnostic Operating System (TEK,DCL); or (3) enters one of two stimulation routines; Troubleshooting or Calibration.

If the 'LE' option has been entered, the message 'TROUBLESHOOTING ('T') or CAL ('C') LOOP? will appear on the diagnostic terminal. Press 'T' and the routine shifts immediately to the Digitizer Troubleshooting Loop—Subtest 04. Press 'C' and the subtest will be repeated for calibrating associated circuitry.

03—DIGITIZER LINEARITY SUBTEST

This diagnostic subtest checks the response (to a unit slope ramp input signal) of the waveform acquisition signal path circuitry and the Digitizer board A/D circuitry.

The Digitizer Linearity subtest is run whenever 'DG 03' <CR> is input on the diagnostic terminal, providing the following conditions are met:

1. The plug in units are installed and set as per Table 4-10 and,
2. The prompt 'SETUP PLUGINS—PRESS 'C' TO CONTINUE, 'S' TO SKIP' is answered 'C'.

Once invoked, the subtest runs a 5 second acquire cycle. On completion of the acquire cycle, the routine will analyze the acquired data and compile statistics on the point count/distribution. If the acquired data was not recognizable as a ramp, the error message 'NO CENTER SCREEN POINT FOUND' '03 DIG LINEARITY FAILED' will be printed on the diagnostic terminal.

If the data was recognizable the diagnostic prints 2 sets of figures—one set for points above and one set for points below center screen as follows: (Refer to subtest 02 for a description of the following statistics.

1. ABOVE CENTER SCREEN VALUE OF:
   PTS OK.... PTS HIGH.... PTS LOW....
   HIGH END POINT VALUE:
   DESIRED.... LIMITS: MAX.... MIN....

2. BELOW CENTER SCREEN VALUE OF:
   PTS OK.... PTS HIGH.... PTS LOW....
   LOW END POINT VALUE:
   DESIRED.... LIMITS: MAX.... MIN....

After printing the preceeding statistics, the digitizer diagnostic then prints the message:

'LINEARITY ERROR PLOT ON 7854 CRT SCREEN'
'PRESS 'E' TO EXPAND, 'S' TO STOP DISPLAY'

At the same time, the 7854 under test displays a plot consisting of the point-by-point differences between the acquired ramp and the 'perfect' ramp constructed about the center screen value. For examination of small differences press 'E' to expand the display vertically by a factor of 2. This display will continue until the operator presses "S".

If the number of bad points (high, low, not digitized) is above the specified limits, the diagnostic will print—'03 DIG LINEARITY FAILED' and depending on the state of the Set Parameters will, (1) conclude the diagnostic, (2) return to the diagnostic operating system after having saved the state of the system at the time the failure was determined (HE—Halt on Error option), or (3) enters one of two stimulation loops. If the LE—Loop on Error option has been entered, the message 'TROUBLESHOOTING ('T') OR CAL ('C') LOOP?' will appear on the diagnostic terminal.

Press 'T'—the routine shifts to subtest 04—Digitizer Troubleshooting Loop.

Press 'C'—the subtest will be repeated and another pass/fail decision printed.

NOTE

If the user answers the prompt with the letter other than 'T' or 'C' the subtest will be terminated.

04—DIGITIZER TROUBLESHOOTING LOOP

This subtest allows observation and/or troubleshooting the waveform digitizing signal path and A/D circuitry of the 7854.

This subtest is run under either of two conditions:

1. 'DG 04' <CR> is entered on the diagnostic terminal, or

2. The operator has initially selected the 'LE' option, and subtest (01, 02, 03) fails, and the operator presses 'T' (troubleshooting loop) on the diagnostic terminal.

Once invoked, this subtest performs a continuous acquire operation in the same plug-in mode as the failed test (refer to Table 4-10 for plug-in conditions). Entry is signaled by the message: 'PRESS ANY KEY TO EXIT.' During the acquisition cycle, both realtime and acquired data will be displayed on the 7854 under test. When the operator presses a key on the diagnostic terminal, the acquire cycle is terminated, the crt blanked, and the subtest exited.

DS [DISPLAY]

The Display command allows the invocation of a complete set of diagnostic, troubleshooting, and fault isolation routines for the 7854 Oscilloscope display circuits. The command consists of a linked set of subtests that may be called in a predefined sequence.

The Display diagnostic can be invoked by either of two methods.

1. Type DS <CR> on the diagnostic terminal to run all ten (10) subtests consecutively, beginning with subtest 01.

2. Type DS [subtest number] <CR> to skip any number of consecutive subtests beginning with subtest 01.

   For example, type 03 for [subtest number] and the Display diagnostic begins the routine at subtest 03 (skipping subtests 01 and 02) and continues through subtest 10.

NOTE

Certain display circuit subtests are shared with the Control Logic command and the Real Time Clock Command. Those subtests are identified in the subtest descriptions.

The Display Diagnostic routine requires functionality of the 7854 Oscilloscope MPU board (A27) and RAM board (A28).

The subtests defined for the display circuits diagnostic package are listed in Table 4-11 and defined functionally in the paragraphs that follow.

SET PARAMETERS

The external Set Parameters for the Display Diagnostic are defined as follows:

NOTE

For invocation of Set Parameters, refer to Set Parameter invocation procedure at the beginning of this section.

HE (Halt on Error)—If the HE option is selected when an error is detected in a subtest, the subtest reports an error message on the terminal screen and returns to the TEK-DCL operating system. This procedure will, under most circumstances, allow the diagnostic routine to be restarted by entering GO <CR> at the terminal keyboard.

LE (Loop on Error)—If the LE option is selected when an error is detected in a subtest, the subtest reports an error message on the terminal screen, then enters the troubleshooting loop defined for that subtest. The HE option will override the LE option.

LP (Loop on Pass)—If the LP option is selected, the subtest enters its associated signature analysis or scope loop if the subtest can detect no errors in its fault detection mode of operation.

DI (Disable Error Messages)—This option is not implemented.

LB (Loop on Batch)—If the LB option is selected, the Display command routine continuously runs Subtests 01 through 06 until halted by the operator pressing the reset or ESC key or, if applicable, the HE, LE, or LP parameter options are invoked. Subtests 07 through 10 are unconditionally skipped.

01—REAL TIME CLOCK SUBTEST

This subtest verifies that the Display Board real time clock circuits operate within specified accuracy limits.

The Real Time Clock Subtest is run unconditionally when either the Display DS or Timer TI diagnostic is invoked.

Once invoked, this subtest enables the Real Time Clock then pauses for 100 msec to verify the presence of a clock interrupt (within the 100 msec period). If no clock interrupts were received during the 100 msec period the diagnostic terminal prints:

'01 RT CLOCK FAILED—CLOCK MISSING'

If a clock interrupt is received within the 100 msec period the diagnostic begins timing a 12 msec period. If an interrupt occurred during the 12 msec period the diagnostic terminal prints:

'01 RT CLOCK FAILED—CLOCK FAST'

Table 4-11
Display Circuits Diagnostic Subtests

PRINTOUT WHEN INVOKED			
NUMBER	DIAGNOSTIC TERMINAL	MICROLAB I	DESCRIPTION
01	RT CLOCK	A29-01	*Real time clock test.
02	RO ACQ DMA	A29-02	**Readout acquire DMA channel test.
03	Y-T: AWRD INTERACTION	A29-03	Display and Control Logic A-word interaction test.
04	X-Y: AWRD/ BWRD INTER-ACTION	A29-04	*Display and Control Logic A-word and B-word interaction tests.
05	CURSORS DSY CYCLE	A29-05	Cursors display cycle test.
06	CHARACTERS DSY CYCLE	A29-06	Character Display cycle tests in both burst mode and 8-KHz mode.
07	Y-T DISPLAY	A29-07	Continuous Y-T display test. (A stimulation loop that forces continuous display and allows checking of display DAC's and analog signal paths from the display board to the crt.)
08	X-Y DISPLAY	A29-08	X-Y graticule pattern display test. (Similar to Subtest 07 except that the display is of an X-Y graticule pattern with the center dot intensified.)
09	CURSORS DISPLAY/ VECTOR GEN	A29-09	Cursors pattern display test. (Similar to Subtest 7 except that the display is of two cursors patterns and is intended for vector generator circuitry test and troubleshooting.)
10	CHARACTERS	A29-10	Character set display test. (Similar to subtest 7 except that display is of character set in both burst mode and 8KHz mode.)

*** Shared with Control Logic command.**
****Shared with Real Time Clock command.**

Otherwise, the diagnostic will time an additional 8 msec period and again check for a clock interrupt. If a clock interrupt did not occur, the diagnostic terminal prints:

'01 RT CLOCK FAILED—CLOCK SLOW'

This subtest PASSED if the clock interrupt is received between 12 msec and 20 msec after the initial clock interrupt.

If this subtest fails, the diagnostic routine will (1) proceed to the next subtest, (2) return to the diagnostic operating system (TEK-DCL), or (3) enter the troubleshooting routine as signaled to the operator through the message:

'SCOPE LOOP #1'
'PRESS [GO] KEY TO EXIT'

The function of this scope loop is to enable and disable the real time clock circuitry and reset the RT Clock Interrupt flip-flop using a 20 msec period.

02—READOUT ACQUIRE DMA SUBTEST

This subtest verifies that the readout acquire DMA channel is operational.

The Readout Acquire DMA subtest is run unconditionally whenever either the Display DS or Control Logic CL diagnostic is invoked.

It does not require timebases be installed in the mainframe under test.

Once invoked, the Readout Acquire DMA subtest first clears (set to 0000H) all memory between addresses 0DF00H and 0DF9EH, which is the area in 7854 RAM space reserved for acquisition of plugin readout data. The test then enables the Readout Acquire DMA channel by setting CRU line address 0017H high. After pausing for 100 msec to allow the DMA channel to operate, the test then shuts off the DMA channel (by setting CRU line 0017H low) and reads 7854 RAM from address 0DF00H through 0DF9EH. If all of the address words in that range are now of the form 0FFXXH (XX is "don't care"), they were properly written by the Readout Acquire DMA channel and the test is considered PASSED. The diagnostic will then proceed to the next subtest. Otherwise, if not all addresses in the appropriate RAM area were properly written, the test is considered FAILED.

NOTE

This test checks only for the existence of correct memory cycles as generated by the Readout Acquire DMA channel. It does not check for correctness of the data written by those DMA cycles.

While this test is running, the Display DMA channel and the Digitizer DMA channel are both disabled. Therefore, the DMA timing generators and prioritizers are not checked for performance when simultaneous DMA requests are received.

If this subtest fails, the diagnostic terminal prints:

'02 RO ACQ DMA FAILED—NO DMA OR—BAD DMA ADDRESS'

then, depending on the Set Parameters selected earlier, (1) continues on to the next subtest, (2) return to the diagnostic operating system (TEK-DCL) or (3) enter the troubleshooting routine for the RO ACQ DMA channel whose entry is signaled to the operator through the messages:

'SCOPE LOOP #1'
'PRESS ANY KEY TO EXIT'

This scope loop enables the RO ACQ DMA channel and then pauses awaiting a terminal keyboard interrupt.

Once invoked, the DMA control circuitry on the Control Logic board (diagram 26 of 7854 schematics) receives a stream of BRRO pulses (Bus-Request, Readout) and, in response, generates a stream of DMA cycles with bus grant directed to the RO-ACQ DMA channel (e.g. BGRO active). Additionally the RO-ACQ DMA channel address generator on the Display board (diagram 31 of 7854 schematics) continually cycles through the addresses 0DF00H through 0DF9EH while running this routine.

03—A-WORD INTERACTION SUBTEST

The A-Word Interaction subtest checks the ability of the 7854 to perform DMA cycles in Y-T display mode for each of the four points-per-waveform settings, (1028, 512, 256, 128)

This subtest is run unconditionally whenever the Display DS or Control Logic CL diagnostic is invoked.

NOTE

Both the Control Logic subtest 02 (A-Word Load) and subtest 03 (Display Done Interrupt must have passed for this subtest to provide a valid result.

Once invoked, this subtest:

1. Resets the display board and disables the system interrupts. The start address for DMA target memory is set to be address 0A000H while the stop address for display DMA target memory is initialized at 0A7FFH, indicating a 1024 points-per-waveform display.

2. The 067-0911-XX breakpoint mechanism is set to trap on address 0A000H, which is the first address in the display DMA target memory as defined for this cycle.

3. The Display board and Control Logic board modeword registers are set to perform a Y-T mode waveform display cycle with start-stop addresses and points-per-waveform resolution as set above. Breakpoint interrupts are enabled.

4. The Display cycle is started and the diagnostic pauses for a set amount of time to allow the Y-T mode display cycle to occur.

5. The Display board is shut off and checks are made to determine whether a BKPT occurred during the last display cycle. A breakpoint would have occurred if, during the last display cycle, the Display board/Control Logic board DMA controller properly accessed the breakpoint target address. This SHOULD have happened so long as the BKPT target address is less than the current display stop address; it SHOULD NOT have happened if the BKPT target address is greater than the current display stop address. (If a BKPT did occur under these

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circumstances, it would indicate a points-per-waveform resolution error.)

6. The BKPT target address is incremented by a value of 09DH and the 067-0911-XX BKPT mechanism is set to trap on this new target address. Steps (3), (4), and (5) are repeated. This loop will continue until the BKPT target address becomes greater than the current stop address.

7. The current display stop address and points-per-waveform modeword preload are set to the next points-per-waveform value to be tested (512 P/W on the second pass, 256 P/W on the third pass, and 128 PW on the fourth and final pass). The above test loop is repeated until all points-per-waveform modes are tested.

This test is considered PASSED if all conditions listed in step (5) are met on all passes through the test loop for all points-per-waveform settings.

The diagnostic terminal prints the message:

'03 Y-T: AWRD INTERACTION PASSED'

then proceeds to the next subtest.

If this subtest failed (not all conditions in step 5 were met) the diagnostic terminal prints the appropriate message:

'03 Y-T: AWRD INTERACTION FAILED—NO DMA OR—BAD DMA ADDRESS'

indicating that no valid DMA cycles occurred when the display and control logic boards were started in a Y-T display cycle. This may be due to a failure of the Control Logic DMA controller/timing generator, the Display board control logic, or a gross failure of the Control Logic board a-word register or Address Output buffers.

'03 Y-T:AWRD INTERACTION FAILED—BAD DMA ADDRESS'

indicates that at least one valid DMA cycle occurred in Y-T display mode but the most recent DMA cycle attempted was invalid. This is most likely due to a failure in the a-word register incrementing logic.

"03 Y-T AWRD INTERACTION FAILED—P/W RESOLUTION ERROR'

indicating that valid DMA cycles have occured, but the number of cycles detected and the target addresses for those DMA cycles are not appropriate for the PW setting currently under test. For example, if the display modeword is set for a 512 point per waveform display, the "P/W RESOLUTION ERROR' failure will occur if the 7854 under test attempts display DMA cycles from addresses greater than 512 words after the start address. This failure may be caused by a display modeword failure or an AWRD Register failure.

The Set Parameters selected earlier will determine whether the diagnostic (1) continues to the next subtest, (2) returns to the diagnostic operating system (TEK-DCL), or (3) enters the troubleshooting routine as signaled to the operator through the following messages:

'SCOPE LOOP #1 Y-T RAMP'
'PRESS ANY KEY TO EXIT'

The scope loop consists of a continously repeated Y-T display cycle with memory data such that a fully functional 7854 would display a unit slope ramp on its crt screen while running this scope loop routine.

The Control Logic and Display board register settings which define this Y-T display cycle are as follows:

DISPLAY MODEWORD = 0804H	(Y-T mode, dots, 1024 P/W.)
ACQUIRE MODEWORD = 0000H	(all acquire functions off.)
AWRD = preset to A000H	indicates that memory from A000H through A7FFH will be used as display data.

After the first display cycle, the scope loop pauses till either a real time clock interrupt (restarts the display board cycle) or a terminal keyboard interrupt (resets the Display and Control Logic board then terminates. the routine) is received. Use of the RT clock interrupt insures that the display board will be periodically restarted in order to aid troubleshooting of display faults.

04—A-WORD/B-WORD INTERACTION SUBTEST

The A-Word/B-Word Interaction subtest checks the ability of the 7854 to perform DMA cycles in X-Y display mode for each of the four points-per-waveform settings (1028, 512, 256, 128)

This subtest is run unconditionally whenever the Display DS or Control Logic CL diagnostic is invoked.

NOTE

Both the Control Logic subtest 02 (A-Word Load) and subtest 03 (Display Done Interrupt) must have passed for this subtest to provide a valid result.

Once invoked, this subtest:

1. Resets the display board and disables the system interrupts. The start address for DMA target memory is set up (address is 0A000H for the a-Word test phase and 0D800H for the B-Word test phase) while the stop address for the Display DMA target memory

is set up for a 1024 P/W display cycle. (Address is 0A7FFH for the A-Word test phase and 0DFFFH for the B-Word test phase.)

2. The 067-0911-XX breakpoint mechanism is set up to trap on the start address for display DMA target memory (0A000H or 0D800H depending on the test phase).

3. The Control Logic and Display board modeword registers are set to perform an X-Y mode waveform display cycle with start/stop addresses and points-per-waveform resolution as set above. Breakpoint interrupts are enabled.

4. The display cycle is started and the diagnostic pauses for a set amount of time to allow the X-Y mode display cycle to occur.

5. The Display board is shut off and checks are made to determine whether a BKPT occurred during the last display cycle. A breakpont would have occurred if, during the last display cycle, the Display board/Control Logic board DMA controller properly accessed the breakpoint target address. This SHOULD have happened so long as the BKPT target address is less than the current display stop address; it SHOULD NOT have happened if the BKPT target address is greater than the current display stop address. (If a BKPT did occur under these circumstances, it would indicate a points-per-waveform resolution error.)

6. The BKPT target address is incremented by a value of 09DH and the 067-0911-XX BKPT mechanism is set to trap on this new target address. Steps (3), (4), and (5) are repeated. This loop will continue until the BKPT target address becomes greater than the current stop address.

7. The current display stop address and points-per-waveform modeword preload are set to the next points-per-waveform value to be tested (512 p/w on the second pass, 256 p/w on the third pass, and 128 p/w on the fourth pass). The above test loop is repeated until all points-per-waveform modes are tested.

After completing the above test sequence for A-Word register addresses, repeat the above for B-Word register addresses.

The current test phase is considered PASSED if all conditions listed in step (5) are met on all passes through the test loop for all points-per-waveform settings.

The diagnostic terminal then prints the message:

'04 X-Y; AWRD/BWRD INTERACTION'
'A-WORD REGISTER ADDRESSES PASSED'
'B-WORD REGISTER ADDRESSES PASSED'

and proceeds to the next subtest.

If this subtest failed (not all conditions in step 5 were met for both A and B-Word registers) the diagnostic terminal prints the appropriate message:

'04 X-Y: AWRD/BWRD INTERACTION
A-WORD REGISTER ADDRESSES FAILED—NO DMA OR—BAD DMA ADDRESS'

The above message indicates that no valid DMA cycles occurred when the Control Logic and Display boards were started in an X-Y display cycle. This may be due to a failure of the Control Logic DMA Controller/Timing Generator, The Display board control logic, or a gross failure of the Control Logic board A-Word register or Address Output buffers.

'04 X-Y: AWRD/BWRD INTERACTION
A-WORD REGISTER ADDRESSES FAILED—BAD DMA ADDRESS'

Indicates that at least one valid DMA cycle occurred in X-Y display mode while checking A-Word addresses but the most recent DMA cycle attempted was invalid. This is most likely due to a failure in the address register incrementing logic.

'04 X-Y: AWRD/BWRD INTERACTION
A-WORD ADDRESSES FAILED—P/W RESOLUTION ERROR'

Indicates that valid DMA cycles have occurred, but the number of cycles detected and the target addresses for those cycles are not appropriate for the P/W setting currently under test. For example, if the display modeword is set for a 512 P/W display, the P/W RESOLUTION ERROR' failure will occur if the 7854 under test attempts display DMA cycles from addresses greater than 512 words after the start address. This failure may be caused by a Display modeword failure or an address register failure (AWRD or BWRD).

'04 X-Y: AWRD/BWRD INTERACTION
A-WORD REGISTER ADDRESSES PASSED
B-WORD REGISTER ADDRESSES FAILED—BAD DMA ADDRESS'

Indicates that valid DMA cycles occurred for A-Word register addresses, but, while the test was checking B-Word register addresses, the most recent DMA cycle attempted was invalid. This may be due to an address register incrementing logic failure, or a failure in the A-Word/B-Word multiplexor.

'04 X-Y: AWRD/BWRD INTERACTION
A-WORD REGISTER ADDRESSES PASSED
B-WORD REGISTER ADDRESSES FAILED—P/W RESOLUTION ERROR'

indicates that a P/W resolution error was detected while checking B-Word register addresses. See above for further information.

The Set Parameters selected earlier will determine whether the diagnostic, (1) continues to the next subtest, (2) returns to the diagnostic operating system (TEK-DCL), or (3) enters the troubleshooting routine as signaled to the operator through the following messages:

'SCOPE LOOP #1 X-Y RAMP'
'PRESS ANY KEY TO EXIT'

The scope loop consists of a continually repeated X-Y display cycle with memory data such that a fully functional 7854 would display a unit slope ramp on its crt screen while running the scope loop routine.

The Control Logic and Display board register settings which define this X-Y display cycle are as follows:

DISPLAY MODEWORD = 0825H	(X-Y mode, dots, 512 p/W.)
ACQUIRE MODEWORD = 0000H	(All acquire functions off.)
AWRD = preset to A000H	Indicates that memory from A000H through A7FFH will be used as vertical display data.
BWRD = preset to D800H	Indicates that memory from D800H through DFFFH will be used as horizontal display data.

After the first display cycle, the Scope Loop pauses till either a real time clock interrupt (restarts the display board cycle) or a terminal keyboard interrupt (resets the Display and Control Logic board then terminates the routine) is received. Use of the RT Clock Interrupt insures that the Display board is periodically restarted, to aid troubleshooting the Display function.

05—CURSORS DISPLAY CYCLE SUBTEST

The Cursors Display Cycle subtest verifies that the Display board circuits interact properly with the Control Logic board circuits to generate repetitious DMA cycles and data transfers for the cursor display function.

This subtest is run unconditionally whenever the Display DS diagnostic is invoked.

NOTE

Subtest 04 (X-Y: AWRD/BWRD INTERACTION) must have passed for this subtest to provide valid results.

1. Once invoked, this subtest resets the Display board circuitry and disables the interrupts. The breakpoint mechanism of the 067-0911-XX is set to trap on address 0A000H, the first address of the memory block used for vertical cursor data.
2. The Display board circuitry is then set to perform cursor display cycles with vertical data beginning at address 0A000H and horizontal data beginning at address 0D800H (ie, A-Word is preset to 0A000H and B-Word is preset to 0B800H, Display modeword is preset to 0824H)
3. The display cycle is started and the diagnostic pauses allowing cursor display cycles to occur.
4. After the delay, the diagnostic re-enables the interrupts so that, if a breakpoint interrupt is pending, it will be allowed to occur. A breakpoint will occur only if the target address was properly accessed by the Display board circuitry while performing the cursors display DMA cycles. If, after the delay, a breakpoint does not occur, the target address was not properly accessed, implying that a DMA cycle did not occur properly. In this case, the test is considered FAILED.
5. If the current target address was properly accessed, the diagnostic will set the breakpoint mechanism on the 067-0911-XX to the next cursor data address (0A002H for the second vertical point, then 0D800H and 0D802H for the two horizontal points) then repeat steps (2), (3) and (4) as listed above.
6. If all four (two vertical data, two horizontal data) addresses in the cursor display cycle are properly accessed, the test is considered PASSED.

The diagnostic terminal then prints the message:

'05 CURSORS DSY CYCLE PASSED'

and proceeds to the next subtest.

If this subtest failed, the diagnostic terminal prints the appropriate message:

'05 CURSORS DSY CYCLE FAILED—NO DMA OR—BAD DMA ADDRESS'

Indicates that no valid DMA cycles occurred when the Display board circuitry was started in Cursors mode. This may be due to either a failure of the Display board DMA control logic or, a failure of the Control Logic board address generator.

The message:

'05 CURSORS DSY CYCLE FAILED—BAD DMA ADDRESS'

Indicates that at least one valid DMA cycle occurred in cursors display mode but the most recent DMA cycle that was attempted was invalid. This is most likely due to a B-Word address generator failure or a failure in the A-Word/B-Word Address least significant bit toggle circuit.

The Set Parameters selected earlier will determine whether the diagnostic (1) continues to the next subtest, (2) returns to the diagnostic operating system (TEK-DCL) or, (3) enters the troubleshooting routines as signaled to the operator through the following message:

'SCOPE LOOP #1'
'LONG VECT: PRESS ANY KEY TO EXIT'

The first scope loop consists of a continually repeated cursor cycle. A fully functional 7854 will display two dots in opposite corners of the crt screen connected by a vector when this scope loop is running.

The Control Logic and Display board register settings which define this cursors display cycle are as follows:

DISPLAY MODEWORD = 0824H	Cursors mode, vector display.
ACQUIRE MODEWORD = 0000H	All acquire functions off.
A-WORD	Preset to 0A000H—indicates that vertical data for the two cursor points will be located at 0A000H and 0A002H.
B-WORD	Preset to 0D800H—indicates that horizontal data for the two cursor points will be located at 0D800H and 0D802H.

After initializing the above listed addresses with data to generate cursor points in opposite corners of the crt screen, the simulation loop sets up the display board circuitry for cursor display cycles from these addresses, starts the display cycle, and then pauses. Since cursor display cycles are free running, the system needs only wait for a terminal keyboard interrupt, thus assuring that the only bus activity during cursor display cycles is that activity generated by the cursor display cycle itself. When a terminal keyboard interrupt is received, the cursor display cycle is terminated and the system proceeds to the second loop.

Entry into the second stimulation loop is signalled by the message:

'SHORT VECT: PRESS ANY KEY TO EXIT'

This second loop functions identically to the first loop; however, the A-Word and B-Word registers are initialized to 0A008H and 0D808H respectively in order to create a display with two cursor points near the center of the crt screen.

06—CHARACTERS DISPLAY CYCLE SUBTEST

This subtest verifies that the Display Board DMA control circuits interact properly with the Control Logic Board circuits to generate repetitive DMA cycles and data transfers for the characters display function. Proper functioning is checked for both the burst mode and the 8-kHz mode. (In the burst mode, all characters are transferred in a block at the fastest possible rate; in the 8-kHz mode, single characters are transferred at approximately 120-microsecond intervals.) Further, the capacity of the display circuits to detect and act upon special display characters (especially ETX) is checked.

This subtest is run unconditionally whenever the Display DS diagnostic is invoked.

NOTE

Subtest 03 (Y-T: AWRD INTERACTION) must have passed for this subtest to provide valid results.

Once invoked, this subtest performs two independent test phases as follows:

Phase 1 - Burst Mode

1. A display data set consisting of 511 rubout (7FH) characters followed by the EXT character (83H) is generated and loaded into the 7854 Oscilloscope memory (addresses 0A000H through 0A3FFH).

2. The display circuits are reset and system interrupts are disabled; the 911 breakpoint mechanism is set to trip on address 0A000H, which is the first memory address of the character data memory block created above.

3. The display and control logic modeword systems are set to perform burst-mode character display cycles with the character memory beginning at address 0A000H; breakpoint interrupts are enabled.

4. The display cycle is started and the subtest pauses for a set period to allow character display cycles to occur.

5. The display circuits are inhibited and checks are made to determine if a breakpoint occurred. (A breakpoint would have occurred if, during the display cycle, the display circuits DMA controller properly accessed a breakpoint target address. This SHOULD have happened if the breakpoint target address was betweem 0A000H and 0A3FFH; it SHOULD NOT have happened once the breakpoint target address became greater than 0A400H. A breakpoint occurring at greater than 0A400H would indicate that ETX was not properly recognized and that the display cycle was not properly terminated.)

6. The breakpoint target address is incremented by a total value of 4DH; the 911 breakpoint mechanism is set to trip on this new target address and 3, 4, and 5 above are repeated. (This loop continues until the target address is greater than 0A400H.) If all conditions started in 5 above are met, the subtest is reported on the diagnostic terminal screen as having passed; if not, a failure is reported.

@

Phase 2 - 8 kHz Mode

1. The display circuits are reset and system interrupts are disabled; the 911 breakpoint mechanism is set to trip on address 0A000H, which is the first address of the character display data set created in Phase 1.

2. The display and control logic modeword systems are set to perform 8-kHz character display cycles with the character memory beginning at address 0A000H.

3. The display cycle is started and the subtest pauses for a set period to allow character display cycles to occur.

4. The display circuits are inhibited and checks are made to determine if a breakpoint occurred. (If a breakpoint interrupt occurred, this indicates that at least one DMA cycle was properly executed. In that instance, the subtest continues testing; if not, an error is reported on the diagnostic terminal screen.)

5. The display circuits are reset and system interrupts are disabled; the 911 breakpoint mechanism is set to trip on address 0A100H.

6. The display and control logic modeword systems are set to perform 8-kHz character display cycles with the character memory beginning at address 0A000H; breakpoint interrupts are enabled.

7. The display cycle is started in 8-kHz character mode and the subtest pauses until a breakpoint interrupt occurs, which indicates that address 0A100H was accessed properly.

8. The 911 breakpoint mechanism is set to trip on address 0A120H (32 addresses past the original address); the subtest pauses so that the total time interval since the breakpoint of (7) above is approximately 1 millisecond.

9. A check is made to determine if a breakpoint occurred on target address 0A120H (If so, this indicates that DMA cycles reoccurring too rapidly and an error is reported on the diagnostic terminal screen.)

10. If the breakpoint has not occurred in check (9) above, an additional 3-millisecond pause period occurs. (If the breakpoint does not occur until after this delay, this indicates that DMA cycles are occurring too slowly and an error is reported on the diagnostic terminal screen. If the breakpoint occurred during the delay, the subtest is reported on the diagnostic terminal screen as having passed.

This subtest is considered PASSED only if both the Burst mode test and the 8 kHz mode test report passing results. If this is the case, messages on the diagnostic terminal will appear as follows:

```
'06 CHARACTERS DSY CYCLE
BURST MODE: PASSED
8 KHZ MODE: PASSED'
```

This subtest is considered FAILED if either the Burst mode test or the 8 kHz mode test returns a failure message. There are three separate failure messages defined for the Burst Mode test and two failure messages defined for the 8 kHz Mode test.

```
'06 CHARACTERS DSY CYCLE
BURST MODE: FAILED—NO DMA OR—BAD
DMA ADDRESS'
```

Indicates that no valid DMA cycles occurred when the display board was started in burst mode character display operation. Assuming that Display Subtest 03 passed, this may be due to a failure in the Display board display mode control logic, DMA control logic, or character control logic.

```
'06 CHARACTERS DSY CYCLE
BURST MODE: FAILED—BAD DMA ADDRESS'
```

Indicates that at least one valid DMA cycle occurred in burst mode characters display operation but the most recent DMA cycle that was attempted was invalid. This is most likely due to a failure in the Display board interface control logic or possibly due to a failure in the Control Logic board address generators.

```
'06 CHARACTERS DSY CYCLE
BURST MODE: FAILED—ETX NOT RECOGNIZED'
```

Indicates that the ETX character contained within the characters display data memory space did not cause the display cycle to terminate as expected. This is most likely due to a failure in the control character buffer or character control logic circuitry on the A29-Display board.

The 8 kHz mode test, which is run only if the Burst mode test passes, has two error messages defined. The message:

```
'06 CHARACTERS DSY CYCLE
BURST MODE: PASSED
8 KHZ MODE: FAILED—NO DMA OR—BAD
DMA ADDRESS'
```

Indicates that no valid DMA cycles occurred when the display board circuitry was started in 8 kHz mode character display operation.

```
'06 CHARACTERS DSY CYCLE
BURST MODE: PASSED
8 KHZ MODE: FAILED—BAD CYCLE TIMING'
```

Indicates that valid DMA cycles occurred but the time interval betwen successive DMA cycles in 8 kHz mode was Outside the specified limits. In the case of either 8

kHz mode failure message, check the Display mode control logic and interconnections between the real time clock and the DMA control logic on the A29-Display board to determine the cause of the failure.

The Set Parameters selected earlier will determine whether the diagnostic (1) continues to the next (TEK-DCL), or (3) enters the troubleshooting routine as signaled to the operator through the following messages:

'PRESS ANY KEY FOR NEXT LOOP'
'SCOPE LOOP #1—ALTERNATING <SPACE> + <RUBOUT>'

The first three scope loops exercise the Burst mode character display function while the fourth loop exercises the 8 kHz mode character display function. The first of these loops, entry into which is signaled by the above messages, is intended to exercise the data paths into and out of the character generator ROM. It does so by generating and continually displaying a dataset consisting of the two characters 'space' (20H) and 'rubout' (7FH). These two characters were chosen since 'space' will cause none of the dots output from the character generator ROM to be low while 'rubout' will cause all of the dots output from the character ROM to be high. A normally functioning 7854 would display a row of alternating spaces and solid blocks along the top of the screen while running this scope loop.

The Control Logic and Display board register settings which define this first burst mode character display cycle are as follows:

DISPLAY MODEWORD = 0900H	Burst mode characters display.
ACQUIRE MODEWORD = 0000H	All acquire functions off.
A-WORD = preset to 0A000H	Indicates that memory from 0A000H through 0A7FFH will be used for the character display dataset.
Dsy Horiz Preload = 0E002H	Characters preload.
Dsy Vert Preload = 01FF0H	Top of screen.

There is no ETX character in the dataset for this scope loop, therefore, there will be no display done interrupt and the character display cycle, once started, will continue indefinitely. After starting the display board with the above setup parameters, the scope loop routine then pauses to wait for an interrupt from the diagnostic terminal keyboard. As soon as a terminal keyboard interrupt is received and processed, the routine terminates the character display cycle, resets the display hardware, and proceeds to the next scope loop.

Entry into the second scope loop is signaled by the message:

'SCOPE LOOP #2—DISPLAY CONTROL CHARACTERS'

This scope loop exercises the various control characters used by the character display hardware. It does so by generating and continually displaying a dataset consisting of the following sequence of special control characters:

NULL	(80H)
LF	(8AH)
CR	(8DH)
RS	(9EH)
CRLF	(9FH)

This sequence is repeated from address 0A000H through address 0A7FEH. Address 0A7FFH is loaded with the ETX character to allow termination of the display cycle.

The control logic and display board modeword register settings which define the second burst mode character display cycle are as follows:

DISPLAY MODEWORD = 0900H	Burst mode character display.
ACQUIRE MODEWORD = 0000H	All acquire functions off.
A-WORD = preset to 0A000H	Indicates that memory from 0A000H through 0A7FFH will be used for the special characters Display dataset.
Dsy Horiz Preload = 0E002H	Characters preload.
Dsy Vert Preload = 1FF0H	Top of screen.

After the first display cycle, the scope loop pauses till either a real time clock interrupt (restarts the display board cycle) or a terminal keyboard interrupt (resets the Display and Control Logic board then terminates the routine) is received. Use of the RT clock interrupt insures that the Display cycle is restarted periodically thus aiding troubleshooting of the characters display functions.

Entry into the third scope loop is signalled by the message:

'BURST MODE: PRESS ANY KEY TO EXIT'

This routine will display the complete set of printable characters available from the 7854 Display board character display circuitry. Formatting is such that the crt screen of the 7854 under test will display 10 lines of forty characters each, with six blank lines in center screen.

The control logic and display board modeword register settings which define the third character display cycle are as follows:

DISPLAY MODEWORD = 0900H	Burst mode character display.
ACQUIRE MODEWORD = 0000H	All acquire functions off.
A-Word = preset to 0A000H	Indicates that memory starting at address 0A0000H will be used for the character display dataset.

Dsy Horiz Preload = 0E002H	Characters preload.
Dsy Vert Preload = 01FF0H	Top of screen.

After setting up the character display dataset and the hardware registers as listed above, this third scope loop functions in a manner identical to the second scope loop.

Entry into the fourth and final scope loop is signaled by the message:

'8 KHZ MODE: PRESS ANY KEY TO EXIT'

This routine is intended to exercise the 8 kHz mode of character display and is such that a fully functional 7854 running the routine would display a pattern which simulates a full readout pattern in 7854 'SCOPE' mode.

The control logic and display modeword register settings which define the fourth character display cycle are as follows:

DISPLAY MODEWORD = 1940H	8 kHz mode, characters + real-time.
ACQUIRE MODEWORD = 0000H	All acquire functions off.
A-WORD = preset to 0A000H	Indicates that memory beginning at address 0A000H will be used for the character display data.
Dsy Horiz preload = 0E002H	Characters preload.
Dsy Vert preload = 01FF0H	Top of screen.

After setting up the characters display dataset and the hardware registers as listed above, this fourth scope loop functions in a manner identical to the second scope loop.

07—Y-T DISPLAY SUBTEST

This subtest generates a single stimulation loop that aids the operator in verifying and calibrating the digital-to-analog output circuits on the A29-Display Board and the analog signal paths from the Display Board to the crt. The stimulation loop provides that the Display Board circuits are forced into a continuous Y-T display (that is, the service routine for the display done interrupt restarts the Display cycle) with the display memory containing data for a single unit-slope ramp.

NOTE

This subtest is simply an alternate call to the troubleshooting routine of the A-word interaction subtest.

This subtest is run whenever the Display DS diagnostic is invoked provided the LB (Loop on Batch) Set Parameter has not been selected.

NOTE

If the LB option is selected, subtests 07 through 10 will be skipped.

Subtest 03 (Y-T: AWRD INTERACTION) must have PASSED.

Once invoked, this subtest generates and displays in Y-T mode, a digitized unit slope ramp on the crt of the 7854 under test.

The display will continue until the operator presses a key on the diagnostic terminal, at which time, the diagnostic shuts off the ramp display and proceeds to the next subtest.

08—X-Y DISPLAY SUBTEST

This subtest generates a single stimulation loop that aids the operator in verifying and calibrating the digital-to-analog output circuits on the A29-Display board and the analog signal paths from the Display board to the crt. The stimulation loop provides that the display board circuits are forced into a continuous X-Y display. This display will, if all circuits operate properly, be a pattern of dots corresponding to the crt graticule.

NOTE

This subtest performs identically to troubleshooting routine 04, AWRD/BWRD Interaction Subtest, however, it displays a graticule pattern rather than a ramp.

This subtest is run whenever the Display DS diagnostic is invoked provided the LB (Loop on Batch) Set Parameter has not been selected.

NOTE

If the LB option is selected, subtest 07 through 10 will be skipped.

Subtest 04 (X-Y: AWRD/BWRD INTERACTION) must have PASSED.

Once invoked, this subtest generates and displays in X-Y mode, a digitized graticule pattern on the crt of the 7854 under test.

The display will continue until the operator presses a key on the diagnostic terminal, at which time, the diagnostic shuts off the ramp display and proceeds to the next subtest.

09—CURSORS DISPLAY/VECTOR GENERATION SUBTEST

This subtest generates two stimulation loops that aid the operator in verifying and calibrating the Display board vector generation circuitry. The stimulation loops provide

that the Display board circuits are forced into two separate continuous X-Y cursor displays with a vector connecting the two cursor dots.

This subtest is simply an alternate call to the troubleshooting routine of the Cursors Display Cycle subtest.

This subtest is run whenever the Display DS diagnostic is invoked provided the LB (Loop on Batch) Set Parameter has not been selected.

NOTE

If the LB option is selected, subtest 07 through 10 will be skipped.

Subtest 05 (CURSORS DISPLAY CYCLE) must have passed.

Once invoked, the subtest prints the message:

'LONG VECT: PRESS ANY KEY TO EXIT'

Indicating that the first continuous vector display (extending diagonally across the entire crt screen) has been started and that the display will continue until the operator presses a key on the diagnostic terminal. When the operator presses a terminal key, the diagnostic shuts off the first display cycle and then prints the message:

'SHORT VECT: PRESS ANY KEY TO EXIT'

This message indicates that the second continuous vector display (extending diagonally across two divisions in the center of the crt screen) has been started and will continue until the operator presses a key on the diagnostic terminal.

When the operator presses a terminal key, the routine shuts off the second vector display and proceeds to the next subtest.

10—CHARACTERS DISPLAY SUBTEST

This subtest generates two stimulation loops that aid the operator in verifying and troubleshooting the Display Board character generator, shift register, and character data formatting/handling circuits. The two loops provide for checking both Burst and 8-kHz modes.

NOTE

This subtest is simply an alternate call to the final two troubleshooting loops in the Character Display Cycle subtest and is provided for operator convenience in testing those parts of the character display circuits not testable by the Character Display Cycle subtest.

This subtest is run whenever the Display DS diagnostic is invoked provided the LB (Loop on Batch) Set parameter has not been selected.

NOTE

If the LB option is selected, subtest 07 through 10 will be skipped.

Subtest 06 (CHARACTERS DISPLAY CYCLE) must have passed.

Once invoked, the subtest prints the message:

'BURST MODE: PRESS ANY KEY TO EXIT'

Indicating that the first character display pattern (a screenful of characters displayed in burst mode) has been started and that the display will continue until the operator presses a key on the diagnostic terminal. When the operator presses a terminal key, the routine shuts off the first character display and then prints the message:

'8 KHZ MODE: PRESS ANY KEY TO EXIT'

This message indicates that the second character display pattern (a SCOPE mode readout-like pattern) has been started in 8 kHz display mode and that this display will continue until the operator presses a key on the diagnostic terminal. When the operator presses a terminal key, the routine shuts off the second character display and then prepares to exit the display board diagnostic.

DISPLAY DIAGNOSTIC EXIT CONDITIONS

At the conclusion of Subtest 10, the display board diagnostic is complete and it will prepare to return control to the diagnostic operating system. The following events occur before the operating system prompt is received:

1. The message "DIAGNOSTIC COMPLETE" is displayed on the diagnostic terminal screen.

2. If subtests 01,02,03,04,05, and 06 are reported on the terminal screen as having passed, the message "A29 PASS" is displayed on the Microlab I LED indicators.

3. If any subtest (01,02,03,04,05,or 06) is reported on the terminal screen as having failed, the message "A29 FAIL" is displayed on the Microlab 1 LED indicators.

Diagnostic Limitations

There is very close interaction beween the A29-Display board and parts of the A27-Control Logic board. Because of this interaction, certain of the display subtests (those

shared with the Control Logic diagnostic routine) will test not only portions of Display Board but also portions of the Control Logic board. In the event of subtest failure it will not be obvious whether the failure was a Display Board failure or a Control Logic Board failure. The troubleshooting procedures and stimilus routines for signature analysis or oscilloscope based testing will enable the operator to determine which board is at fault and aid in isolation to the faulty component. The diagnostic routine alone will not be able to make this determination in such instances of interaction.

GP [GPIB]

The GPIB command allows invocation of a firmware package to aid signature analysis (Subtest 03—GPIB SA <CR>) and to check general functionality of the address switches and input/output capabilities (Subtest 01 and 02—GPIB COMM <CR>).

To invoke a particular subtest, type (using the diagnostic terminal keyboard) GPIB <space bar> [TEST NAME (Comm or SA)] <CR>.

SET PARAMETERS

No Set Parameters are recognized by this command.

The subtests defined for the GPIB circuits diagnostic package are listed in Table 4-12 and defined functionally in the paragraphs that follow.

01—GPIB REG (GPIB/MPU INTERFACE SUBTEST)

The GPIB REG subtest verifies the action of the following M68488 GPIB registers (located on the A30-GPIB board): Address Mode, Address Status, and Serial Poll registers. Interconnecting circuitry between the microprocessor interface and the GPIA chip is also exercised by this routine.

This subtest is run whenever the GPIB diagnostic is invoked under the following conditions: (1) GPIB COMM <CR> is entered or (2) GPIB <CR> is entered and the last setting entered is 'COMM'.

Once invoked, the microprocessor writes to the GPIA registers. It then examines the read registers to determine that the bits were set correctly.

Upon completion of the subtest, the diagnostic terminal prints 01 GPIB REG PASSED and proceeds to subtest 02 or prints

01 GPIB REG FAILED and
ERR GPIB REG RxR SB[YYYYYYYY] IS[ZZZZZZZZ]

Where 'X' is the GPIA Read Register in error, YYYYYYYY and ZZZZZZZZ are the bit masks, displayed in binary.

If the GPIB/MPU Interface subtest passed, the MPU circuitry on the 7854 GPIB board is considered functional.

02—GPIB I/O

The GPIB I/O subtest verifies the functionality of the handshake lines and the GPIA I/O registers. It also verifies that the GPIB interrupts are generated correctly.

The GPIB I/O subtest is run whenever the GPIB COMM diagnostic is invoked, providing the test fixture prompt—'A GPIB CONTROLLER MUST BE ATTACHED TO RUN TEST 02' was completed. If this condition is not met the subtest will be 'SKIPPED'.

Once invoked, this subtest prints instruction messages to be input on the GPIB test fixture. The subtest proceeds automatically after the user types 'C' on the diagnostic terminal when finished entering commands (on the GPIB test fixture).

Table 4-12
GPIB Diagnostic Subtests

PRINTOUT WHEN INVOKED			
NUMBER	DIAGNOSTIC TERMINAL	MICROLAB I	FAULT COVERAGE
01	GPIB REG	A30—-01	GPIA chip registers and the microprocessor interface components.
02	GPIB I/O	A30—-2	GPIA registers and the GPIB interface components.
03	GPIB SA	A30—-03	GPIA chip and microprocessor interface.

The instruction messages (COMMANDs) are as follows:

DESCRIPTION

PERFORM THE FOLLOWING ON THE GPIB TEST FIXTURE:

Clear all Test Fixture functions
Set Test Fixture A Talker
Assert Remote Enable
Assert Attention
Make the 7854 a listener, Send MLA-14 (Hex 2E)
Cause a Group Execute Trigger, Send (Hex 80)

TYPE 'C' ON THE RS232 TERMINAL WHEN DONE PERFORM THE FOLLOWING ON THE GPIB TEST FIXTURE:

Make the 7854 a listener MLA-14 Send (Hex 2E)
Unassert Attention
Assert EOI
Send an "*" (Hex 2A) as a message
Unassert EOI

TYPE 'C' ON THE RS232 TERMINAL WHEN DONE PERFORM THE FOLLOWING ON THE GPIB TEST FIXTURE:

Assert Attention
Make the 7854 a talker Send MTA-14 (Hex 4E)
Set Test Fixture a listener
Unassert Attention
Handshake in character

% (25 HEX) SHOULD BE MESSAGE RECEIVED
TYPE 'C' ON THE RS232 TERMINAL WHEN DONE

If the subtest passed, the message 'PASSED' appears beside the test name on the terminal, then 'DIAGNOSTIC COMPLETE' appears.

If the GPIB I/O subtest passed the GPIB interface of the 7854 A30-GPIB board is working correctly.

If the subtest fails, the message:

02 GPIB I/O FAILED

and print

ERR INTERRUPT NOT GENERATED

If an interrupt was not generated at the proper interval, and/or

ERR GPIB REG RxR SB[YYYYYYYY] IS [ZZZZZZZZ]

where X is the GPIA Read Register in error, YYYYYYYY and ZZZZZZZZ are the bit masks, displayed in binary.

At the conclusion of this subtest the message:

DIAGNOSTIC COMPLETE

Is printed on the diagnostic terminal.

GPIB SA SIGNATURE ANALYSIS LOOP

The Signature Analysis Loop is a signature routine used to verify the signatures (using a SONY/TEKTRONIX 308 or equivalent) of the 7854 A30-GPIB board.

This subtest is run whenever the GPIB diagnostic is invoked as follows: (1) GPIB SA <CR> or (2) GPIB <CR> and the default settings prevail or the last test setting entered was 'SA'. It's invocation is indicated on the diagnostic terminal as follows: 'SIG ANAL LOOP ENTERED', 'PRESS [GO] KEY TO EXIT.'

NOTE

The 'GO' key is located on the Microlab I front panel.

This routine provides the clock-on/clock-off pulses and a loop which writes to/reads from the various registers on the M68488 GPIA chip.

Press the [GO] key and the diagnostic terminates the loop and prints the message:

DIAGNOSTIC COMPLETE

On the diagnostic terminal.

MP [MPU SIG ANAL]

The MPU command invokes a signature analysis loop for checking signatures of the A27-MPU board CRU I/O flag circuitry.

This command is run whenever MPU <CR> is entered on the diagnostic terminal. Its invocation as indicated on the diagnostic terminal is 'MPU SIG ANAL LOOP V ' 'PRESS [GO] KEY TO EXIT'

Once invoked, the line stimulus is performed in two (2) stages: first, the CRU lines are set high, the program pauses, then all CRU lines are set low. Secondly, all CRU lines are pulsed high, then low in sequence.

Upon exit of the Signature Analysis stimulation routine the terminal will print the message 'DIAGNOSTIC COMPLETE'.

@

SET PARAMETERS

No Set Parameters are recognized by this command.

RAM [RAM TEST]

The RAM command allows for complete functional testing of the 7854 Oscilloscope RAM circuits. It allows for either an automatic check of the A28- RAM board using all of the specific RAM tests or for a specific test of particular memory space on the board.

This RAM command is run whenever RAM [ADDR SPACE], [TYPE TEST] <CR> is printed on the diagnostic terminal. Refer to following text for [ADDR SPACE] and '[TYPE TEST]' parameters.

Values for the "[ADDR SPACE]" parameters are:

<CR>	Defaults to previously set up tests and conditions.
DE	Defaults to options set up in TEK-DCL tables.
AL	Tests all memories configured in 7854 Oscilloscope.
C0	C000 through C7FF.
C8	C800 through CFFF.
DO	DOOO through D7FF.
D8	D8OO through DFFF.
A0	AOOO through A7FF.
A8	A800 through AFFF.
B0	B000 through B7FF.
B8	B800 through BFFF.
SA	Defaults to signature analysis loop on 8K RAM.

Valid values for the "[TYPE TEST]" parameter are:

<CR>	Defaults to previously setup tests and conditions.
DE	Default set of tests are executed (01 through 04).
AL	All tests in order.
01	Write/read alternate 1's and 0's.
02	Address line independence.
03	Data line independence.
04	Address uniqueness.
05	Soak.
06	March.

Upon completion of a subtest, the disposition of that subtest (PASS, FAIL, LOOPING) is printed after the subtest name. At the conclusion of the RAM diagnostic, the diagnostic terminal prints the message "DIAGNOSTIC COMPLETE".

The subtests defined for the RAM diagnotic package are listed in Table 4-13 and defined functionally in the paragraphs that follow.

SET PARAMETERS

The external Set Parameters which may be implemented for the RAM command are defined as follows:

HE (Halt on Error)—If this condition is set, the diagnostic is aborted and an appropriate error message is displayed on the terminal screen when the first RAM error is encountered. Control is returned to the operating system to process the next command.

NH (No Halt on Error)—If this condition is set, all errors are logged upon occurrence and processing continues to completion.

LE (Loop on Error)—If this condition is set, the test being run loops back through the configuration (set up previously) of the RAM in which the error occurred.

NL (No Loop on Error)—If this condition is set, processing continues to completion after an error is detected.

LP (Pass Loop)—If this condition is set, when a RAM test is completed, the diagnostic loops back to the first RAM tested in that portion of the test. The range of looping is determined by the address space parameter entered in the command.

NP (No Pass Loop)—If this condition is set, no further processing will occur.

DI (Disable Error Messages—If this condition is set, all of the RAM error message in the form '**ERROR ADDR. XXXX SB/YYYY IS/ZZZZ' are disabled for display on the diagnostic Terminal screen. All other prompt messages and general error messages are printed normally (including error summary blocks).

ND (Enable Error Message)—If this condition is set, all error messages are displayed upon occurrence.

01—WRITE/READ ALTERNATE ONES AND ZEROS

This diagnostic module verifies that both a one (1) and a zero (0) can be written to and read from each memory cell in the RAM memory space under test.

NOTE

This subtest is limited to checking only basic functionality of the individual memory cells. Other memory defects are covered in succeeding subtests.

This subtest requires that the A27-MPU board be functional.

Table 4-13
RAM Diagnostic Subtests

PRINTOUT WHEN INVOKED			
NUMBER	DIAGNOSTIC TERMINAL	MICROLAB I	FAULT COVERAGE
01	WR/RD 1/o	A28—-01	Data line shorts, opens and pattern sensitivity.
02	ADDR IND	A28—-02	Address line shorts and opens.
03	DATA IND	A28—-03	Data line shorts, opens and adjacent disturb.
04	ADDR UNIQ	A28—-04	Address uniqueness, shorts and opens in address lines.
05	SOAK	A28—-05	Data retention of both ones and zeros.
06	MARCH	A28—-06	Address uniqueness and data disturb.
SA	SA	A28—-07	Stimulus for troubleshooting using signature comparison.

The Write/Read Alternate Ones/Zeros subtest is run whenever the RAM diagnostic is invoked and:

1. AL, DE or 01 is specified as the test(s) to run.
2. RAM <CR> or RAM addr <CR> was entered and the default settings prevail (defaults to the last settings entered).

Once invoked this subtest writes patterns of '5555' and 'AAAA' (alternating ones and zeros) into memory, waits approximately 1/2 second for the RAM to settle, then attempts to read back the pattern.

If this subtest passed, the diagnostic terminal prints 01 WR/RD 1/0 PASSED and proceeds to the next subtest.

If this subtest failed, the diagnostic terminal prints

'01 WR/RD 1/0 FAIL'
'**ERR ADDR[address][should be-data value] [is-data value]'

[address] refers to the address of the failing data value.

[should be-data] is the hexadecimal equivalent of the binary data resident in that memory space if the RAM is functioning correctly.

[is-data] is the hexadecimal equivalent of the binary data at that memory location.

The program will continue until all locations have been read (within the selected memory block), printing the message as above, for each error found.

If the 'DI' option had been selected, the diagnostic terminal prints only:

'SUMMARY BLOCK[beginning address]
'[number of]FAILURES
'ERROR BIT MASK [Bit mask in hexadecimal notation]

[beginning address] refers to the beginning address of the memory block which is in error.

[number of] is the number of errors found in the specified memory block.

[bit mask in hexadecimal notation] The diagnostic terminal displays the bit mask in hexadecimal form. When converted to binary, the 0's designate correct bits, and the 1's designate defective bit levels.

Example—If the hexadecimal readout is 0020H, converted to binary—0000 0000 0010 0000 shows that bit 5 is in error.

After the above data is printed on the diagnostic terminal the routine will begin the next subtest.

02— ADDRESS LINE INDEPENDENCE

This diagnostic module verifies that no address line shorts exist on the A28-RAM board.

NOTE

This subtest is limited to checking only the independence of the address lines. It does not test data lines or individual RAM chips.

This subtest requires that the A27-MPU board be functional.

The Address Line Independence subtest is run whenever the RAM diagnostic is invoked and:

1. AL, DE or 02 is specified as the test(s) to run.
2. RAM <CR> or RAM addr <CR> was entered and the default settings prevail (defaults to the last setting entered).

Once invoked, this subtest first tests the independence within a 1K block of memory by bringing each of the lower twelve (12) address lines high one at a time, write an 'FFFF' to that location, bring the 12 address lines low, write '0000' to that location then check that the original memory location still contains 'FFFF'.

The subtest then checks the independence between the 1K blocks in the RAM memory space ('AL' parameter only) by writing an 'FFFF' to each block address (one at a time, excluding block address A000), writing '0000' to 'AD00', then checking the original block for 'FFFF'.

If this subtest passed, the diagnostic terminal prints:

'02 ADDR IND PASSED' and proceeds to the next subtest.

If this subtest failed, the diagnostic terminal prints:

'02 ADDR IND FAIL'
'**ERR ADDR [address][should be-data][is-data]

[address] refers to the address of the failing data value.

[should be-data] is the hexadecimal equivalent of the binary data resident in that memory space if the RAM is functioning correctly.

[is-data] is the hexadecimal equivalent of the binary data at that memory location.

The program will continue until all locations have been read (within the selected memory block), printing the message as above, for each error found.

If the 'DI' option had been selected the diagnostic terminal prints only:

'SUMMARY BLOCK [beginning address]
'[number of] FAILURES
'ERROR BIT MASK [bit mask in hexadecimal notation]

[beginning address] refers to the beginning address of the memory block which is in error.

[number of] is the number of errors found in the specified memory block.

[bit mask in hexadecimal notation] The diagnostic terminal displays the bit mask in hexadecimal form. When converted to binary, the 0's designate correct bits, and the 1's designate defective bit levels.

Example—If the hexadecimal readout is 0020H, converted to binary—0000 0000 0010 0000 shows that bit 5 is in error.

03— DATA LINE INDEPENDENCE

This diagnostic subtest verifies that the data lines are not shorted together.

NOTE

This subtest checks only those data lines comprising a given word and does not disturb the entire address space.

This subtest requires that the A27-MPU board be functional.

The Data Line Independence subtest is run whenever the RAM diagnostic is invoked and:

1. AL, DE or 03 is specified as the test(s) to run.
2. RAM <CR> or RAM addr <CR> was entered and the default settings prevail (defaults to the last settings entered).

Once invoked, this subtest writes zeros to all address locations specified. Each data line is then brought high, one at a time for all addresses specified in the address parameter. The neighboring data lines are then examined for a zero level.

If this subtest passed, the diagnostic terminal prints:

'03 DATA IND PASS'

The Set Parameters will determine how the diagnostic will proceed.

If this subtest failed, the diagnostic terminal prints:

'03 DATA IND FAIL'
'**ERR ADDR [beginning address][should be-data][is-data]

[address] refers the failing data value.

[should be-data] is the hexadecmal equivalent of the binary data resident in that memory space if the RAM is functioning correctly.

[is-data] is the hexadecimal equivalent of the binary data at that memory location.

The program will continue until all locations have been read (within the selected memory block), printing the message as above, for each error found.

If the 'DI' option had been selected the diagnostic terminal prints only:

'SUMMARY BLOCK [beginning address]
'[number of]FAILURES]'
'ERROR BIT MASK [bit mask in hexadecimal notation]

[beginning address] refers to the beginning address of the memory block which is in error.

[number of] is the number of errors found in the specified memory block.

[bit mask in hexadecimal notation] The diagnostic terminal displays the bit mask in hexadecimal form. When converted to binary, the 0's designate correct bits, and the 1's designate defective bit levels.

Example—If the hexadecimal readout is 0020H, converted to binary—0000 0000 0010 0000 shows that bit 5 is in error.

After the above data is printed on the diagnostic terminal, the routine will begin the next subtest.

04—ADDRESS LINE UNIQUENESS

This diagnostic subtest verifies that each address corresponds to a unique memory location (the chip selects, and the address lines are in working order).

NOTE

This subtest requires that the MPU board be functional.

The Address Line Uniqueness subtest is run whenever the RAM diagnostic is invoked and:

1. AL, DE or 04 is specified as the test(s) to run.
2. RAM <CR> or RAM addr <CR> was entered and the default settings prevail (defaults to the last settings entered).

Once invoked, this subtest writes to all predetermined addresses specified, then reads back the data to verify that there is only one address by which a particular memory location can be accessed.

If this subtest passed, the diagnostic terminal prints:

'04 ADDR UNIQ PASS'

The Set Parameters will determine how the diagnostic will proceed.

If this subtest failed, the diagnostic terminal prints:

'04 ADDR UNIQ FAIL'
'**ERR ADDR [address][should be-data][is-data]

[address] of the failing data value.

[should be-data] is the hexadecimal equivalent of the binary data resident in that memory space if the RAM is functioning correctly.

[is-data] is the hexadecimal equivalent of the binary data at that memory location.

The program will continue until all locations have been read (within the selected memory block), printing the message as above, for each error found.

If the 'DI' option had been selected the diagnostic terminal prints:

'SUMMARY BLOCK [beginning address]
'[number of]FAILURES]'
'ERROR BIT MASK [bit mask in hexadecimal notation]

[beginning address] refers to the beginning address of the memory block which is in error.

[number of] is the number of errors found in the specified memory block.

[bit mask in hexadecimal notation] The diagnostic terminal displays the bit mask in hexadecimal form. When converted to binary, the 0's designate correct bits, and the 1's designate defective bit levels.

Example—If the hexadecimal readout is 0020H, converted to binary—0000 0000 0010 0000 shows that bit 5 is in error.

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After the above data is printed on the diagnostic terminal, the routine will begin the next subtest.

05—SOAK TEST

This diagnostic subtest verifies the static nature of the RAM chips under test.

NOTE

This subtest tests only the data retention capability of the RAM chips. Other chip and board functions are not tested by this subtest.

This subtest requires that the A27-MPU board be functional.

The Soak subtest is run whenever the RAM diagnostic is invoked and:

1. AL or 05 is specified as the test(s) to run.
2. RAM <CR> or RAM addr <CR> was entered and the last setting was AL or 05.

Once invoked, this subtest writes an 'AAAA' (alternating ones and zeros) to memory, pauses approximately 10 seconds, then attempts to read back the entered pattern.

The Subtest then writes '5555' (alternating zeros and ones) to memory, pauses approximately 10 seconds, then attempts to readback the '5555' pattern.

If this subtest passed, the diagnostic terminal prints:

'05 SOAK PASS'

The Set Parameters will determine how the diagnostic will proceed.

If the test failed, the error messages are enabled and printed for each error found as follows:

'05 SOAK FAIL'
'**ERR ADDR [address][should be-data][is-data]'

[address] the failing data value.

[should be-data] is the hexadecmal equivalent of the binary data resident in that memory space if the RAM is functioning correctly.

[is-data] is the hexadecimal equivalent of the binary data at that memory location.

The program will continue until all locations have been read (within the selected memory block), printing the message as above, for each error found.

If the 'DI' option has been selected, the diagnostic terminal prints:

'SUMMARY BLOCK [beginning address]
'[number of]FAILURES'
'ERROR BIT MASK [bit mask in hexadecimal notation]

[beginning address] refers to the beginning address of the memory block which is in error.

[number of] is the number of errors found in the specified memory block.

[bit mask in hexadecimal notation] The diagnostic terminal displays the bit mask in hexadecimal form. When converted to binary, the 0's designate correct bits, and the 1's designate defective bit levels.

Example—If the hexadecimal readout is 0020H, converted to binary—0000 0000 0010 0000 shows that bit 5 is in error. [beginning address] refers to the first address of the address space being read.

After the above is printed on the diagnostic terminal, the routine will begin the next subtest.

06—MARCH TEST

This diagnostic subtest verifies that writing to a memory location will not disturb another memory location.

NOTE

This subtest requires that the A27-MPU board be functional.

The March subtest is run whenever the RAM diagnostic is invoked and:

1. AL or 06 is specified as the test(s) to run.
2. RAM <CR> or RAM addr <CR> was entered and the last setting was AL or 06.

Once invoked, this subtest initially writes a one to all memory location.

—Then, a one is read and a zero written to each location sequentially from the lowest to highest address.

—Next, a zero is read and a one written to each location sequentially from the lowest to the highest address.

—Again, a one is read and a zero written to each location sequentially from the lowest to the highest address.

—Then, a zero is read and a one is written to each location sequentially from the lowest to the highest address.

—Finally, read ones in all locations.

If this subtest passed, the diagnostic terminal prints:

'06 MARCH PASS'

The settings of the Set Parameters determine how the diagnostic will proceed.

If the test failed, the error messages are enabled and printed for each error found as follows;

'06 MARCH FAIL'
'ERR ADDR [address][should be-data][is-data]'

[address] of the failing data values.

[should be-data] is the hexadecimal equivalent of the binary data resident in that memory space if the RAM is functioning correctly.

[is-data] is the hexadecimal equivalent of the binary data at that memory location.

The program will continue until all locations have been read (within the selected memory block), printing the message as above, for each error found.

If the 'DI' option had been selected, the diagnostic terminal prints:

'SUMMARY BLOCK [beginning address]
'[numbered of] FAILURES'
'ERROR BIT MASK [bit mask in hexadecimal notation]

[beginning address] refers to the beginning address of the memory block which is in error.

[number of] is the number of errors found in the specified memory block.

[bit mask in hexadecimal notation] The diagnostic terminal displays the bit mask in hexadecimal form. When converted to binary, the 0's designate correct bits, and the 1's designate defective bit levels.

Example—If the hexadecimal readout is 0020H, converted to binary—0000 0000 0010 0000 shows that bit 5 is in error.

SA SIGNATURE ANALYSIS LOOP

This stimulus routine is used in conjunction with appropriate signature tables for troubleshooting the A28-RAM board.

NOTE

Any Signature Analyzer compatible with the SONY/TEKTRONIX 308 Signature Analyzer may be used. Refer to Test Equipment in the Troubleshooting section.

This subtest requires that the A27-MPU board be functional.

The Signature Analysis Loop is entered whenever RAM SA <CR> is typed on the diagnostic terminal.

Once invoked, this routine provides the clock-on/clock-off pulses and a loop which reads all 8K memory locations with the memory range of the option entered (2K, 4K, 8K).

The invocation of this subtest is signaled through the following diagnostic terminal message:

'SIG ANAL LOOP ENTERED'
'PRESS [GO] KEY TO EXIT'

RO [ROM]

The ROM check sum command allows invocation of a complete check sum test of the A31-ROM board or the 067-0961-XX Diagnostic Memory board. A user selected command invocation line parameter determines the board checked.

The diagnostic is run whenever 'ROM [OPERATIONAL PARAMETER] <CR>' is entered on the diagnostic terminal.

[Operational Parameter] type (on the diagnostic terminal) '78' or '7854' to select the 7854 ROM board test, and 09 or 0961 to select the 067-0961-XX Diagnostic Memory board test.

Also invocation through Microlab I front panel by depressing either [8] or [9] while switching ON the power.

[8]—equivalent to "ROM 7854"
[9]—equivalent to "ROM 0961"

All other diagnostic system functions are bypassed. Press 'reset' to return control to the diagnostic operating system (TEK-DCL). Once invoked, the diagnostic calculates 8 bit check sums of blocks of memory space corresponding to physical ROM or EPROM chips. These calculations are then compared to reference values stored in the headers of each (ROM/EPROM). If the calculated check sum value does not match the stored reference value, a 2 digit error code is displayed. '**ERROR [2 digit error code]' 'DIAGNOSTIC COMPLETE'.

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7854 memory blocks are as follows:

Memory Address	I.C.
0000H through 3FFFH	ROMS U100, U110
4000H through 7FFFH	ROMS U200, U210

067-0961-XX memory blocks as follows:

Memory address	I.C.
0000H through 0FFF	EPROMS U330, U430
1000H through 1FFF	EPROMS U310, U410
2000H through 2FFF	EPROMS U100, U200
3000H through 3FFF	EPROMS U120, U220
4000H through 4FFF	EPROMS U320, U420
5000H through 5FFF	EPROMS U300, U400
6000H through 6FFF	EPROMS U110, U210

Error codes are as follows:

Code Number	Description
ERROR 51	ROM ERROR—U100 on 7854 ROM BOARD
ERROR 52	ROM ERROR—U110 on 7854 ROM BOARD
ERROR 53	ROM ERROR—U200 on 7854 ROM BOARD
ERROR 54	ROM ERROR—U210 on 7854 ROM BOARD
ERROR 61	EPROM ERROR—U200 on 067-0961-XX
ERROR 62	EPROM ERROR—U210 on 067-0961-XX
ERROR 63	EPROM ERROR—U220 on 067-0961-XX
ERROR 64	EPROM ERROR—U230 on 067-0961-XX
ERROR 65	EPROM ERROR—U100 on 067-0961-XX
ERROR 66	EPROM ERROR—U110 on 067-0961-XX
ERROR 67	EPROM ERROR—U120 on 067-0961-XX
ERROR 68	EPROM ERROR—U130 on 067-0961-XX
ERROR 69	EPROM ERROR—U400 on 067-0961-XX
ERROR 70	EPROM ERROR—U410 on 067-0961-XX
ERROR 71	EPROM ERROR—U420 on 067-0961-XX
ERROR 72	EPROM ERROR—U430 on 067-0961-XX
ERROR 73	EPROM ERROR—U300 on 067-0961-XX
ERROR 74	EPROM ERROR—U310 on 067-0961-XX
ERROR 75	EPROM ERROR—U320 on 067-0961-XX
ERROR 76	EPROM ERROR—U330 on 067-0961-XX

RS [ROM SIGNATURE ANALYSIS]

The ROM Signature command invokes a signature analysis stimulation loop for test and troubleshooting of the 7854 Oscilloscope ROM Board (A31) and the 067-0961-XX Diagnostic Memory Board. Signature analysis is performed by reading all memory address from 0000H through 9FFFH. This sequence is repeated continuously until the operator presses the Microlab I GO key. All 7854 Oscilloscope interrupts are disabled (except reset and load). Since it is used to test the 7854 Oscilloscope ROM, the diagnostic code is located permanently on the 067-0911-XX Interface Board PROM space (in addresses 0E800H through 0FFFFH).

The ROM Signature command is invoked through one of three paths: (1) Enter RS <CR> on the diagnostic system terminal, (2) Automatically, by Self Test or power up test logic (Error code 43), and (3) 'A' key on Microlab I front panel is depressed upon power up of the diagnostic system. (All other operating system functions will be bypassed.) At the conclusion of the ROM Signature routine the diagnostic terminal prints the message:

DIAGNOSTIC COMPLETE'

TI [REAL TIME CLOCK]

The Real Time Clock command invokes a diagnostic test and troubleshooting routine for the A29-Display board real time clock circuits. This test is shared with the A29-Display board diagnostic routine and will also be invoked as a part of the DS command sequence.

NOTE

The Real Time Clock command requires that the 7854 Oscilloscope A27-MPU board is functional.

This diagnostic is run whenever TI <CR> is entered on the diagnostics terminal.

The diagnostic test for the real time clock circuits is a two-stage test. Initially, the diagnostic verifies that the circuits produce clock pulses by enabling the clock and then pausing for 100 milliseconds. Occurrence of a clock interrupt is detected using the breakpoint mechanism. If no clock interrupt is received during the delay, the clock is considered to be inoperative and the message "FAILED - CLOCK MISSING" is displayed on the diagnostic terminal screen.

If clock pulses are received during the delay, the diagnostic then checks the clock period. Upon receipt of the next clock pulse, the diagnostic begins a 12-millisecond test period. After this period, a check is made to determine if an interrupt occurred. If so, the message "FAILED - CLOCK FAST" will be displayed on the diagnostic terminal screen. If not, an additional 8-millisecond period is begun. If, at the end of this period, the interrupt has not occurred, the message "FAILED - CLOCK SLOW" is displayed on the diagnostic terminal screen. If the interrupt occurs during the 8-millisecond delay, the clock test is considered to have passed.

The troubleshooting routine associated with this diagnostic is a single scope loop that periodically enables and disables the real time clock circuit while preventing the 7854 Oscilloscope microprocessor from responding to such interrupts.

SET PARAMETERS

The Set Parameters defined for this subtest are as follows:

HE (Halt on Error)—This option is not implemented because the default condition is to return to the TEK-DCL operating system at completion.

LE (Loop on Error)—If the LE option is selected upon clock test error detection, the diagnostic prints the appropriate error messages and enters the real time clock troubleshooting loop.

LP (Loop on Pass)—If the LP option is selected, the diagnostic enters the associated troubleshooting routine if the clock circuits meet specifications.

LB (Loop on Batch)—This option is not implemented.

DI (Disable Error Messages)—This option is not implemented.

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SPECIFICATION

The following characteristics for the 067-0911-00 Diagnostic Test Interface apply when installed in a fully operable MicroLab I mainframe operating at an ambient temperature between 0° and +55° C.

TABLE 5-1
Electrical Characteristics

Characteristic	Performance Requirement
Power Consumption	
+5 V	≤1.1 amperes
+12 V*	≤100 milliamperes
-5 V*	≤50 milliamperes

*No power is drawn from the +12-volt and -5-volt supplies unless the Test Processor board is installed for self test of the 067-0911-00.

TABLE 5-2
Environmental Characteristics

Characteristics	Description
Temperature	
Operating	0° to +55° C (+32° to +131° F).
Storage	-62° to +85° C (-79° to +185° F)
Altitude	
Operating	4,500 m (15,000 ft.) maximum
Storage	15,000 m (50,000 ft.) maximum
Humidity	
Operating	80% relative (max), noncondensing.
Storage	80% relative (max), noncondensing

THEORY OF OPERATION

This section of the manual describes the operation of the 067-0911-XX Diagnostic Test Interface. The description begins by telling how the 067-0911-XX fits into the architecture of the 7854 Oscilloscope and the MicroLab I, using block diagram Figure 6-1. The description continues in detail, explaining the relationship between the stages of each major circuit. Schematic diagrams of all major circuits are located in Section 10, Diagrams and Circuit Board Illustrations. Wide, shaded lines outline the stages on each schematic; the stage names are within shaded boxes. Refer to the appropriate schematic diagram in section 10 when reading this description.

HOW THE 067-0911-XX DIAGNOSTIC TEST INTERFACE FITS INTO THE 7854 ARCHITECTURE

The 067-0911-XX Diagnostic Test Interface is part of a system that forms a bus extension of the 7854 digital section. The 067-0911-XX receives address, data, and control buses from the Microprocessor Board of the 7854 under test. The 067-0911-XX provides the 7854 under test with:

1. Additional PROM memory (4 k words) to the 7854 digital system bus. Of the 4 k words, 2 k are permanently resident and 2 k are in a bank that is switchable into a 1 k block of 7854 address spaces.

2. Additional RAM memory (1.5 k words) to the 7854 digital system bus. Of the 1.5 k words, 512 are permanently resident in the RAM, and 1024 may be enabled or disabled under program control.

3. Additional I/O devices for the 7854 digital system bus, such as:

   a. An RS-232 serial I/O port for a display terminal,

   b. The front-panel keyboard of the MicroLab I, and

   c. The display of the MicroLab I.

4. Control devices to monitor and control operations on the 7854 digital system bus, such as:

   a. Full-function breakpoint, and

   b. A "Load" interrupt on Reset to force operation into diagnostic firmware.

Devices in the 067-0911-XX system are located in unused areas of 7854 address space, which allows normal 7854 operation (if desired) when the 067-0911-XX is installed and the 067-0961-XX Diagnostic Memory Board is not installed (push the "Special" button on the front panel of the MicroLab I to begin normal oscilloscope operation).

Firmware in the 067-0911-XX consists of the following functional modules:

- Diagnostic operating system (permanent).
- Debug routines (examine, dump, registers, etc.).
- ROM test, ROM signature (bank-switched, 1).
- Self-test, 067-0911/MicroLab I (bank-switched, 2).

The Diagnostic Operating System includes the command processor, the interrupt handlers, the I/O utilities, and the breakpoint routines.

The 067-0961-00 Diagnostic Memory Board contains firmware for the actual diagnostic test of the 7854.

HOW THE 067-0911-XX DIAGNOSTIC TEST INTERFACE FITS INTO THE MICROLAB I ARCHITECTURE

The 067-0911-XX Diagnostic Test Interface connects to the MicroLab I to make the MicroLab I part of a system to test the 7854 Oscilloscope. The A3 Interface Board plugs into the connector where the MicroLab I's Personality Board would normally operate. The 067-0911-XX:

1. Permits memory and I/O devices in the MicroLab I to send data to the 7854, and

2. Permits the 7854 to control those devices.

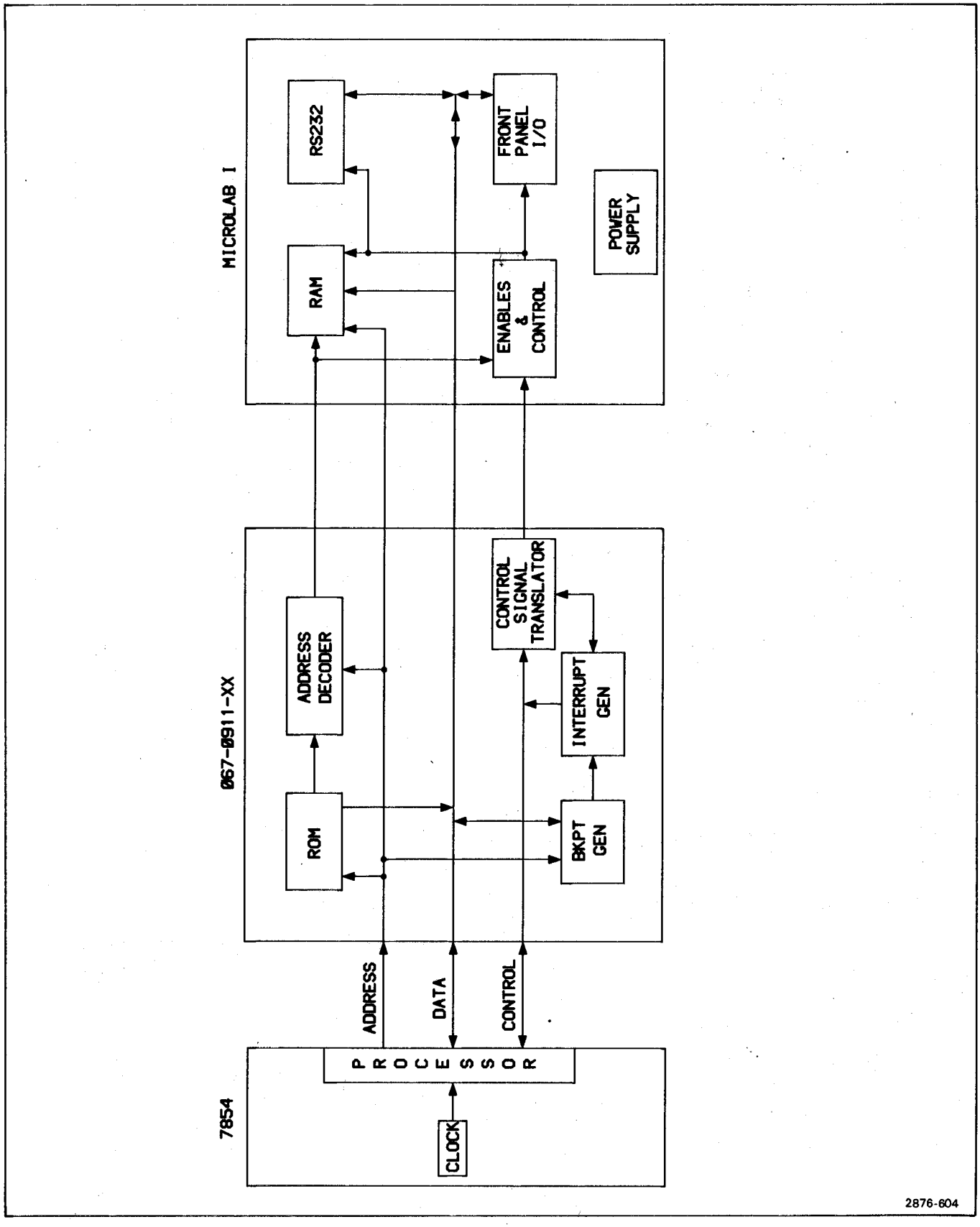


Figure 6-1. Simplified block diagram of 7854, 067-0911-XX, and MicroLab I system.

The A3 Interface Board provides a ROM, firmware, links to the 7854's processor, and a breakpoint mechanism. The A3 Interface Board performs the following processor-dependent functions:

- address decoding,
- control signal translation, and
- interrupt encoding and control.

When used in the 067-0911-XX Diagnostic Test Interface, the MicroLab I performs the processor-independent functions of the test system, such as RAM, I/O via its front-panel keyboard, and serial I/O via its RS-232 port. Figure 6-1 shows a simplified block diagram of the 7854, 067-0911-XX and MicroLab I system. Refer to the MicroLab I instruction manual for further information.

DIAGNOSTIC PACKAGE CIRCUIT DESCRIPTION

Complete schematic diagrams are located in Section 10, Diagrams and Circuit Board Illustrations. The number inside a diamond preceding a heading in the following discussion indicates the diagram being described. Wide, shaded lines enclose the stages of each major circuit; the stage names are within shaded boxes, and as subheadings in the discussion of that schematic diagram.

The A3 Interface Board receives the address, data and control buses of the 7854 digital section. (The buses connect via the A1 Cable Termination Board and its cables.) The A3 Interface Board serves as a bus extension to provide additional PROM memory and control registers to the 7854 bus, and as a bus interface to allow memory and I/O devices in the MicroLab I mainframe to interface to the 7854 bus.

◇1 PROM MEMORY

The PROM Memory circuit contains the stored firmware which constitutes the Diagnostic Operating System. The 7854 microprocessor may access this stored firmware by placing on the WA Bus an address in the appropriate address range. Selected data from the PROMs then appears on the BD Bus for presentation back to the microprocessor.

The PROM Memory consists of U120, U220, U225 and U320; and buffers U110 and U200.

The PROM Memory's two sections are designated PROM 0 and PROM 1. A low level on the $\overline{\text{PROMCØ}}$ line will cause PROM Ø (U220 and U320) to place data on the BD Bus. A low level on the $\overline{\text{PROMC1}}$ line will cause PROM 1 (U120 and U225) to place data on the BD Bus. When the $\overline{\text{BUFDRV}}$ line is at a low level, bidirectional buffers U110 and U200 transfer data from the BD Bus to the 7854 PD Bus. The buffers send data from the 7854 PD Bus to the A3 Interface Board's BD Bus when the $\overline{\text{BUFDRV}}$ line is at a high level.

PROM Ø (U220 and U320) contains 2048 16-bit words located in the 7854 address spaces F000 through FFFF. The Address Decoding logic on diagram 2 produces the $\overline{\text{PROMCØ}}$ signal that enables PROM Ø.

PROM 1 (U120 and U225) also contains 2048 16-bit words, but this PROM data is located in the 7854 address space from address E800 through EFFF. Because this address range allows only 1024 unique word addresses, the highest order address bit on PROM chips U120 and U225 is connected to the PROMBK line from the Control Register (diagram 4) rather than to the 7854 address bus. This allows the 7854 microprocessor to determine, under program control, which block of data (in PROMs U120 and U225) will be accessible to the bus. This method of control effectively "bank switches" 2048 words of PROM data into 1024 word-address spaces.

◇2 ADDRESS DECODING & CONTROL

The Address Decoding & Control circuitry decodes address information from the 7854 and produces control signals for the A3 Interface Board and the MicroLab I.

ADDRESS DECODING

Two one-of-four decoders (U420A and B) and a group of gates (U430A, U435D, U460C, U410B, U460A, U540D, U410A and U380A) monitor the WA Bus and the $\overline{\text{PMEM}}$ line. (A low level on the $\overline{\text{PMEM}}$ line indicates that a valid address is on the WA Bus.)

Decoder U420B and gate U410B monitor the WA10 through WA14 lines. When the address on the WA Bus is between E800 and E8FF, U420B will produce a low level on the $\overline{\text{PROMC1}}$ line. The low level on $\overline{\text{PROMC1}}$ will enable PROM C1, on diagram 1, and will activate U465, which will assert a high level on the OSMEM line to indicate that a device on the A3 Interface Board is addressed. When the address on the WA Bus is between F000 and FFFF, U460A will produce a low level on the $\overline{\text{PROMCØ}}$ line. The low level on $\overline{\text{PROMCØ}}$ will enable PROM CØ, on diagram 1, and will activate U465 which will assert a high level on the OSMEM line.

Gate U460C receives the inverted YØ output of U420B and the WA9 line. When the address on the WA Bus is between E400 and E7FF, U460C will assert a low level on the $\overline{\text{RAMCØ}}$ line. The low level on $\overline{\text{RAMCØ}}$ will activate U465, which will assert the OSMEM signal.

Gate U435D also receives the inverted YØ output of U420B. Its other input is the inverted WA9 line. When the address on the WA Bus is between E000 and E3FF, U435D will assert a high level on the $\overline{\text{M}}$/IO line.

Decoder U420A and gate U430A monitor the WA4 through WA8 and $\overline{\text{M}}$/IO lines. The $\overline{\text{M}}$/IO line must be at a high level for U430A and U420A to operate. Decoder U420A will respond to four groups of WA Bus addresses. The four groups of addresses, and the output U420A will produce for each group, are as follows:

Address Range	Output of U420A
E38Ø to E39E	$\overline{\text{BKREGCS}}$ (Breakpoint address REGister Chip Select)
E3AØ to E3BE	$\overline{\text{CTREGCS}}$ (ConTrol REGister Chip Select)
E3CØ to E3DE	$\overline{\text{BKDATA}}$ (BreaKpoint DATA latch)
E3EØ to E3FE	$\overline{\text{ONBDIO}}$ (ON BoarD Input/Output to MicroLab I)

The output of U430A, which enables U420A, will activate U465 to assert the OSMEM signal.

Gates U540D, U410A, U380A and U460D are connected so that U460D will assert a low level on the $\overline{\text{RAMC1}}$ line when the $\overline{\text{RAM1EN}}$ is high and the address on the WA Bus is between 9800 and 9FFF. (FF U350 on diagram 4, sets the $\overline{\text{RAM1EN}}$ line to a high level.) The low level on $\overline{\text{RAMC1}}$ will activate U465, which will assert a high level on the OSMEM line.

The $\overline{\text{ONBDIO}}$ line activates devices in the MicroLab I mainframe, as follows:

Address	Device	Function
E3EØ	MicroLab I F/P Display Data	W
E3E2	MicroLab I F/P Display Data	W
E3E4	MicroLab I F/P Keyboard Data	R
E3E4	MicroLab I F/P Keyboard Flag Reset	W
E3E8	MicroLab I Terminal I/O Control	R/W
E3EA	MicroLab I Terminal I/O Data	R/W
E3EC	MicroLab I Cassette I/O Control	R/W
E3EE	MicroLab I Cassette I/O Data	R/W
E3FØ	MicroLab I Modem I/O Control	R/W
E3F2	MicroLab I Modem I/O Data	R/W

CONTROL

The Control signal translation circuitry produces two signals for the MicroLab I and six signals for other parts of the A3 Interface Board. The Control circuitry is shown on the lower part of diagram 2.

Buffer U510 has Schmitt trigger inputs that reduce any noise present on the cable from the 7854.

A high on the 7854 $\overline{\text{PMEM}}$ line when the processor is between bus cycles will cause gate U380B and inverter U380C to assert a high on the R/$\overline{\text{W}}$ line to the MicroLab I. During a bus cycle, the $\overline{\text{PMEM}}$ line will be at a low level, which will allow the R/$\overline{\text{W}}$ line to follow the state of the PR/W line from the 7854.

Flip-flop U535B and gates U435C, U540A and C and U560C will produce the Bus enable ($\overline{\text{E}}$) signal for the MicroLab I. The timing is different for read and write cycles. Figures 6-2 and 6-3 show the relation of the inputs to the $\overline{\text{E}}$ output.

On the first processor instruction cycle after the $\overline{\text{PRESET}}$ signal ends, inverter U520B and FFs U535A and U530B will generate the $\overline{\text{INTLD}}$ signal for the 7854 Microprocessor Board. This ensures that a power-up or a reset condition will force the Microprocessor Board into the Diagnostic System firmware. Figure 6-4 shows the timing of the $\overline{\text{INTLD}}$ signal relative to its constituent signals.

When the 7854 Microprocessor Board addresses the range E400 to FFFF and the PWAIT line is high, gates U430B, U540B and U560A will produce the INTRDY signal for the 7854.

The buffered PR/$\overline{\text{W}}$ signal, from U510 pin 5, becomes the IR/$\overline{\text{W}}$ signal. The IR/$\overline{\text{W}}$ signal is inverted, by U520E,

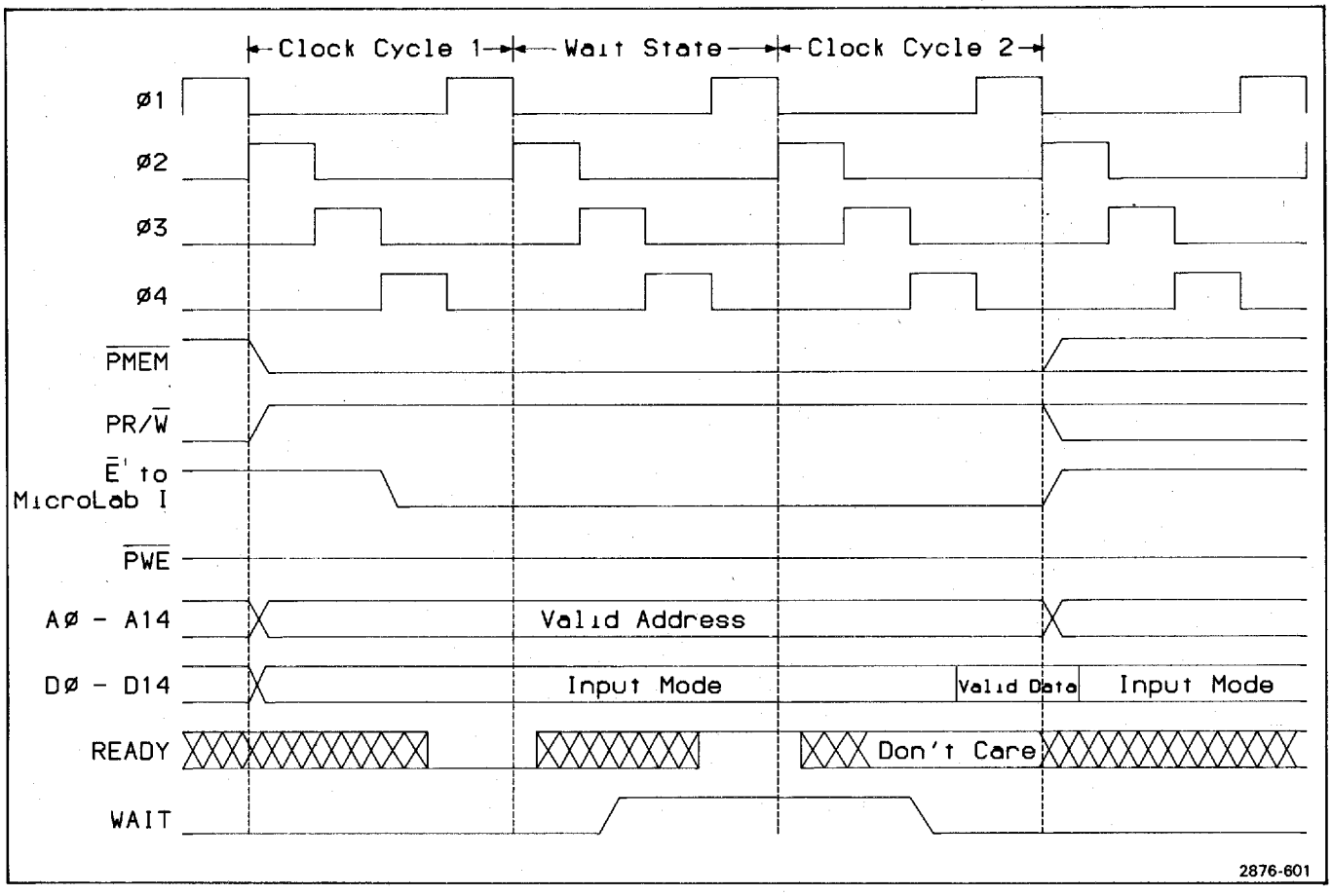


Figure 6-2. Timing of bus enable ($\overline{E}$) signal for MicroLab I during a read cycle.

to form the $\overline{READ}$ signal. The buffered Pø4 signal is inverted, by U440C, to form $\overline{PHASE\ 4}$. Low levels on the buffered $\overline{PWE}$ and PR/$\overline{W}$ lines will activate U540C to produce a high level on the WRP line.

BREAKPOINT ADDRESS LATCH & COMPARATORS

The Breakpoint Address Latch & Comparators compare the data on the WA Address Bus to a stored reference value on the RA Bus to determine if they are equal, and produces interrupt control signals for the 7854. The Breakpoint Address Latch & Comparators circuitry has sections called Address Latch, Address Comparators and Interrupt Control.

ADDRESS LATCH

The Address Latch may be written to, under processor control, to store a target address for the breakpoint mechanism. The target address will be applied to, and held, on the reference address (RA) Bus. Gated buffers can apply the data from the RA Bus to the MicroLab I for readback to the processor.

When a value is to be written to the Address Latch, the $\overline{BKREGCS}$ line will be at a low level, enabling U445A and B.

Register FFs U130 and U330 store data from the BD Bus on the trailing, negative-going edge of the WRP (WRite Pulse). The IR/$\overline{W}$ line will be at a low level while the WRP pulse occurs, indicating that a Bus write cycle is occurring. A positive-going pulse on the IR/$\overline{W}$ line (indicating a Bus read cycle) will activate U445B, whose output will turn on buffers U140 and U340. These buffers apply data from the breakpoint address latch to the BD Bus, to allow readback of the breakpoint reference address.

A low on the $\overline{INTRES}$ line (at power-up or when the Microlab I Reset button is pressed) will clear FFs U130 and U330.

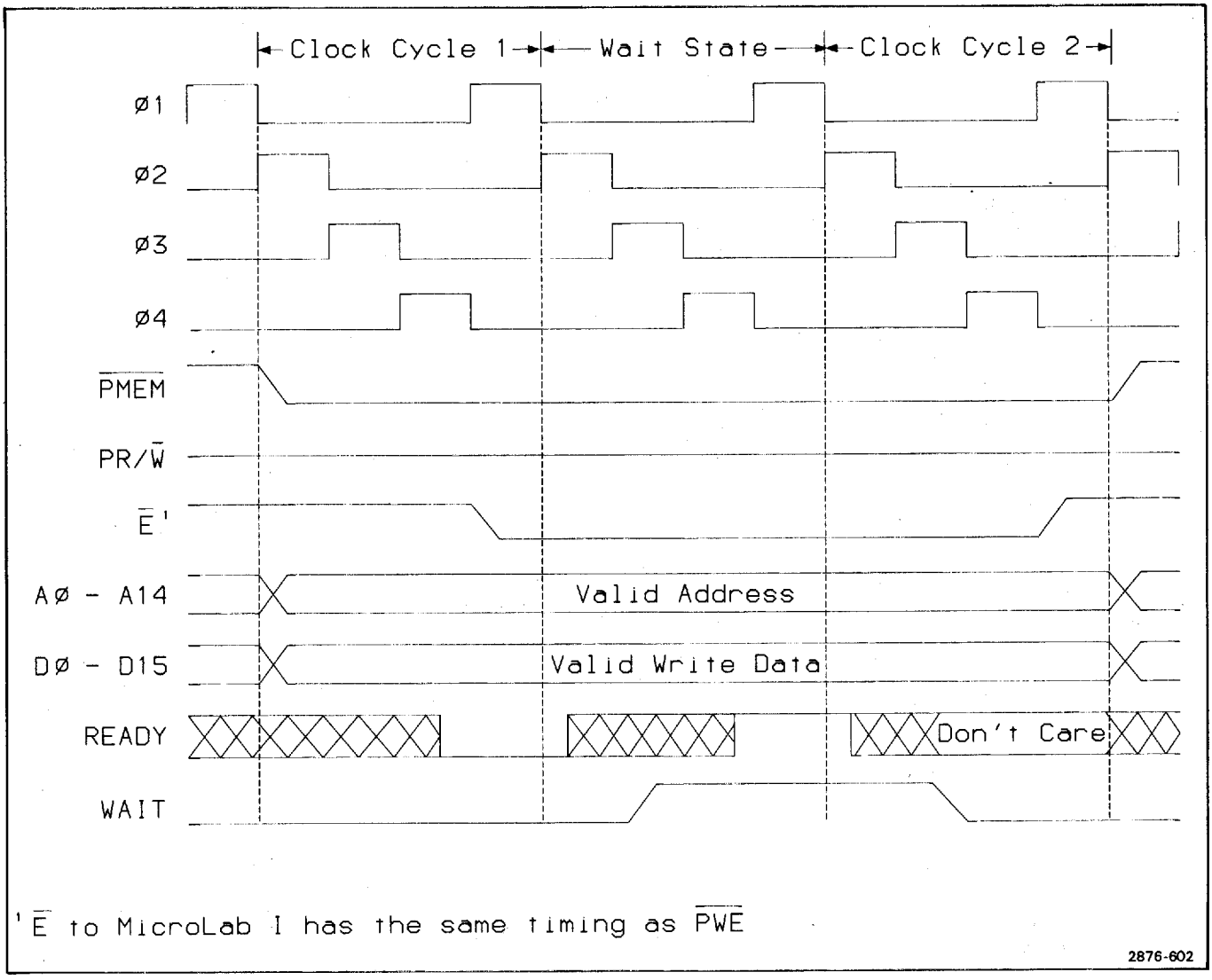


Figure 6-3. Timing of bus enable ($\overline{E}$) signal for MicroLab I during a write cycle.

ADDRESS COMPARATORS

The Address Comparators receive 15 bits of data from the RA and WA Buses and "decide" whether the data (addresses) on the WA Bus is greater than, equal to, or less than the Data on the RA Bus (breakpoint target address). Comparators U230, U240 and U250 compare the lowest five, middle five, and highest five bits of the address Bus with the corresponding bits of the RA Bus, respectively. The outputs of U230, U240 and U250 go to comparator U260 and inverter U160, which will produce a low level on the $\overline{\text{DET ADHI}}$, $\overline{\text{DET ADEQ}}$ or $\overline{\text{DET ADLO}}$ line to show the relation of the WA Bus data to the RA Bus data.

INTERRUPT CONTROL

The Interrupt Control circuit produces the ICØ, IC1, IC2, IC3, $\overline{\text{RSTCIB}}$, READY and $\overline{\text{LOAD}}$ signals for the 7854. The Interrupt Control circuit consists of FF U530A, priority encoder U210, U435A and U170A.

When clocked by the BKINT pulse, FF U530A will produce a low level on its $\overline{Q}$ output. A low level on $\overline{\text{INTRES}}$ or $\overline{\text{BKDATA}}$ will reset U530A, causing its output to be a high level.

Priority encoder U210 produces the ICØ, IC1, IC2 and IC3 signals. The ICØ line will be at a low level when any of the inputs to U210 is low. When the $\overline{\text{SPECIAL}}$ line is at a low level, the IC1, IC2, and IC3 lines will be at low levels, encoding interrupt priority level Ø. When FF U530A's output is at a low level and the $\overline{\text{SPECIAL}}$ line is at a high level, the IC1 and IC3 lines will be at low levels and the IC2 line will be at a high level, encoding interrupt priority level 2.

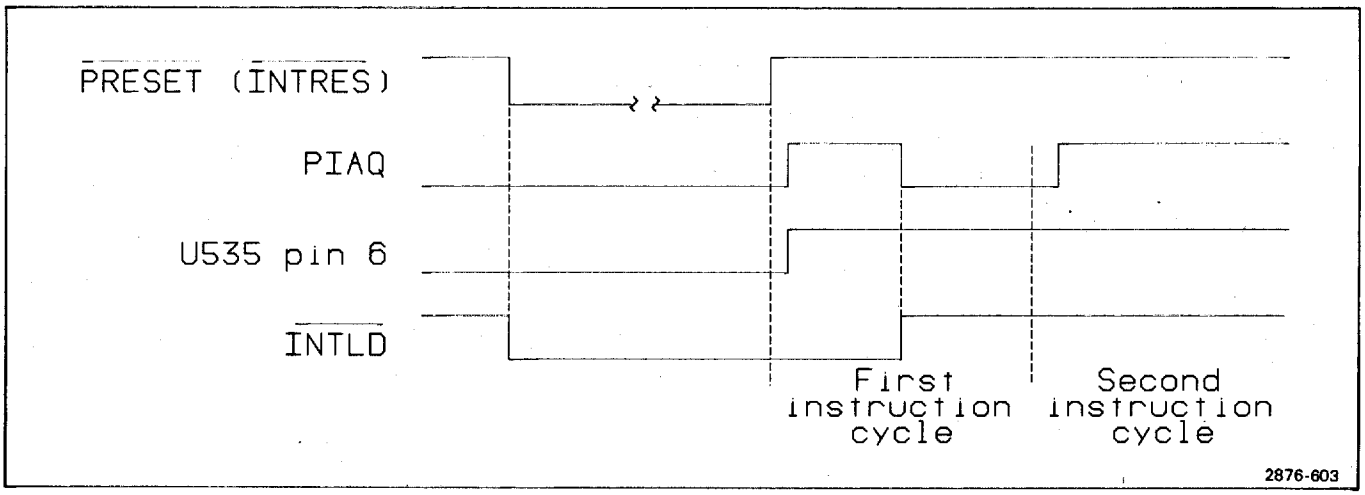


Figure 6-4. Timing of INTLD and its constituent signals.

When the IREQ line is at a low level and U530A's output and the SPECIAL line are at high levels, the IC1 line will be at a low level and the IC2 and IC3 lines will be at high levels, encoding interrupt priority level 3.

Buffer U170A passes the RESET signal from the MicroLab I to the 7854 as RSTCIB. The INTRDY and INTLD signals, from diagram 2, go to the 7854 as READY and LOAD, respectively.

4 BREAKPOINT DATA LATCH & CONTROL

The Breakpoint Data Latch & Control circuitry consists of the Control Register, which determines the operational mode of the Diagnostic Interface circuitry, the Breakpoint Interrupt Generator and the Breakpoint Data Latch.

CONTROL REGISTER

The Control Register is an eight-bit register which may be written to and read back under program control. This register has the following functions and control bits:

Breakpoint mode control (bits 0, 1, 2, 3)	Enables breakpoint mechanism, determines breakpoint mode and breakpoint qualifiers.
PROMBK (bit 6)	Selects which bank of PROM 1 (U120 or U225) will be activated.
RAM1EN (bit 7)	Enables or disables the RAM memory located from 9800 to 9FFF.

The Control Register consists of octal FF U350 and gated buffer U360.

A log-logic level on the CTREGCS line, via U440D, will enable U445D and U460B so that the Control Register can operate. A positive-going pulse on the WRP line will activate U460B. The positive-going, trailing edge of U460B's output will clock Data into FF U350. The IR/W line will be at a low level while the WRP pulse occurs. A positive-going pulse on IR/W will activate U445D, whose output will turn on buffer U360. Buffer U360 will apply data from FF U350 to the BD Bus to allow readback of the control word.

A low level on the INTRES (reset) line will clear FF U350.

BREAKPOINT INTERRUPT GENERATOR

The Breakpoint Interrupt Generator (BIG) produces the BKINT signal, which clocks data from the BD Bus into the Breakpoint Data Latch and generates a BKINT signal. The BIG consists of multiplexers U270 and U280; gated buffer U170B; gates U380D, U560C and D; and buffer U520C.

Bits 0 and 1 of the Control Register are qualifying bits that cause multiplexer U270 to select one of four inputs as its output. The FETCH, IR/W, and READ inputs to U270 qualify the breakpoint so that it will occur only during a fetch, write, or read operation, respectively. The fourth input (ground) allows a breakpoint on any type of bus cycle. A low level on the selected input will cause U270 to turn on buffer U170B.

Bits 2 and 3 of the Control Register cause multiplexer U280 to select one of its four inputs as its output. A low level on the selected input will cause U280 to produce a

low level output. The $\overline{\text{PHASE 4}}$ line is used to synchronize the BKINT signal to ensure correct timing for the 7854 Microprocessor Board. The meaning of the four inputs to U280 are as follows: IC∅, no breakpoint; IC1, breakpoint at data equal; IC2 and IC3 will cause breakpoints at data high or data low when qualified by OSMEM or WA14, respectively. This indicates that the less-than address breakpoint will not function for Bus addresses less than 8000; and the greater-than address breakpoint will not function on addresses corresponding to devices in the MicroLab I mainframe or on the 067-0911-XX Diagnostic Test Interface.

BREAKPOINT DATA LATCH

The Breakpoint Data Latch (BDL) will store data from the BD bus when it receives the BKINT signal, thus saving the data on the bus when the BKINT occurred. A low level on the $\overline{\text{BKDATA}}$ line will cause the BDL to apply its data to the BD Bus for readback by the processor.

TEST PROCESSOR BOARD

The A2 Test Processor Board operates with the A3 Interface Board (in the MicroLab I) to let the diagnostic system test itself. The Test Processor consists of a microprocesor, U310; two PROMs, U200 and U300; and a clock generator, U520.

The A2 Test Processor Board simulates the Microprocessor Board of the 7854 Oscilloscope. Microprocessor U310 exchanges data with the A3 Interface Board, and requests data from PROMs U200 and U300. PROMs U200 and U300 contain the low memory-interrupt vectors needed to perform the self-test of the Diagnostic Interface and the MicroLab I system.

CABLE TERMINATION BOARD

The A1 Cable Termination Board Connects the A3 Interface Board to P130 of the 7854 MPU Board. The A1 Cable Termination Board consists of four buffers (for data on the address and control buses) and two transceivers for the data bus.

THE 067-0911-00 SELF TEST

The Self Test command provides a routine that verifies that the 3 boards of the 067-0911-00 Diagnostic Test Interface are functional and are interacting properly with the MicroLab I mainframe. This verification assures that errors encountered when using any of the Diagnostic or Debug/Utility commands described in Section 4, Command Dictionary, are indeed problems in the 7854 under test.

067-0911-00 POWER UP SEQUENCE

The following power-up tests are part of the Self Test and are automatically invoked whenever power is applied to the 911/MicroLab I system. The following subtests are run each time on power-up:

RAM
ROM
INTERFACE CONTROL REGISTERS
MASKABLE RAM
ROM ID

These tests are run in sequence and, if an error is detected, the appropriate error code (as described later in this section) is displayed on both the MicroLab I front panel LED readout and on the terminal screen. Exit from the power-up tests is done through one of three paths:

1. If none of the subtests reports an error, the message "NO TEST SYSTEM FAULTS DETECTED" is displayed on the terminal screen, followed by an operating system command prompt.

2. If the ROM ID subtest fails (ERROR 43), the power-up test branches immediately into the ROM Signature Analysis routine, which is equivalent to invoking the RS command. See the Command Dictionary, Section 4 and the Rom Signature flowchart in Section 3 for further information.

3. If any of the other tests fail, the appropriate error message is displayed on the terminal screen, followed by the message "**067-0911-00 FAULTS DETECTED" and "ERR-PRESS C".

If an error is encountered, system command execution will halt until the operator presses the terminal keyboard C key. This delay is included to ensure that the operator is aware of the error condition and to allow him the option of continuing despite the error. Once he presses the terminal C key, in response to the prompt, the system will, if capable of doing so, issue an ordinary operating system command prompt.

HOW TO USE THE SELF TEST

The Self Test should be run each time the 067-0911-00 Diagnostic Test Interface is installed into the MicroLab I mainframe to ensure proper interconnection of all parts. It should also be run when an error is suspect in the MicroLab I or the 067-0911-00 Diagnostic Test Interface itself (nothing seems to work).

The Self Test is invoked by typing ST <CR> on the system terminal when connected as shown in the setup figure at the top of the Self Test flowchart in Section 2, Test Procedures. In addition, the Self Test will run when the 067-0911-00 Cable Termination board is connected to the MPU board of a turned-on 7854 Oscilloscope (assuming MPU board is functional). This second configuration is not advised however, as errors may be indicated in the 067-0911-00 when in actuality, the 7854 is at fault.

Once the test equipment is properly setup and the Self Test command is invoked, the test proceeds as given on the Self Test flowchart in Section 2, Test Procedures. A functional description of the individual subtest follows:

RAM SUBTEST

The RAM subtest verifies functionality of the MicroLab I RAM between E400 (hex) and E7FF (hex). This is done by first writing alternating 1's and 0's to each memory location, reading the data back from each location and comparing the data to what it should be. After this data integrity test, Self Test routine writes each address within the Ram block to that location as data. It then reads back this data and compares it to what it should be, verifying the integrity of each address.

A failure in either phase of this test results in the messages "**ERROR 20" and "ERR-PRESS C" displayed on the terminal. Pressing the C key on the terminal at this point advances the Self Test to the next subroutine.

ROM SUBTEST

This subtest verifies the four EPROM chips on the 067-0911-00 Test Interface board by calculating a checksum on each and comparing the results to known good values. A failure results in "**ERROR 29" and one or more of the following being displayed on the display terminal:

"U120-ROM-ERR", "U220-ROM-ERR", "U225-ROM-ERR" or "U320-ROM-ERR". These error messages indicate the faulty EPROM(s).

INTERFACE SUBTEST

This subtest performs write/read checking of the 067-0911-00 Test Interface Board breakpoint address register and the interface control register. The registers are written with all bit patterns not involving the PROM bank switch bit (which can cause TEK-DCL to fail if changed in other than very specific conditions) and read back as required.

A failure in either register results in the message "**ERROR 21" and "ERR-PRESS C" displayed on the terminal screen. Pressing the C key on the terminal at this point advances the Self Test to the next subroutine.

MASKABLE RAM SUBTEST

This subtest checks the MicroLab I RAM addresses between 9800 (hex) and 9FFF (hex) and is enabled through the interface control register. (Because of addressing conflicts, this subtest is automatically skipped if the 067-0911-00 Cable Termination board is connected to a 7854 Oscilloscope with the standard ROM board installed.)

A failure in this test results in the message "**ERROR 22" and "ERR-PRESS C" displayed on the terminal screen. Pressing the C key on the terminal at this point advances the Self Test to the next subroutine.

BREAKPOINT SUBTEST

This subtest checks the 067-0911-00 Test Interface Board breakpoint mechanism for operation in the read only, write only, fetch only, and any access modes by setting appropriate breakpoint conditions and accessing memory at the target addresses to detect breakpoint operation.

A failure in this test results in the message "**ERROR 23" and "ERR-PRESS C" displayed on the terminal screen. Pressing the C key on the terminal at this point advances the Self Test to the next subroutine.

ROM IDENTITY SUBTEST

This subtest checks the low address ROM space in which the system interrupt vectors are stored. The routine detects the use of the following in the test configurations and initializes the subtest accordingly: 7854 Oscilloscope ROM board, 067-0961-00 Diagnostic Memory board, or the 911 Test Processor board. If the system interrupt vectors are not correct, the interrupt driven TEK-DCL operating system is not able to receive commands from the terminal keyboard.

A failure in this test results in the message "**ERROR 43" displayed on the terminal screen.

KEYBOARD SUBTEST

This subtest checks the MicroLab I front-panel keyboard interface. It requires operator intervention in that the operator must press the front-panel keys in the following order: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, DEC, INC, LOAD ADDRESS, LOAD DATA, SHIFT, GO, and AUTO.

If an invalid key code is received during this sequence or if the operator violates the sequence, the message "**ERROR 28" is displayed on the terminal screen.

RS232 INTERFACE SUBTEST

This subtest allows the operator to check operation of the RS232 interface and the Terminal. Test entry is indicated by the message "RS232 - PRESS (GO)" on the terminal screen. In this test, the 911/MicroLab I system simply echos terminal key pressings back to the terminal display.

An error results in the message "**ERROR 24" displayed on the terminal screen. No other error checking is done.

DISPLAY SUBTEST

This subtest allows checking of the MicroLab I front-panel LED display. It is a simple scanning routine that displays all possible characters in each display digit. The operator must detect faults such as missing segments, missing digits, etc.

This routine contains no automatic error checking, but is merely a stimulation routine. Refer to the Self Test flowchart Procedure in Section 2 for character display sequence.

MAINTENANCE

This section of the manual contains information for performing preventive maintenance, troubleshooting, and corrective maintenance for the 067-0911-XX Diagnostic Test Interface.

PREVENTIVE MAINTENANCE

Preventive maintenance, when performed on a regular basis, can prevent or forestall breakdown and may improve the reliability of the assembly. The severity of the environment to which the assembly is subjected will determine the frequency of maintenance.

CLEANING

The assembly should be cleaned as often as operating conditions require. Accumulation of dirt in the assembly can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation. It also provides an electrical conduction path which may result in instrument failure.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this assembly. Use a nonresidue type of cleaner, preferably isopropyl alcohol or totally denatured ethyl alcohol. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

Cleaning the interior of the pod should only be occasionally necessary. The best way to clean the pod interior is to blow off the accumulated dust with dry, low-velocity air (approximately 5 lb/in^2. Remove any dirt which remains with a soft brush or a cloth dampened with a mild detergent and water solution. A cotton-tipped applicator is useful for cleaning in narrow spaces, or for cleaning more delicate circuit components. Refer to Component Removal and Replacement for instructions on disassembly of the pod.

CAUTION

Circuit boards and components must be dry before applying power to prevent damage from electrical arcing.

VISUAL INSPECTION

The assembly should be inspected occasionally for such defects as broken connections, improperly seated semiconductors, damaged circuit boards, and heat-damaged parts. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged parts are found. Overheating usually indicates other trouble in the system; therefore, correcting the cause of overheating is important to prevent recurrence of the damage.

SEMICONDUCTOR CHECKS

Periodic checks of semiconductors are not recommended. The best check of semiconductor performance is actual operation in the assembly. More details on semiconductors are given under Troubleshooting later in this section.

TROUBLESHOOTING

The following information is provided to facilitate troubleshooting of the 067-0911-XX Diagnostic Test Interface. Information contained in other sections of this manual should be used in conjunction with the following data to aid in locating a defective component. An understanding of the circuit operation is helpful in locating troubles. See Section 6, 067-0911-XX theory of Operation, for this information.

TROUBLESHOOTING AIDS

DIAGRAMS

Complete schematic diagrams are given on the pullout pages in Section 10, 067-0911-XX Diagrams and Circuit Board Illustrations. The component number and electrical value of each component in this instrument are shown on these diagrams. (See the first page of the Diagrams and Circuit Board Illustrations section for definitions of the reference designators and symbols used to identify components in this assembly.)

SELF TEST DESCRIPTION

The Self Test description contained in Section 7, the 067-0911-XX Self Test, describes the diagnostic command for verifying the functionality of the 067-0911-XX hardware and firmware.

067-0911-XX SELF TEST PROCEDURE

This is a flowcharted procedure for troubleshooting the 067-0911-XX Diagnostic Test Interface, and is located in volume 2 of the test procedures manuals.

SIGNATURE TABLES

Part of the signature tables located behind the Signature Tables tab pertain to Troubleshooting the 067-0911-XX and should be used in conjunction with the flowcharted 067-0911-XX Self Test Procedure mentioned above.

CIRCUIT BOARD ILLUSTRATIONS

To aid in locating circuit components, a circuit board illustration is provided on the back of the pullout page facing the first schematic diagram associated with that board. Each circuit board illustration is arranged in a grid locator with a grid index to facilitate rapid location of components contained in the schematic diagrams.

COMPONENT COLOR CODING

The assembly contains brown composition resistors, some metal-film resistors, and some wire-wound resistors. The resistance values of wire-wound resistors are usually printed on the component body. The resistance values of composition resistors and metal-film resistors are color coded on the components using the EIR color code (some metal-film resistors may have the value printed on the body). The color code is read starting with the stripe nearest the end of the resistor. Composition resistors have four stripes, which consist of two significant figures, a multiplier, and a tolerance value (see Fig. 8-1). Metal-film resistors have five stripes consisting of three significant figures, a multiplier, and a tolerance value.

The values of the small electrolytics are marked on the side of the component body. The molded rectangular epoxy capacitors used in the assembly are marked with the manufacturer's identification and capacitance value.

The cathode end of glass-encased diodes is indicated by a stripe, a series of stripes, or a dot. The cathode and anode ends of metal-encased diodes can be identified by the diode symbol marked on the body.

SEMICONDUCTOR LEAD CONFIGURATION

Lead configurations for semiconductor devices used in this assembly are shown in Figure 8-2.

STATIC-SENSITIVE DEVICES

CAUTION

Static discharge can damage any semiconductor component in this assembly..

This assembly contains electrical components that are susceptible to damage from static discharge. See Table 8-1 for relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

TABLE 8-1
Relative Susceptiliby to Damage from Static Discharge

Semiconductor Classes	Relative Susceptibility Levels[1]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs (most sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-Frequency bipolar transistors	5
JFETs	6
Linear Microcircuits	7
Low-power Schottky TTL	8
TTL (least sensitive)	9

[1] **Voltage equivalent for levels.**

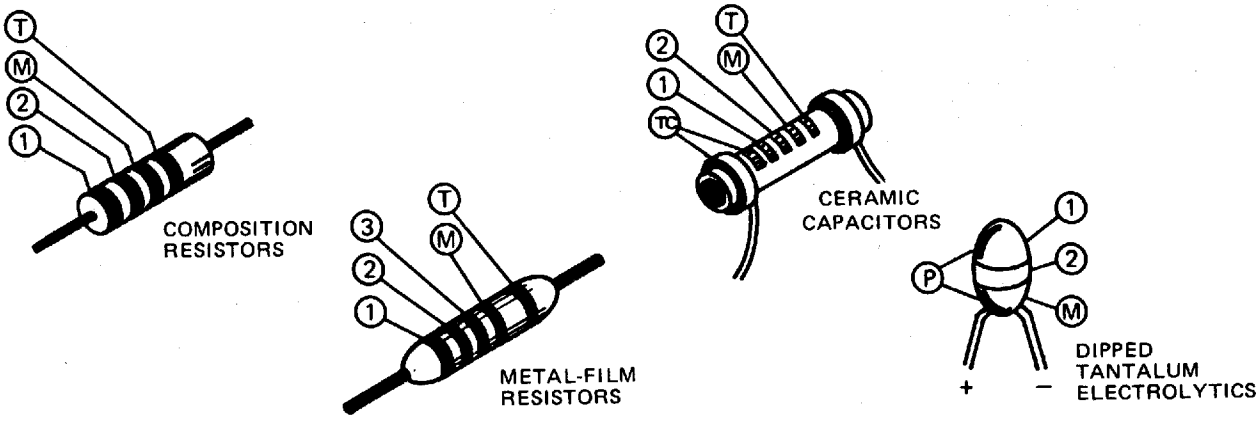
1 = 100 to 500 V
2 = 200 to 500 V
3 = 250V
4 = 500 V
5 = 400 to 600 V
6 = 600 to 800 V
7 = 400 to 1000 V (est.)
8 = 900 V
9 = 1200 V

(Voltage discharged from a 100 pF capacitor through a resistance of 100 ohms).

COLOR CODE

① ② and ③ - 1ST, 2ND, AND 3RD SIGNIFICANT FIGS.
Ⓜ - MULTIPLIER Ⓣ - TOLERANCE;
Ⓣⓒ - TEMPERATURE COEFFICIENT.

Ⓣ AND/OR Ⓣⓒ COLOR CODE MAY NOT BE PRESENT ON SOME CAPACITORS;
Ⓟ - POLARITY AND VOLTAGE RATING



COLOR	SIGNIFICANT FIGURES	RESISTORS		CAPACITORS			DIPPED TANTALUM VOLTAGE RATING
		MULTIPLIER (OHMS)	TOLERANCE	MULTIPLIER (pF)	TOLERANCE		
					OVER 10pF	UNDER 10pF	
BLACK	0	1	---	1	±20%	± 2pF	4VDC
BROWN	1	10	±1%	10	±1%	±0.1pF	6VDC
RED	2	10^2 or 100	±2%	10^2or 100	±2%	---	10VDC
ORANGE	3	10^3or 1 K	±3%	10^3 or 1000	±3%	---	15VDC
YELLOW	4	10^4 or 10K	±4%	10^4 or 10,000	+100% −0%	---	20VDC
GREEN	5	10^5 or 100 K	±1/2%	10^5or 100,000	±5%	±0.5pF	25VDC
BLUE	6	10^6 or 1 M	±1/4%	10^6 or 1,000,000	---	---	35VDC
VIOLET	7	---	±1/10%	10^7 or 10,000,000	---	---	50VDC
GRAY	8	---	---	10^{-2} or 0.01	+80% −20%	±0.25pF	---
WHITE	9	---	---	10^{-1} or 0.1	±10%	±1pF	3VDC
GOLD	---	10^{-1} or 0.1	±5%	---	---	---	---
SILVER	---	10^{-2} or 0.01	±10%	---	---	---	---
NONE	---	---	±20%	---	±10%	±1pF	---

2876-55

Figure 8-1. Color codes for resistors and capacitors.

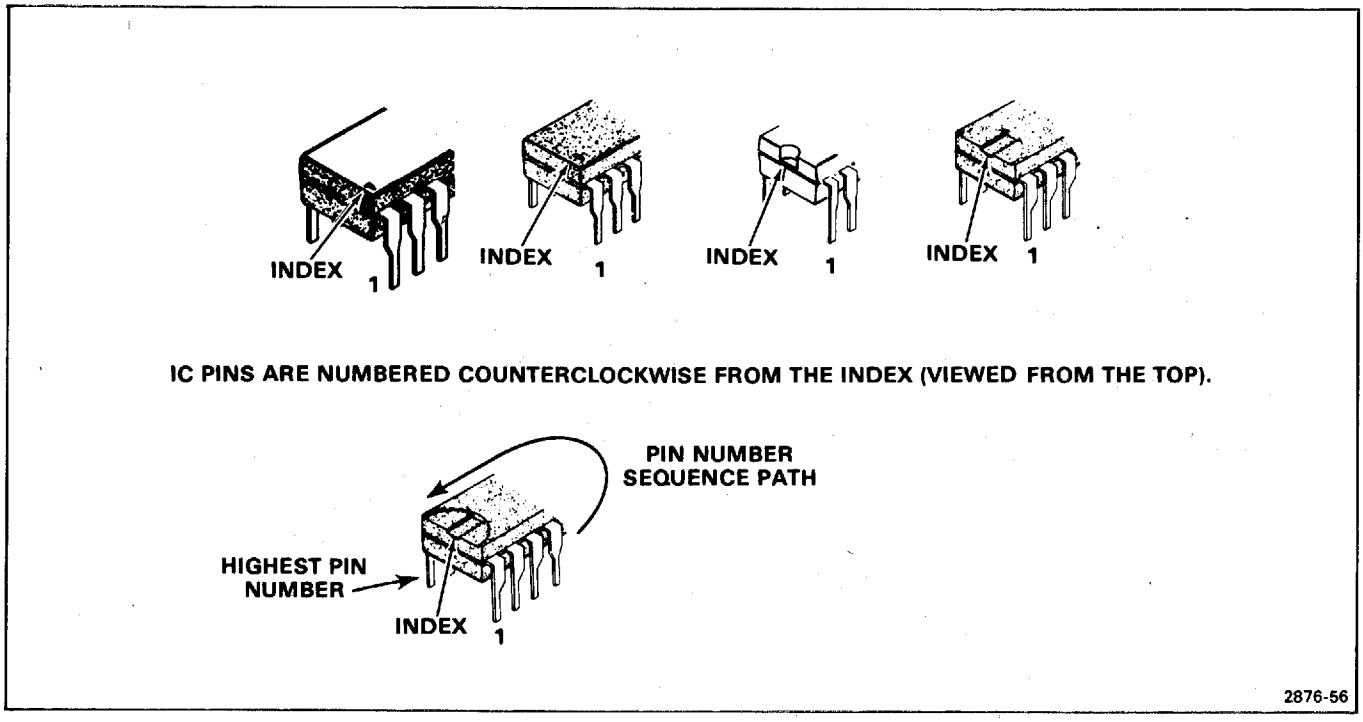


Figure 8-2. Semiconductor lead configuration.

Observe the following precautions to avoid damage.

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive assemblies or components.
3. Discharge the static-voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.
4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
5. Keep the component leads shorted together whenever possible.
6. Pick up components by the body, never by the leads.
7. Do not slide the components over any surface.
8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.
9. Use a soldering iron that is connected to earth ground.
10. Use only special antistatic suction-type desoldering tools.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and assembly repair. Special techniques are required to replace components in the 067-0911-XX Diagnostic Test Interface.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, you should be able to obtain many of the standard electronic components from a local commercial source in your area. Before you purchase or order a part from a source other than Tektronix, Inc., please check the electrical parts list for the proper value, rating, tolerance and description.

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Some parts are manufactured or selected by Tektronix, Inc. to satisfy particular requirements, or are manufactured for Tektronix, Inc. to our specifications. Most of the mechanical parts used in this instrument have been manufactured by Tektronix, Inc. To determine manufacturer of parts, refer to Parts List, Cross Index Mfr. Code Number to Manufacturer.

When ordering replacement parts from Tektronix, Inc., include the following information:

1. Instrument type.
2. Instrument serial number.
3. A description of the part (if electrical, include circuit number).
4. Tektronix part number.

SOLDERING TECHNIQUES

WARNING

To avoid electric-shock hazard, disconnect the instrument from the power source before soldering.

The reliability and accuracy of this assembly can be maintained only if proper soldering techniques are used when repairing or replacing parts.

The desoldering and removal of parts is especially critical and should be done only with a vacuum solder extractor; further, one approved by a Tektronix Inc., Service Center.

Use wire solder with rosin core, 63% tin, 37% lead. Contact your local Tektronix Inc. representative or field office for approved solders.

Several multilayer circuit boards are used in this system. Conductive paths between the top and bottom board layers may connect with one or any number of inner layers. Once this inner conductive path is broken (due mainly to poor soldering practices) between the top and bottom layer, the board is unuseable and must be replaced. Damage can void warranty.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum type desoldering equipment, should attempt repair of any board in this system.

When soldering on circuit boards or small wiring, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron can cause the etched circuit wiring to separate from the board base material, and melt the insulation from small wiring. Always keep the soldering-iron tip properly tinned to ensure the best heat transfer to the solder joint. Apply only enough heat to make a good solder joint. To protect heat-sensitive components, hold the component lead with a pair of long-nose pliers between the component body and the solder joint.

The following technique should be used to replace a component on any of the circuit boards.

1. Touch the tip of the vacuum desoldering tool directly to the solder to be removed.

CAUTION

Excessive heat can cause the etched circuit wiring to separate from the board base material.

Never allow the solder extractor to remain on the board for more than three (3) seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for multi-pin components) must not be used. Damage can void warranty.

NOTE

Some components are difficult to remove from the circuit boards due to a bend placed in each lead during machine insertion of the component. The purpose of the bent leads is to hold the component in position during a flow-solder manufacturing process which solders all components at once. To make removal of machine inserted components easier, straighten the leads of the component on the back of the circuit board using a small screwdriver or pliers.

When removing multi-pin components i.e., IC's, do not heat adjacent conductors consecutively (see Fig. 8-3). Allow a moment for the circuit board to cool before proceeding to the next pin.

2. Bend the leads of the replacement components to fit the holes in the circuit board. Insert the leads into the holes in the board, or as originally positioned.
3. Touch the iron to the connection and apply enough solder to make a firm solder joint.
4. Cut off any excess lead protruding through the board.
5. Clean the areas around the solder connection with a flux removing solvent. Be careful not to remove information printed on the circuit board.

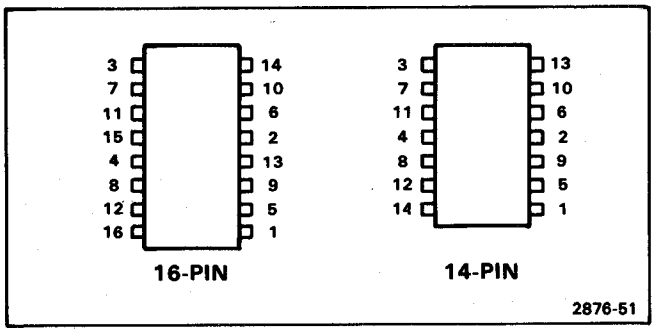

Figure 8-3. Recommended desoldering sequence for multi-pin devices.

COMPONENT REMOVAL AND REPLACEMENT

CAUTION

To avoid component damage, always disconnect the assembly from the power source before removing or replacing components.

The exploded-view drawing associated with the Replaceable Mechanical Parts list (located at the rear of this manual) may be helpful in the disassembly of the A1-Cable Termination board.

CIRCUIT BOARDS

If a circuit board is damaged beyond repair, replace the entire board assembly. Part numbers are given in Section 9, Replaceable Electrical Parts, for completely wired boards.

How to Remove the Cable Termination Board (A1)

1. Remove the three small nuts securing the gray-ribbon cable side of the Pod housing.
2. Remove the two screws on either side of the multi-pin connector, and lift away the component side of the Pod housing.
3. Remove the two board-mounting screws on either side of the gray-ribbon cable.
4. To replace the Cable Termination board, reverse the order of removal.

SEMICONDUCTORS

Semiconductors should not be replaced unless actually defective. If removed from their sockets during routine maintenance, return them to their original sockets. Unnecessary replacement of semiconductors may affect the adjustment of the instrument. When semiconductors are replaced, check the operation of circuits which may be affected.

CAUTION

To avoid component damage always disconnect the assembly from the power source before removing or replacing components.

Replacement semiconductors should be of the original type or a direct replacement. Lead configurations of the semiconductors used in this instrument are shown in Figure 8-2.

CAUTION

Do not remove stickers affixed to the top of EPROM's. Removal of this sticker will allow light into the chip, and may cause partial erasure of its data.

An extracting tool should be used to remove the in-line integrated circuits to prevent damaging the pins. This tool is available from Tektronix, Inc,; order Tektronix Part 003-0619-00. If an extracting tool is not available, use care to avoid damaging the pins. Pull slowly and evenly on both ends of the integrated circuit. Try to avoid one end disengaging from the socket before the other end.

SOFTWARE/FIRMWARE PERFORMANCE REPORT

If errors in documentation of normal instrument operation occur, the error report form (provided at the rear of this manual) should be completed and returned to Tektronix, Inc.

Instructions for completing the Software/Firmware Performance Report are placed just before the report form, which may be reproduced.

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REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix Instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer Index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

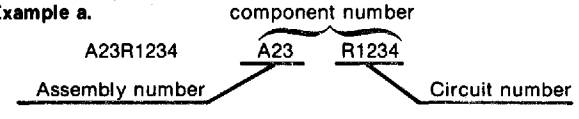
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

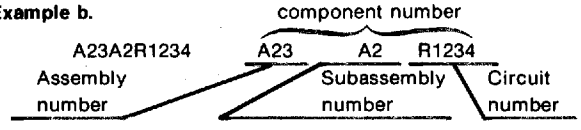
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
88407	BULOVA WATCH CO. INC. ELECTRONICS DIV.	61-20 WOODSIDE AVE	WOODSIDE, NY 11377
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-6317-00			CKT BOARD ASSY:CABLE TERMINATION	80009	670-6317-00
A2	670-6318-00			CKT BOARD ASSY:TEST PROCESSOR	80009	670-6318-00
A3	670-6319-01			CKT BOARD ASSY:INTERFACE	80009	670-6319-01
A1	----- -----			CKT BOARD ASSY:CABLE TERMINATION		
A1C100	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C200	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C300	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C400	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1R100	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A1R200	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A1R201	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A1R600	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A1R601	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A1U100	156-1111-01			MICROCIRCUIT,DI:OCTAL BUS XCVR	80009	156-1111-01
A1U200	156-1111-01			MICROCIRCUIT,DI:OCTAL BUS XCVR	80009	156-1111-01
A1U300	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A1U400	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A1U500	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A1U600	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A2	----- -----			CKT BOARD ASSY:TEST PROCESSOR		
A2C129	290-0106-00			CAP.,FXD,ELCTLT:10UF,+75-10%,15V	56289	30D106G015BA9
A2C200	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C321	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C500	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	72982	8035D9AADC0G150K
A2C521	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2C522	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A2L500	108-0170-01			COIL,RF:FIXED,360NH	80009	108-0170-01
A2R110	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A2R111	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A2R320	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A2R321	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A2R410	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
A2R500	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2U120	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0385-00
A2U200	160-0786-00			MICROCIRCUIT,DI:32 X 8 PROM,PROGRAMMED	80009	160-0786-00
A2U300	160-0784-00			MICROCIRCUIT,DI:32 X 8 PROM,PROGRAMMED	80009	160-0784-00
A2U310	156-0935-00			MICROCIRCUIT,DI:MICROPROCESSOR,16 BIT	80009	156-0935-00
A2U520	156-0993-00			MICROCIRCUIT,INTFC:FOUR PH CLOCK GE/DRIVER	80009	156-0993-00
A2Y520	158-0152-00			XTAL UNIT,QTZ:48.0 MHZ,0.015%	88407	80AX-1232
A3	----- -----			CKT BOARD ASSY:INTERFACE		
A3C110	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C120	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C129	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C130	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C150	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C150	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3C170	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C210	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C225	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C230	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C250	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C260	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C270	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C280	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C300	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C330	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C340	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C350	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C360	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C500	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C520	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C580	290-0219-00			CAP.,FXD,ELCTLT:5UF,+75-10%,25V	56289	30D505G025BA9
A3R210	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
A3R280	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
A3R300	307-0598-00			RES NTWK,FXD FI:7,330 OHM,2%,1.0W	91637	MSP08A01331G
A3R305	307-0594-00			RES NTWK,FXD FI:7,220 OHM,2%,1.0W	91637	CSP08G01221G
A3R400	307-0598-00			RES NTWK,FXD FI:7,330 OHM,2%,1.0W	91637	MSP08A01331G
A3R405	307-0594-00			RES NTWK,FXD FI:7,220 OHM,2%,1.0W	91637	CSP08G01221G
A3R410	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A3R420	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A3R540	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A3U110	156-1111-01			MICROCIRCUIT,DI:OCTAL BUS XCVR	80009	156-1111-01
A3U120	160-0783-00			MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-0783-00
A3U130	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	80009	156-0865-02
A3U140	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A3U150	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A3U160	156-0385-02			MICROCIRCUIT,DI:HEX INVERTED	80009	156-0385-02
A3U170	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A3U200	156-1111-01			MICROCIRCUIT,DI:OCTAL BUS XCVR	80009	156-1111-01
A3U210	156-1176-01			MICROCIRCUIT,DI:8/3 LINE PRIORITY ENCODER	80009	156-1176-01
A3U220	160-0785-00			MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-0785-00
A3U225	160-0787-00			MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-0787-00
A3U230	156-0953-02			MICROCIRCUIT,DI:4 BIT MAGNITUDE CMPRTR	80009	156-0953-02
A3U240	156-0953-02			MICROCIRCUIT,DI:4 BIT MAGNITUDE CMPRTR	80009	156-0953-02
A3U250	156-0953-02			MICROCIRCUIT,DI:4 BIT MAGNITUDE CMPRTR	80009	156-0953-02
A3U260	156-0953-02			MICROCIRCUIT,DI:UDE CMPRTR	80009	156-0953-02
A3U270	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	80009	156-0798-02
A3U280	156-0471-02			MICROCIRCUIT,DI:DUAL 4/1 DATA SEL/MUX	80009	156-0471-02
A3U320	160-0788-00			MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-0788-00
A3U330	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	80009	156-0865-02
A3U340	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A3U350	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	80009	156-0865-02
A3U360	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A3U370	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A3U380	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A3U410	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	80009	156-0464-02
A3U420	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR/DEMUX	80009	156-0541-02
A3U430	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	80009	156-0464-02
A3U435	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	80009	156-0480-02
A3U440	156-0385-02			MICROCIRCUIT,DI:HEX INVERTED	80009	156-0385-02
A3U445	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	80009	156-0382-02

@

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3U460	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	80009	156-0382-02
A3U465	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	80009	156-0465-02
A3U510	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	04713	SN74LS244N OR J
A3U520	156-0385-02			MICROCIRCUIT,DI:HEX INVERTED	80009	156-0385-02
A3U530	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGETRIGGERED FF	80009	SN74LS109AN OR J
A3U535	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGETRIGGERED FF	80009	SN74LS109AN OR J
A3U540	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A3U560	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	80009	156-0479-02

@

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
U120	160-0783-00			MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-0783-00
U200	160-0784-00			MICROCIRCUIT,DI:32 X 8 PROM,PROGRAMMED	80009	160-0784-00
U220	160-0785-00			MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-0785-00
U225	160-0787-00			MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-0787-00
U300	160-0786-00			MICROCIRCUIT,DI:32 X 8 PROM,PROGRAMMED	80009	160-0786-00
U320	160-0788-00			MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-0788-00

@

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

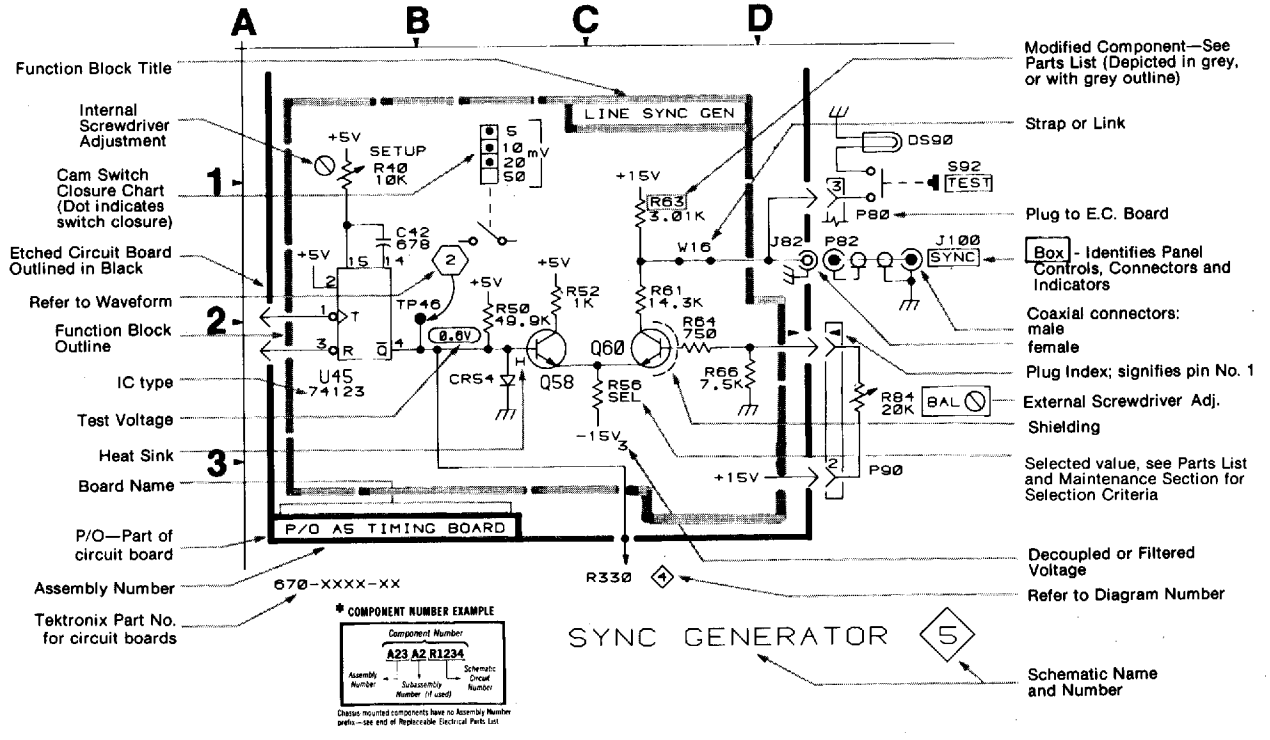
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



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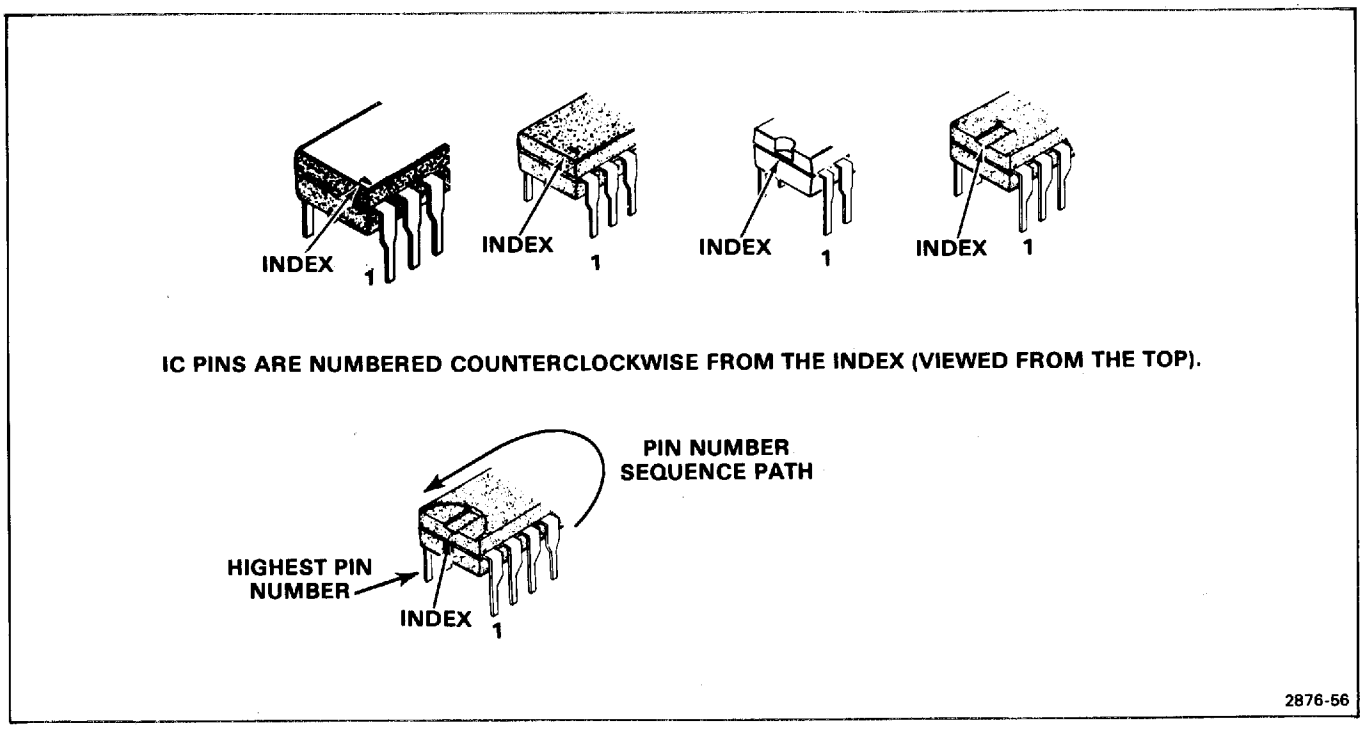

Figure 10-1. Semiconductor Lead Configurations.

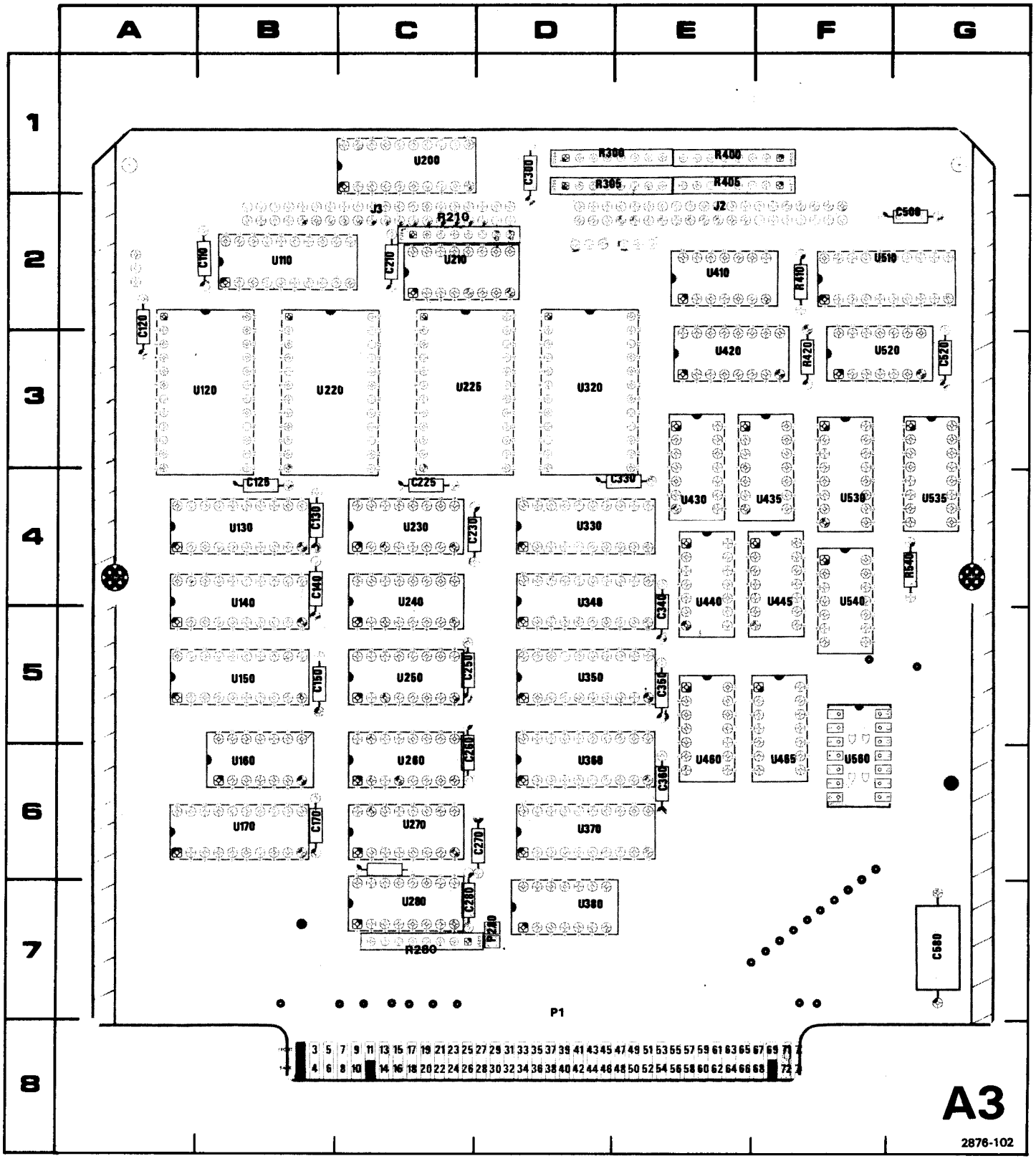

Figure 10-2. A3-Interface circuit board assembly.

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PROM MEMORY DIAGRAM 1

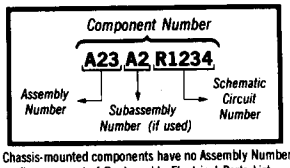
ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J2	A1	E2
J3	G1	C2
R300A	A1	D1
R300B	B2	D1
R300C	A2	D1
R300D	B2	D1
R300E	A2	D1
R300F	B3	D1
R300G	A3	D1
R305A	A1	D1
R305B	B1	D1
R305C	A2	D1
R305D	B2	D1
R305E	A2	D1
R305F	B2	D1
R305G	A3	D1
R400A	B4	E1
R400B	A4	E1
R400C	B4	E1
R400D	A4	E1
R400E	B3	E1
R400F	A3	E1
R400G	B3	E1
R405A	B4	E1
R405B	A4	E1
R405C	B4	E1
R405D	A4	E1
R405E	B3	E1
R405F	A3	E1
R405G	B3	E1
R410	A4	F2
R420	A5	F3
U110	G3	B2
U120	E3	B3
U200	G3	C1
U220	C3	B3
U225	E1	C3
U320	C1	D3

Partial A3 also shown on diagrams 2, 3 and 4.

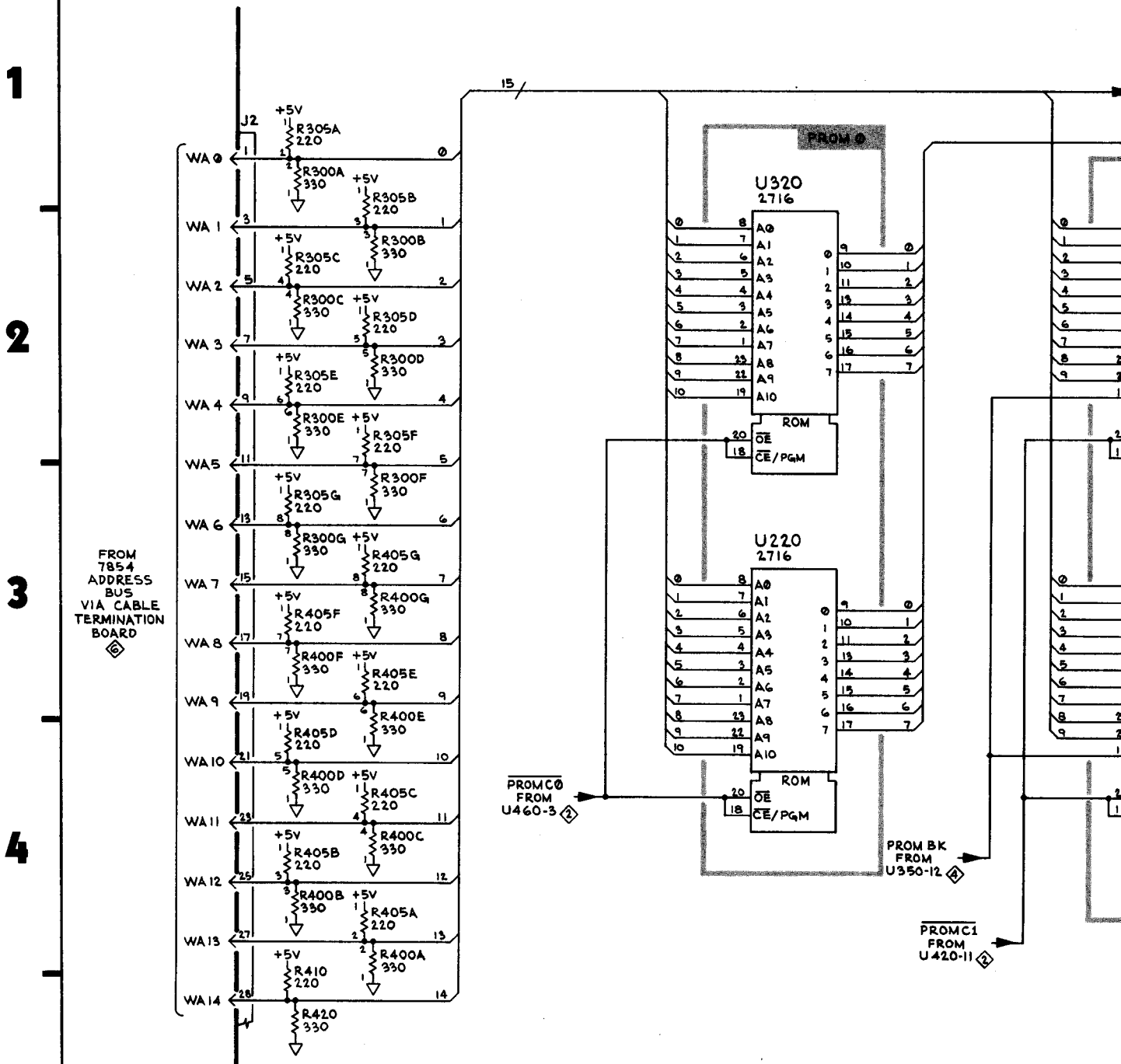
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

A3
2876-102



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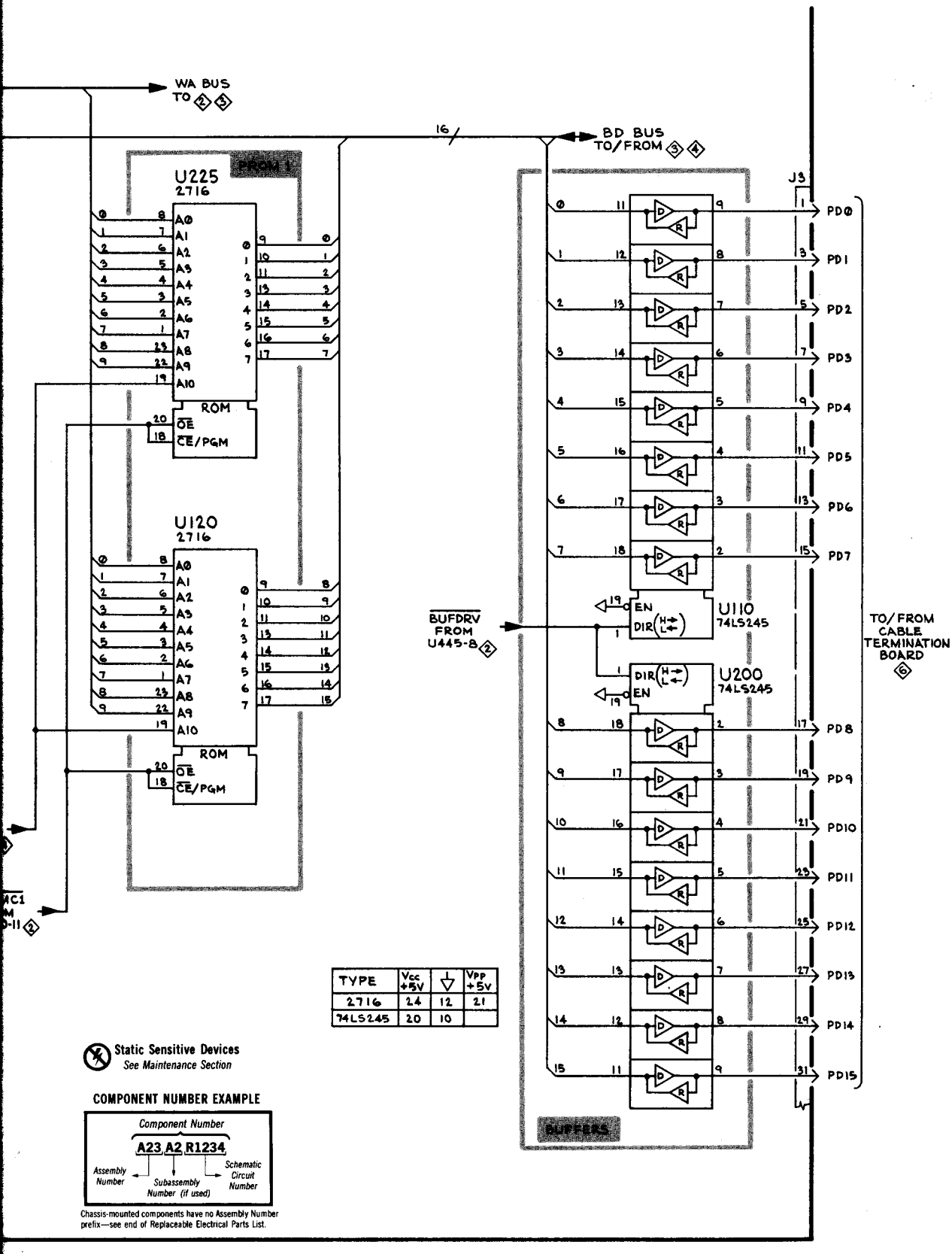


TYPE	Vcc +5V	⏚	VPP +5V
2716	24	12	21
74LS245	20	10	

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

PROM MEMORY 1

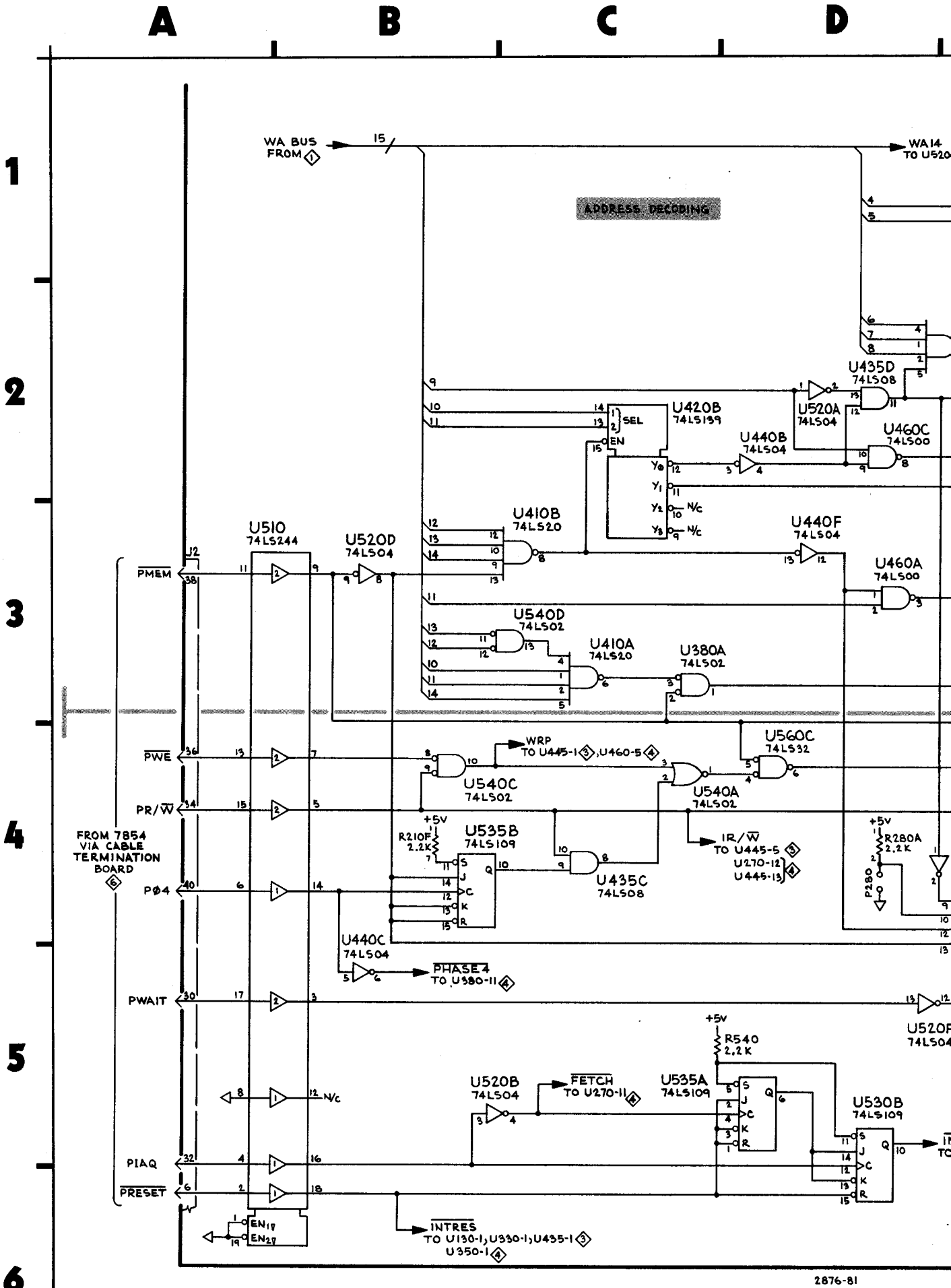
ADDRESS DECODING AND CONTROL DIAGRAM 2

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J2	G3	E2
J3	G3	C2
P1	G2	D8
P1	G4	D8
R210F	B4	C2
R280A	D4	7C
R280B	F3	7C
R540	D5	G4
U160F	G3	B6
U380A	C3	D7
U380B	F4	D7
U380C	G4	D7
U410A	C3	E2
U410B	C3	E2
U420A	E1	E3
U420B	C2	E3
U430A	E2	E4
U430B	E4	E4
U435C	C4	F4
U435D	D2	F4
U440A	E4	E4
U440B	D2	E4
U440C	B4	E4
U440F	D3	E4
U445C	F3	F4
U460A	D3	E6
U460C	D2	E6
U460D	E3	E6
U465	F3	F6
U510	A3	F2
U520A	D2	F3
U520B	B5	F3
U520D	B3	F3
U520E	E4	F3
U520F	D5	F3
U530B	D5	F4
U535A	C5	G4
U535B	B4	G4
U540A	C4	F4
U540B	E5	F4
U540C	B4	F4
U540D	C3	F4
U560A	E5	F6
U560C	D4	F6

Partial A3 also shown on diagrams 1, 3 and 4.

For circuit board illustration see Figure 10-1 on the reverse side of Section 10 Diagrams & Circuit Bd Illustration foldout.



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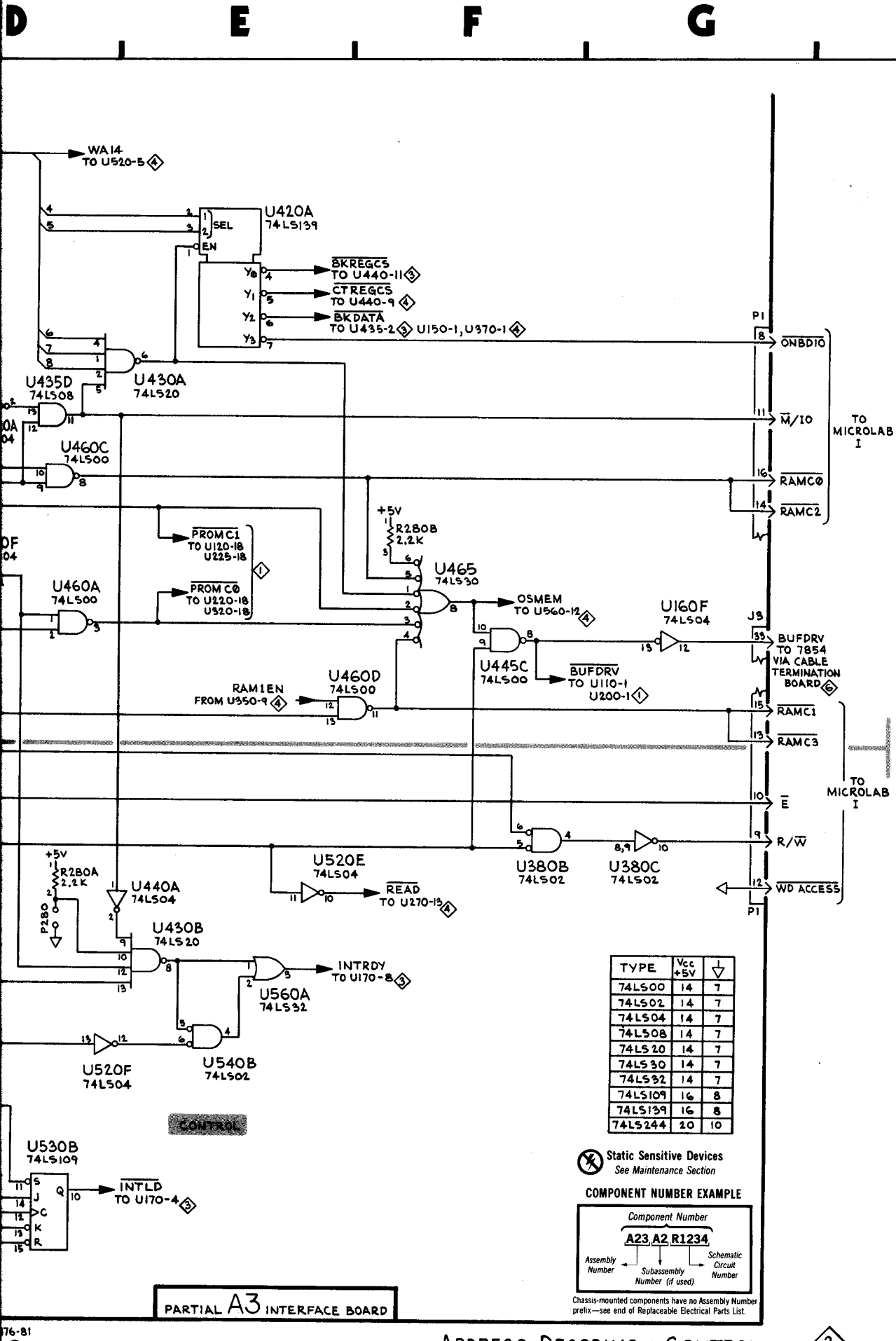

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ADDRESS DECODING & CONTROL 2

BREAKPOINT ADDRESS LATCH AND COMPARATORS DIAGRAM 3

ASSEMBLY A3

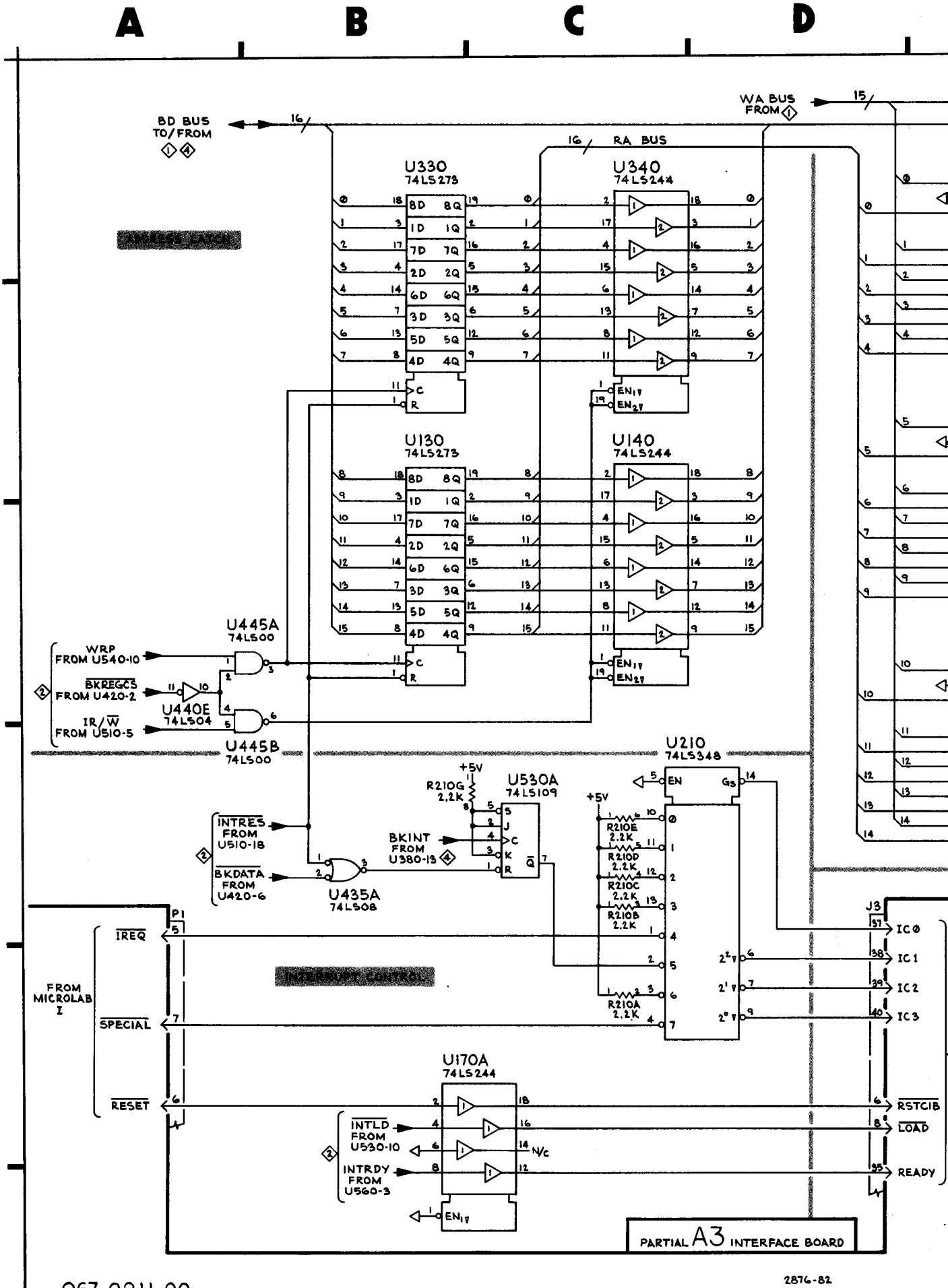
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J3	D5	C2
P1	A4	D8
P1	G1	D8
R210A	C5	C2
R210B	C4	C2
R210C	C4	C2
R210D	C4	C2
R210E	C4	C2
R210G	B4	C2
R280G	E2	7C
U130	B2	B4
U140	C2	B4
U160A	F3	B6
U160B	F3	B6
U160C	F2	B6
U160D	F3	B6
U160E	F4	B6
U170A	B5	B6
U210	C4	C2
U230	E1	C4
U240	E2	C4
U250	E3	C5
U260	F2	C6
U330	B1	D4
U340	C1	D4
U435A	B4	F4
U435B	F4	F4
U440E	A3	E4
U445A	B3	F4
U445B	B4	F4
U530A	C4	F4

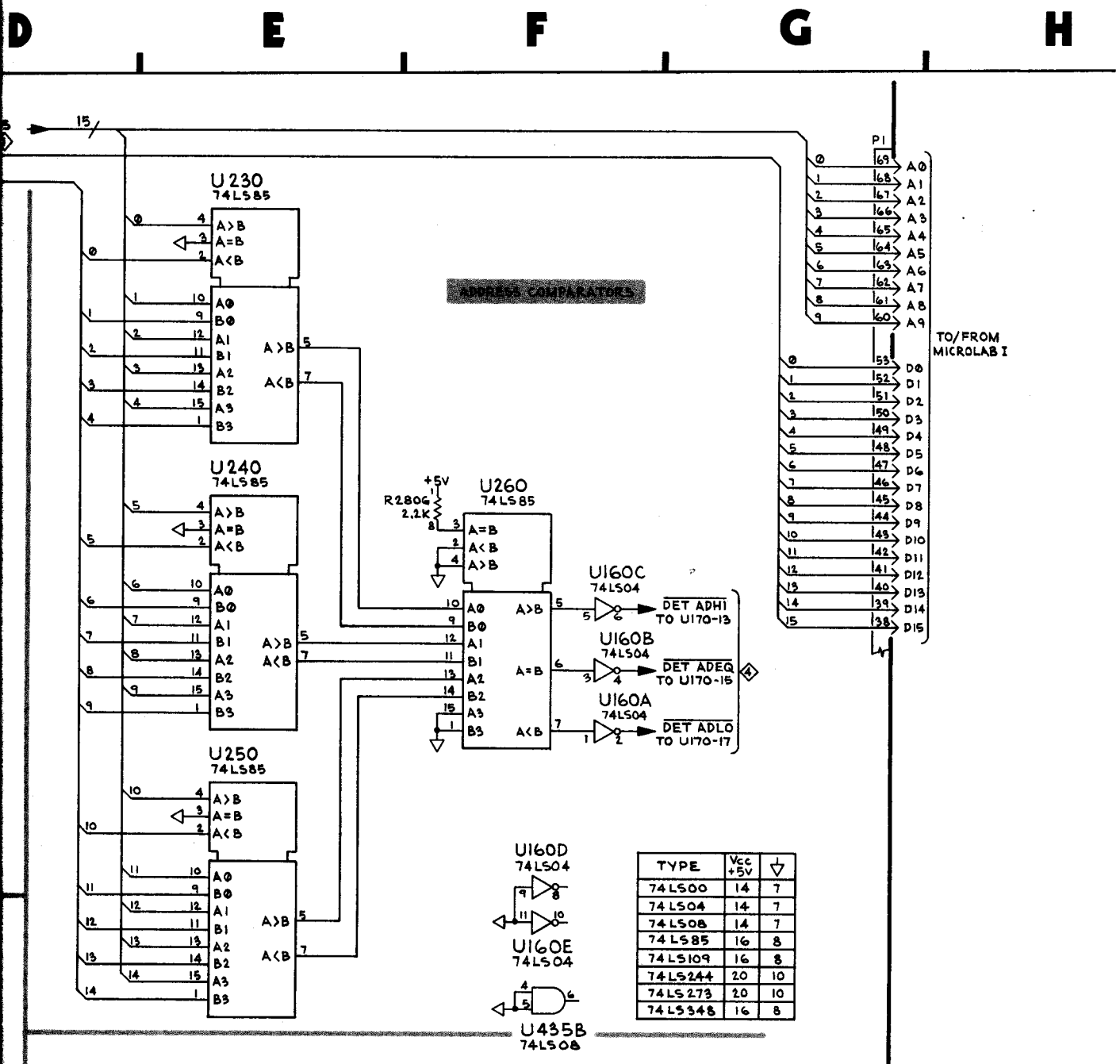
Partial A3 also shown on diagrams 1, 2 and 4.

For circuit board illustration see Figure 10-1 on the reverse side of Section 10 Diagrams & Circuit Bd Illustration foldout.

A3-interface circuit board locator

@

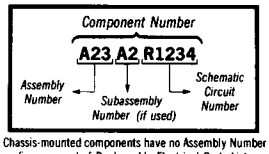

A
B
C
D
1
2
3
4
5
6
BD BUS TO/FROM ① ④
16
WA BUS FROM ①
15
16 RA BUS
U330
74LS273
U340
74LS244
ADDRESS LATCH
U130
74LS273
U140
74LS244
U445A
74LS00
WRP FROM U540-10
BKREGCS FROM U420-2
U440E
74LS04
IR/W FROM U510-5
U445B
74LS00
U210
74LS348
+5V
R210G 2.2K
U530A
74LS109
INTRES FROM U510-18
BKINT FROM U380-13 ④
BKDATA FROM U420-6
U435A
74LS08
R210E 2.2K
R210D 2.2K
R210C 2.2K
R210B 2.2K
R210A 2.2K
P1
IREQ
FROM MICROLAB I
SPECIAL
RESET
INTERRUPT CONTROL
J3
IC0
IC1
IC2
IC3
U170A
74LS244
INTLD FROM U530-10
INTRDY FROM U560-3
N/c
RSTCIB
LOAD
READY
PARTIAL A3 INTERFACE BOARD
067-0911-00
2876-82



TYPE	Vcc +5V	⏚
74LS00	14	7
74LS04	14	7
74LS08	14	7
74LS85	16	8
74LS109	16	8
74LS244	20	10
74LS273	20	10
74LS348	16	8

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

BREAKPOINT ADDRESS LATCH & COMPARATORS

3

876-82

BREAKPOINT DATA LATCH AND CONTROL DIAGRAM 4

ASSEMBLY A3

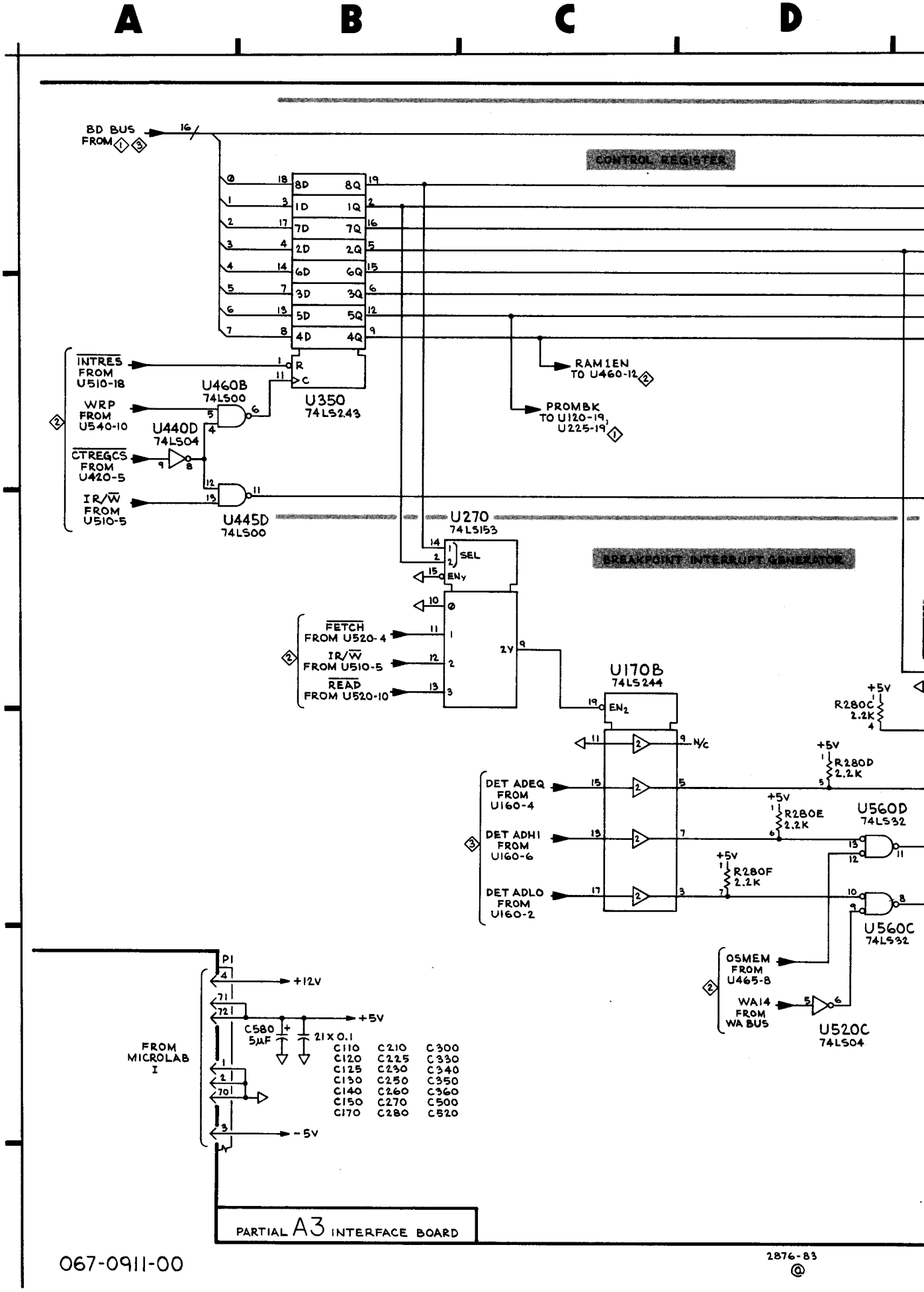
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	B5	B2
C120	B5	A2
C125	B5	B4
C130	B5	B4
C140	B5	B4
C150	B5	B5
C170	B5	B6
C210	B5	C2
C225	B5	C4
C230	B5	C4
C250	B5	C5
C260	B5	C6
C270	B5	D6
C280	B5	C7
C300	B5	D1
C330	B5	E4
C340	B5	E4
C350	B5	E5
C360	B5	E6
C500	B5	G2
C520	B5	G3
C580	B5	G7
J2	G5	E2
J3	G3	C2
P1	A5	D8
R280C	D3	7C
R280D	D4	7C
R280E	D4	7C
R280F	D4	7C
U150	F3	B5
U170B	C3	B6
U270	C3	C6
U280	E3	C7
U350	B2	D5
U360	E2	D6
U370	F1	D6
U380D	F3	D7
U440D	A2	E4
U445D	B3	F4
U460B	A2	E6
U520C	D5	F3
U560C	D5	F6
U560D	D4	F6

Partial A3 also shown on diagrams 1, 2 and 3.

For circuit board illustration see Figure 10-1 on the reverse side of Section 10 Diagrams & Circuit Bd Illustration foldout.

A3-Interface circuit board locator

@


A
B
C
D
1
2
3
4
5
6
BD BUS FROM ◇1 ◇3
16
CONTROL REGISTER
8D 8Q
1D 1Q
7D 7Q
2D 2Q
6D 6Q
3D 3Q
5D 5Q
4D 4Q
INTRES FROM U510-18
R
C
U350 74LS243
RAM1EN TO U460-12 ◇2
PROMBK TO U120-19, U225-19 ◇1
WRP FROM U540-10
U460B 74LS00
U440D 74LS04
CTREGCS FROM U420-5
IR/W FROM U510-5
U445D 74LS00
U270 74LS153
SEL
ENy
BREAKPOINT INTERRUPT GENERATOR
FETCH FROM U520-4
IR/W FROM U510-5
READ FROM U520-10
2Y
U170B 74LS244
EN2
N/c
+5V
R280C 2.2K
R280D 2.2K
R280E 2.2K
R280F 2.2K
DET ADEQ FROM U160-4
DET ADH1 FROM U160-6
DET ADLO FROM U160-2
U560D 74LS32
U560C 74LS32
OSMEM FROM U465-8
WA14 FROM WA BUS
U520C 74LS04
P1
+12V
+5V
-5V
C580 5µF
21 X 0.1
C110 C210 C300
C120 C225 C330
C125 C230 C340
C130 C250 C350
C140 C260 C360
C150 C270 C500
C170 C280 C520
FROM MICROLAB I
PARTIAL A3 INTERFACE BOARD
067-0911-00
2876-83

D E F G H

BREAKPOINT DATA LATCH

16 / BD BUS TO 3

U370
74LS374

U360
74LS244

BKDATA FROM U420-6 2

U150
74LS374

U280
74LS153

U380D
74LS02

PHASE 4 FROM U440-6 2

BKINT TO U530-4 3

U560D
74LS32

U560C
74LS32

U520C
74LS04

+5V
R280C 2.2K
R280D 2.2K
R280E 2.2K

J3

+12V
-5V
+5V
J2

TO CABLE TERMINATION BOARD 6

TYPE	Vcc +5V	⏚
74LS00	14	7
74LS02	14	7
74LS04	14	7
74LS32	14	7
74LS153	16	8
74LS244	20	10
74LS273	20	10
74LS374	20	10

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

76-83
©

BREAKPOINT DATA LATCH & CONTROL 4

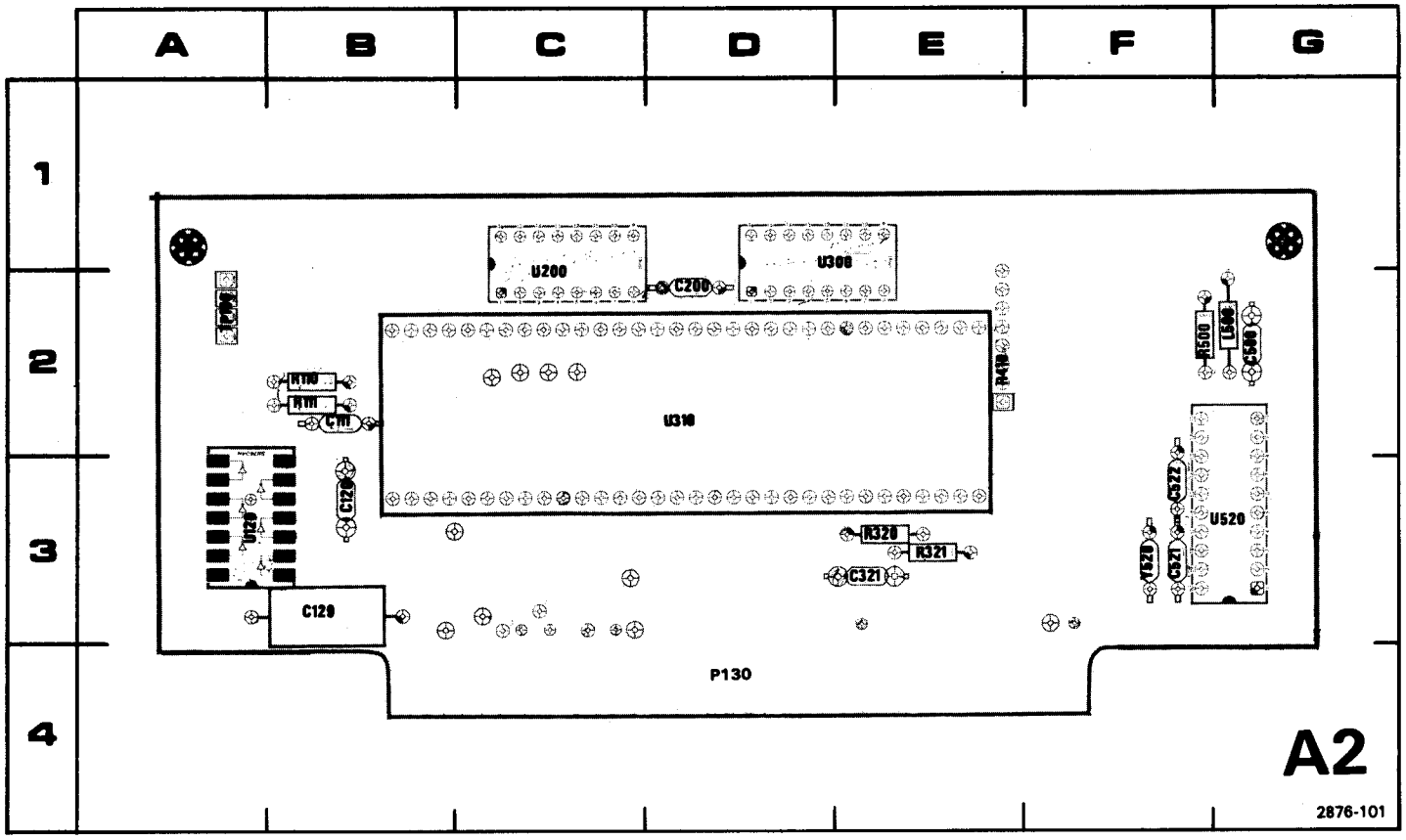
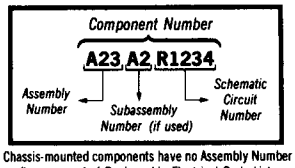


Figure 10-3. A2-Test Processor circuit board assembly.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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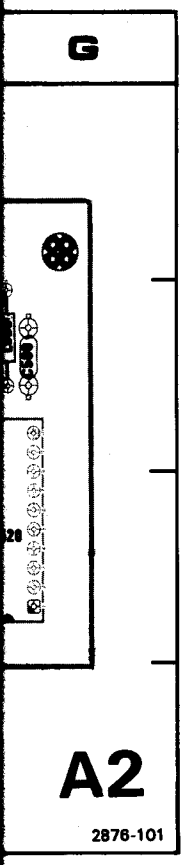
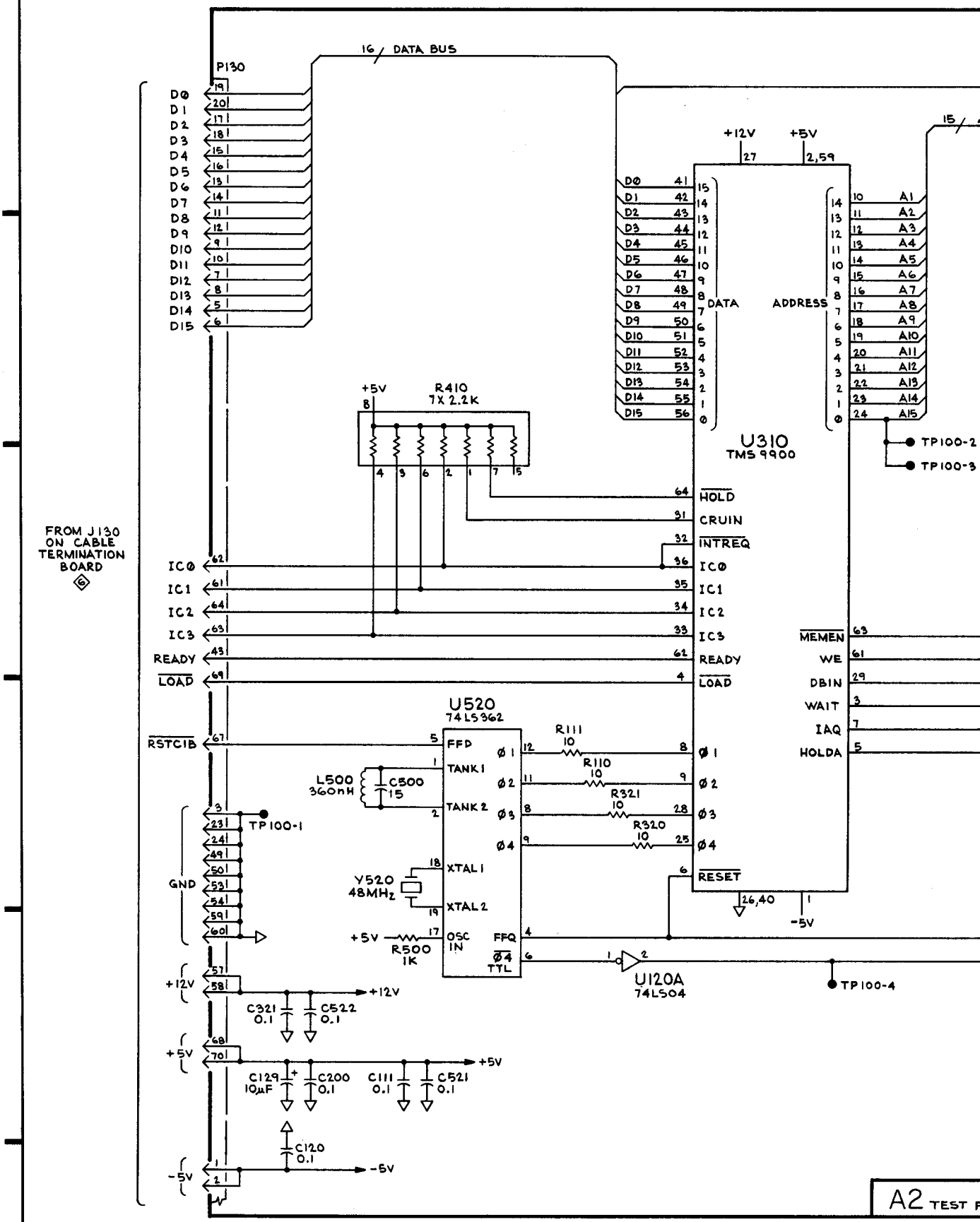


TEST PROCESSOR BOARD DIAGRAM 5

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C111	B5	B2
C120	B6	B3
C129	B5	B3
C200	B5	D2
C321	B5	E3
C500	B4	E3
C521	B5	F3
C522	B5	F3
L500	B4	G2
P130	A1	D4
P130	G1	D4
R110	C4	B2
R111	C4	B2
R320	C4	E3
R321	C4	E3
R410	B2	E2
R500	B5	F2
TP100	B4	A2
TP100	D2	A2
TP100	D3	A2
TP100	D5	A2
U120A	C5	A3
U200	E1	C2
U300	E2	C2
U310	D2	D2
U520	B4	G3
Y520	B4	F3



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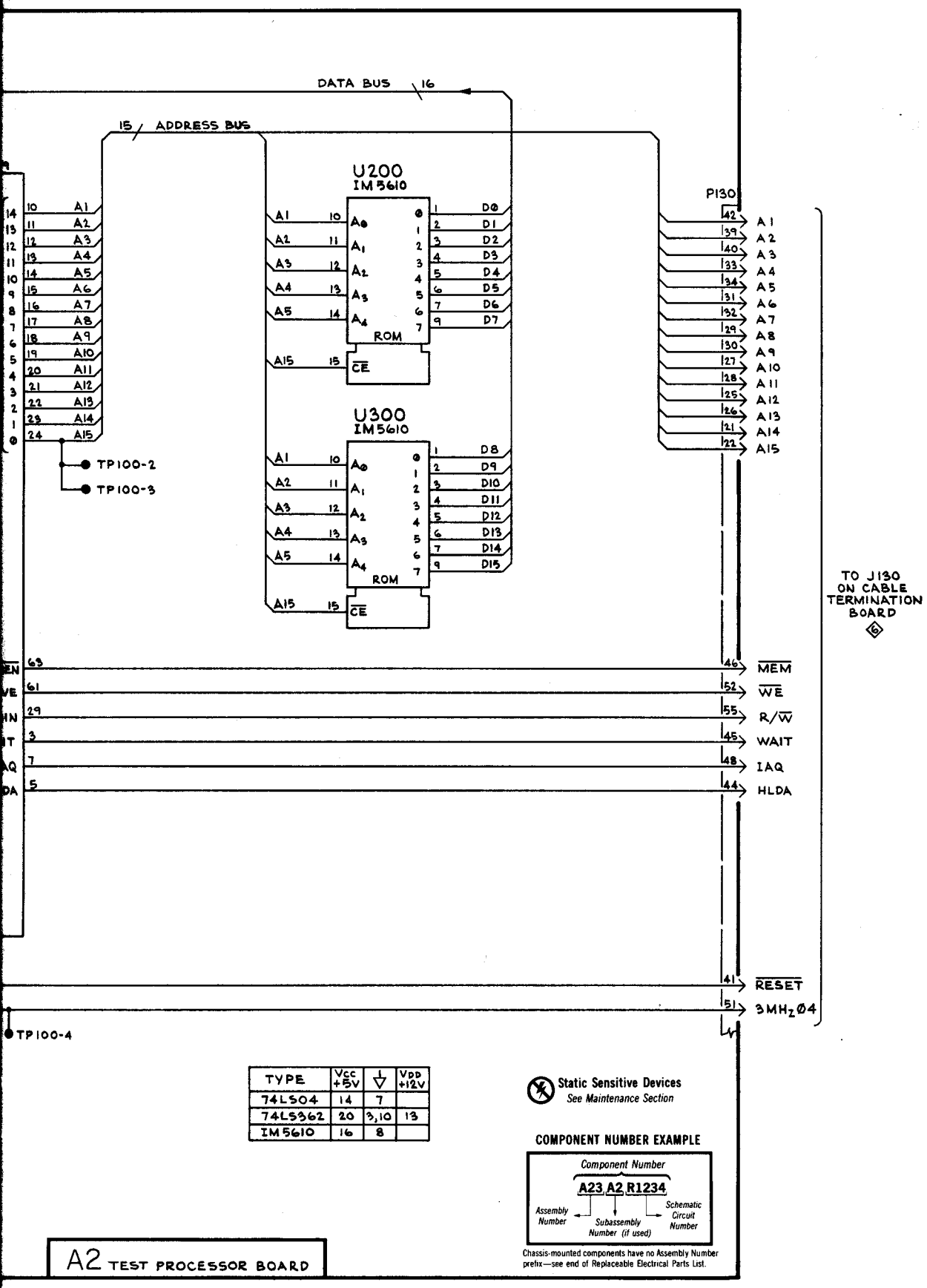


TYPE	Vcc +5V	⏚	VDD +12V
74LS04	14	7	
74LS362	20	3,10	13
IM5610	16	8	

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23,A2,R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

A2 TEST PROCESSOR BOARD

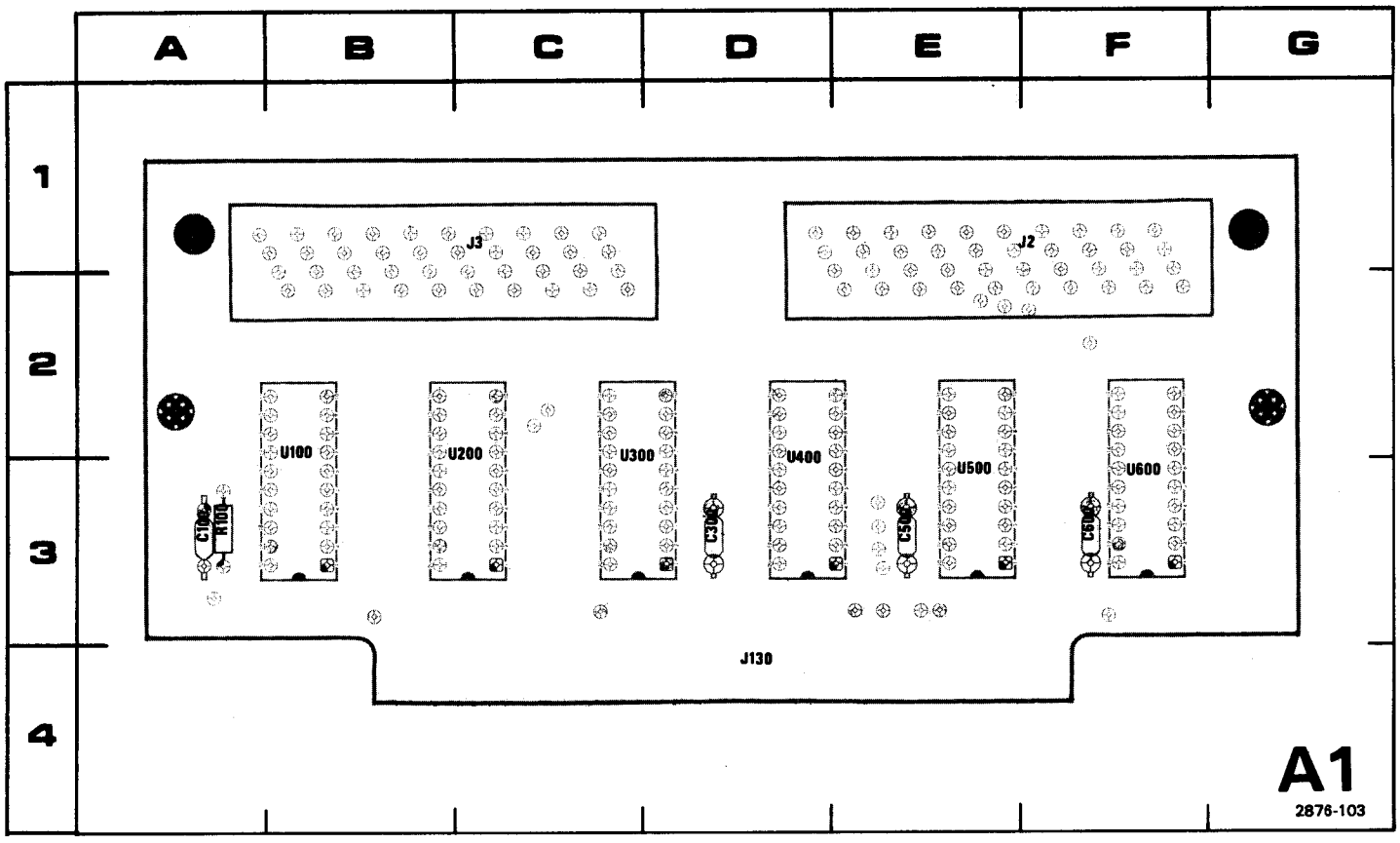
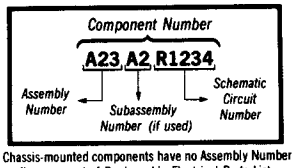


Figure 10-4. A1-Cable Termination circuit board assembly.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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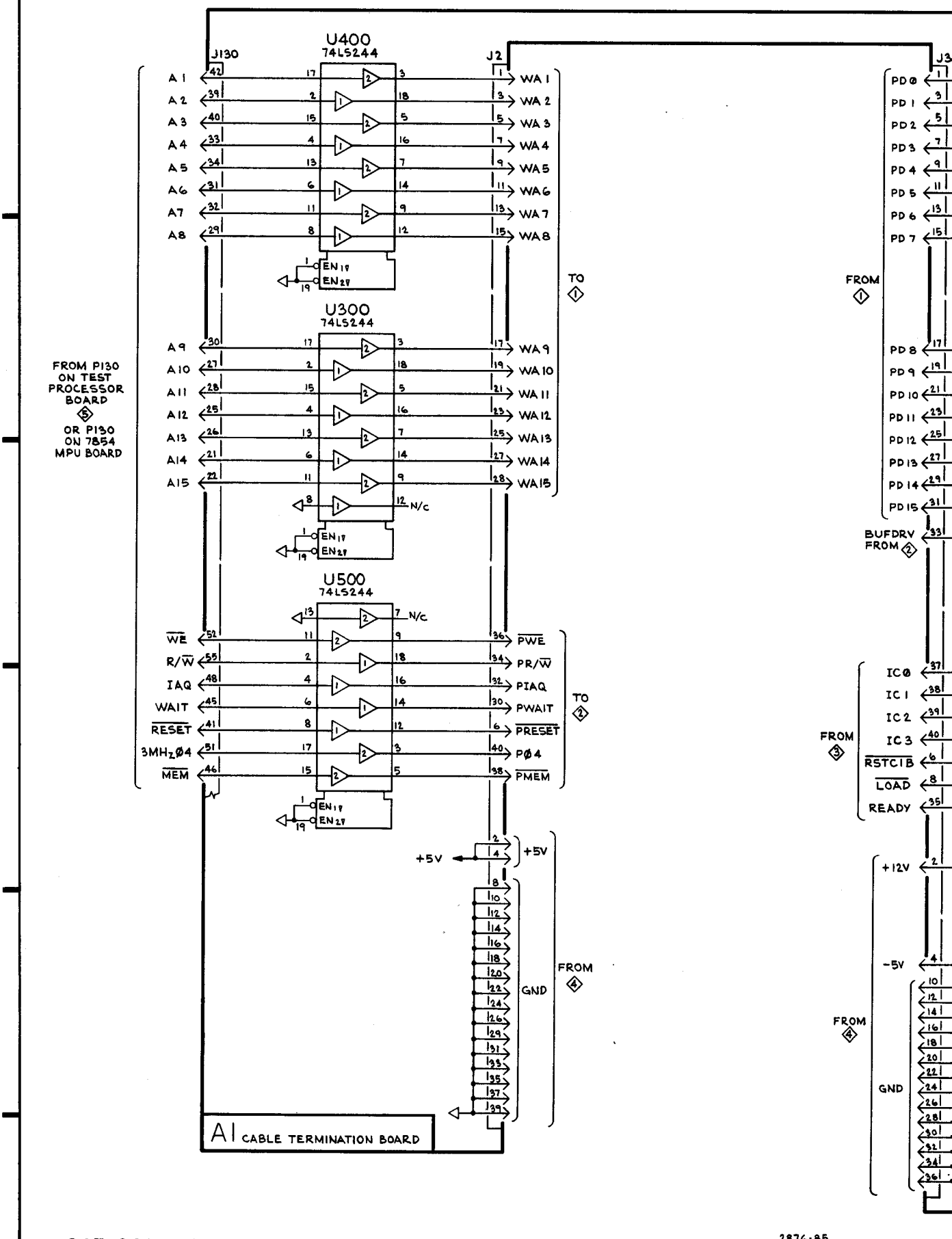
CABLE TERMINATION BOARD DIAGRAM 6

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	F5	A3
C300	F5	D3
C500	F5	G2
C600	F5	F3
J2	C1	F1
J3	E1	C1
J130	A1	D4
J130	F1	D4
R100	F2	A3
R200	E3	**
R201	E3	**
R600	E3	**
R601	E3	**
U100	F2	B2
U200	F1	C2
U300	B2	E1
U400	B1	D2
U500	B3	E3
U600	F3	F3

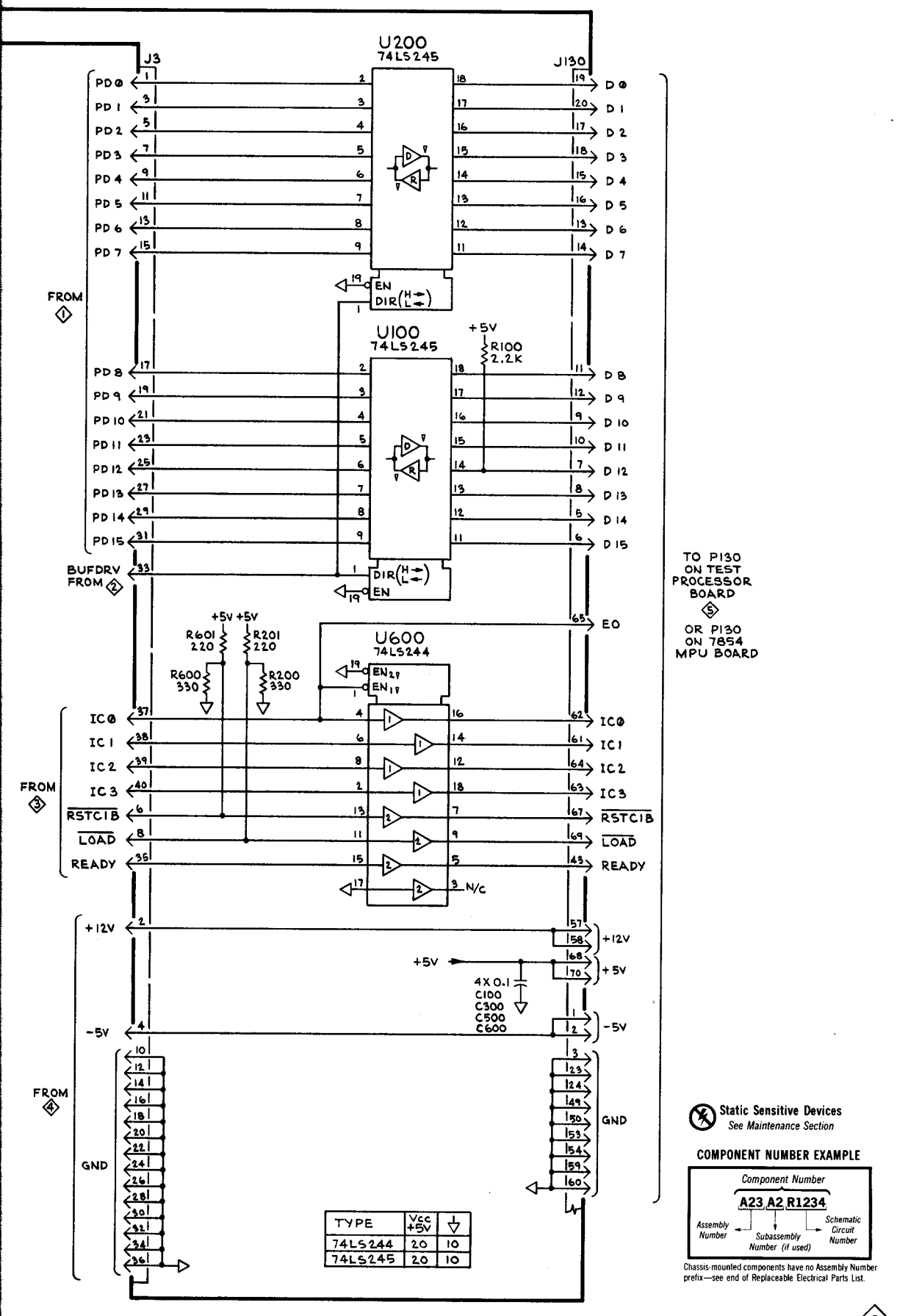
A1

2876-103



067-0911-00

2876-85



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

CABLE TERMINATION BOARD

6

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

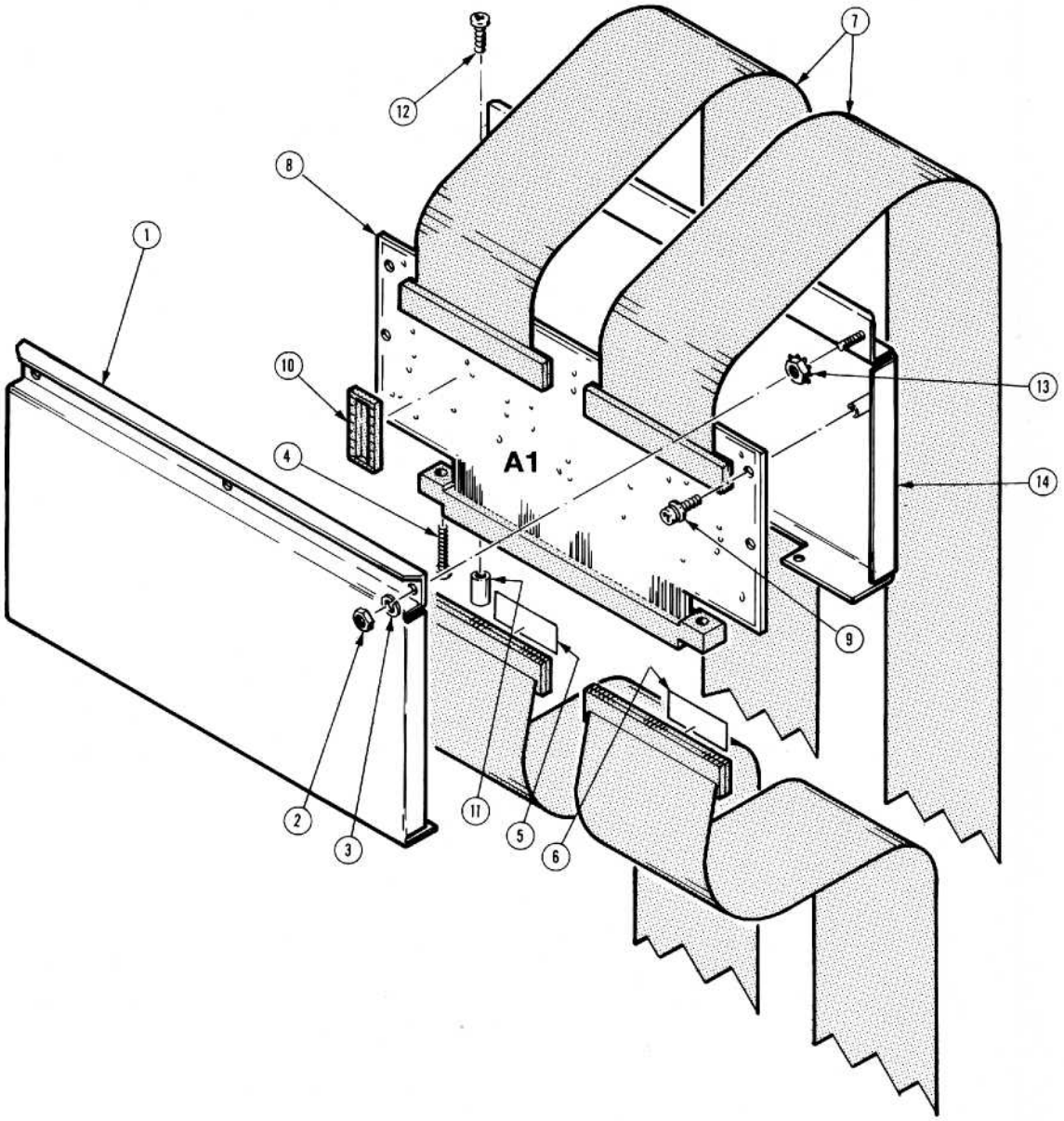
ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON-WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
06776	ROBINSON NUGENT INC.	800 E. 8TH ST., BOX 470	NEW ALBANY, IN 47150
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
82647	TEXAS INSTRUMENTS, INC., CONTROL PRODUCTS DIV.	34 FOREST ST.	ATTLEBORO, MA 02703
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-	067-0911-00			1		FIXTURE,CAL:DIAGNOSTIC PACKAGE	80009	067-0911-00
-1	380-0603-00			1		. HSG HALF,CONN:BACK	80009	380-0603-00
						(ATTACHING PARTS)		
-2	210-0406-00			3		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-3	210-0054-00			3		. WASHER,LOCK:SPLIT,0.118 ID X 0.212"OD STL	83385	OBD
-4	211-0014-00			2		. SCREW,MACHINE:4-40 X 0.50 INCH,PNH STL	83385	OBD
						- - - * - - -		
-5	334-3713-00			1		. MARKER,IDENT:MKD CONNECT TO J2	80009	334-3713-00
-6	334-3714-00			1		. MARKER,IDENT:MKD CONNECT TO J3	80009	334-3714-00
-7	175-2655-00			2		. CA ASSY,SP,ELEC:60.5 INCH LONG	80009	175-2655-00
-8	----- -----			1		. CKT BOARD ASSY:TERMINATION(SEE EPL)		
						(ATTACHING PARTS)		
-9	211-0116-00			2		. SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	OBD
						- - - * - - -		
	----- -----			-		. . CKT BOARD ASSY INCLUDES:		
-10	136-0634-00			2		. . SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	82647	CS9002-20
-11	129-0536-00			1		. SPACER,POST:0.3555 L,W/4-40 THD THRU	80009	129-0536-00
						(ATTACHING PARTS)		
-12	211-0008-00			1		. SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-13	210-0406-00			3		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-14	380-0602-00			1		. HSG HALF,CONN:FRONT	80009	380-0602-00
-15	----- -----			1		. CKT BOARD ASSY:TEST PROCESSOR(SEE EPL)		
-16	131-0608-00			4		. . TERMINAL,PIN:0.365 L X 0.25 PH,BRZ,GOLD PL	22526	47357
-17	136-0716-00			1		. . SKT,PL-IN ELEK:MICROCKT,64 CONT	06776	1CN649-S5-H6
-18	136-0260-02			2		. . SOCKET,PLUG-IN:16 CONTACT,LOW CLEARANCE	82647	C9316-18
-19	----- -----			1		. CKT BOARD ASSY:INTERFACE(SEE EPL)		
-20	136-0578-00			4		. . SOCKET,PLUG-IN:24 DIP,LOW PROFILE	73803	CS9002-24
-21	131-0608-00			82		. . TERMINAL,PIN:0.365 L X 0.25 PH,BRZ,GOLD PL	22526	47357
-22	105-0160-00			2		. . EJECTOR,CKT BD:WHITE PLASTIC	80009	105-0160-00
-23	214-1337-00			2		. . PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00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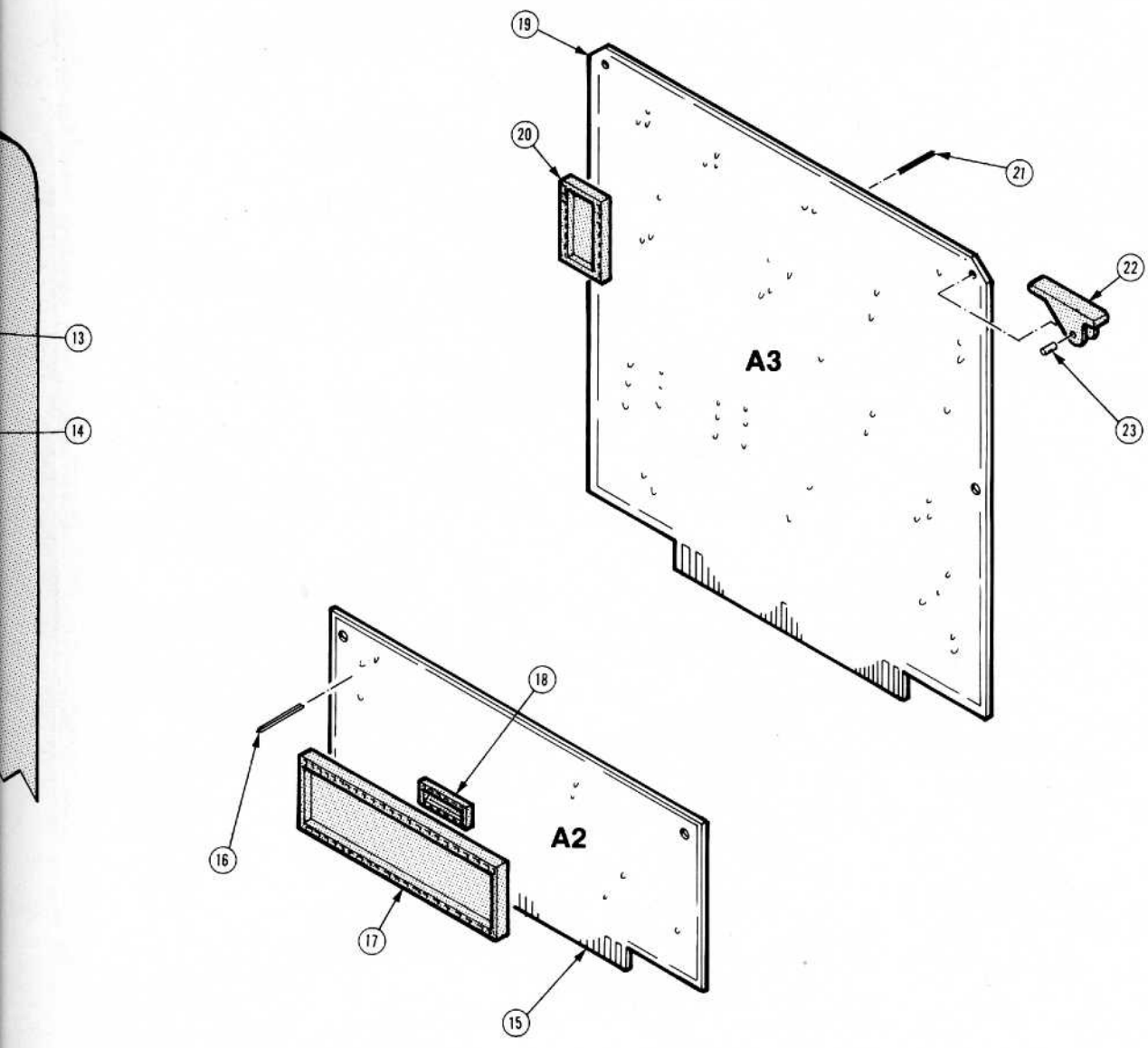
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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	070-2876-00			1		MANUAL,TECH:SERVICE	80009	070-2876-00

CUMULATIVE UPDATE POLICY

The manual "Signature Tables for 7854 Diagnostic Troubleshooting Using 067-0911-XX Diagnostic Test Interface", part number 070-2972-XX, should be inserted behind this tab. Upon receipt of a new signature table manual, the older manual should be discarded and replaced with the newer. Signature table manuals are of a cumulative nature and contain all previous signature versions (as indicated by the tabs).

Documents found helpful in troubleshooting the 7854 Oscilloscope may be inserted behind this tab. These may include:

067-0961-00 Diagnostic Memory Board manual
067-0912-00 Analog Test Board data sheet
067-0913-00 Extender Board data sheet
067-0914-00 Extender Board data sheet
067-0915-00 Extender Board data sheet

APPENDIX A

ERROR CODE SUMMARY

ERROR NO.	DESCRIPTION
01	Diagnostic System Self Test Error—refer to Error Codes 20 through 43 below.
02	Terminal Read Error—Framing Error
03	Terminal Read Error—Overrun Error
04	Input line length greater than 80 characters
05	Invalid parameter for command invocation
06	Invalid Command not in command tables
07	Invalid Numeric Input
10	Memory Write Error on Examine command
20	Self Test RAM Error
21	Self Test Interface Control Register Error
22	Self Test Maskable RAM Error
23	Self Test Breakpoint Error
24	Self Test RS232 Communication Error
25	Self Test Breakpoint Address Register Error
28	Self Test Microlab 1 Keypad Error
29	Self Test EPROM Error—U120 on 067-0911-XX
30	Self Test EPROM Error—U220 on 067-0911-XX
31	Self Test EPROM Error—U225 on 067-0911-XX
32	Self Test EPROM Error—U320 on 067-0911-XX
43	Self Test ROM ID Error (Int Vctrs Error)
44	7854 Ram Configuration Error
45	Specified RAM address block not installed
46	GPIB board not installed when GPIB Test invoked
51	ROM Error—U100 on 7854 ROM board
52	ROM Error—U110 on 7854 ROM board
53	ROM Error—U200 on 7854 ROM board
54	ROM Error—U210 on 7854 ROM board
61	EPROM Error—U200 on 067-0961-XX
62	EPROM Error—U210 on 067-0961-XX
63	EPROM Error—U220 on 067-0961-XX
64	EPROM Error—U230 on 067-0961-XX
65	EPROM Error—U100 on 067-0961-XX
66	EPROM Error—U110 on 067-0961-XX
67	EPROM Error—U120 on 067-0961-XX
68	EPROM Error—U130 on 067-0961-XX
69	EPROM Error—U400 on 067-0961-XX
70	EPROM Error—U410 on 067-0961-XX
71	EPROM Error—U420 on 067-0961-XX
72	EPROM Error—U430 on 067-0961-XX
73	EPROM Error—U300 on 067-0961-XX
74	EPROM Error—U310 on 067-0961-XX
75	EPROM Error—U320 on 067-0961-XX
76	EPROM Error—U330 on 067-0961-XX

INSTRUCTIONS FOR COMPLETING THE SOFTWARE/FIRMWARE PERFORMANCE REPORT

I. Please type or print clearly. Use a separate Software/Firmware Performance Report (SFPR) for each problem.

II. SECTION A
Fill in the serial number of the 7854 Oscilloscope the diagnostic firmware version (067-0961-) and the 067-0911- Diagnostic Test Interface version. With the 7854 ROM board installed, press the ID key on the 7854 and copy the entire line of Version information, beginning with TEK/7854.

III. SECTION B
Use the complete company mailing address. Include the name and phone number of the person reporting the error. Also, be sure to fill in the name of the person submitting the SFPR.

IV. SECTION C
Check the reason for report and whether the error is reproducible. We cannot fix a problem when we cannot reproduce the error condition.

V. SECTION D
Give a complete description of the system configuration on which the problem occurred. Include related peripherals, interfaces, options, special switch and/or strap settings and operating system.

VI. SECTION E
Describe the problem completely. Include any information which might help in evaluating the error with the SFPR. If you have determined a procedure to avoid the error condition, please include this procedure. If this problem prevents you from accomplishing any useful work with the product, please state this fact. Be sure to include with the SFPR any information (programs, listings, hard copies, etc.) which will help us duplicate your problem.

VII. SECTION F
This section is for use by Tektronix Lab Scopes Software Maintenance personnel. DO NOT WRITE IN THIS SPACE.

VIII. Mail **all** copies of the Software/Firmware Performance Report to:

TEKTRONIX, INC.
LAB SCOPES SOFTWARE MAINTENANCE
P.O. BOX 500
BEAVERTON, OREGON 97077

SEND TO: TEKTRONIX, INC.
LAB SCOPES SOFTWARE MAINTENANCE
P.O. BOX 500
BEAVERTON, OREGON 97077

7854/DIAGNOSTIC SYSTEM SOFTWARE/FIRMWARE PERFORMANCE REPORT

7854 OSCILLOSCOPE SERIAL # _____

(A) **LINE ONE OF 7854 DISPLAY WHEN ID KEY IS PRESSED (7854 ROM INSTALLED)** TEK/7854, _____

DIAGNOSTIC FIRMWARE VERSION 067-0961- _____

DIAGNOSTIC TEST INTERFACE VERSION 067-0911- _____

(B)
COMPANY NAME: _____
USER: _____
ADDRESS: _____
CITY: _____ STATE: _____ ZIP: _____
PHONE: _____ EXTENSION: _____

FORM SUBMITTED BY: _____ DATE: _____

REASON FOR REPORT
- ☐ Software/Firmware Error
- ☐ Documentation Error
- ☐ Suggested Enhancement

(C)
IS THE ERROR REPRODUCIBLE?
- ☐ Yes ☐ No
- ☐ Intermittent

(D) SYSTEM DESCRIPTION: (Hardware, software, firmware and host related to the problem)

(E) DESCRIPTION OF PROBLEM:

LIST ENCLOSURES:

INTERNAL USE ONLY

(DO NOT WRITE BELOW THIS LINE)

(F)

DATE RECEIVED _____

SPR # _____

SPR LOG

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.