LD110/111A
3½ Digit A/D Converter Set

Siliconix

FEATURES

- Buffered Reference Input
- MOSFET Input
- Auto-Zero System
- Auto-Polarity
- Over and Under Range Signals

BENEFITS

- High Gain Stability
- Reduced Signal Loading
- Reduced Offset and Drift Over Temperature
- Reduced External Parts Count
- Easily Interfaced

APPLICATIONS

- High Performance Digital Voltmeters
- Digital Panel Meters
- Digital Instrumentation Readouts
- μP A/D Interface Subsystem
- Auto-Zeroed Microvolt or Strain Guage Systems

DESCRIPTION

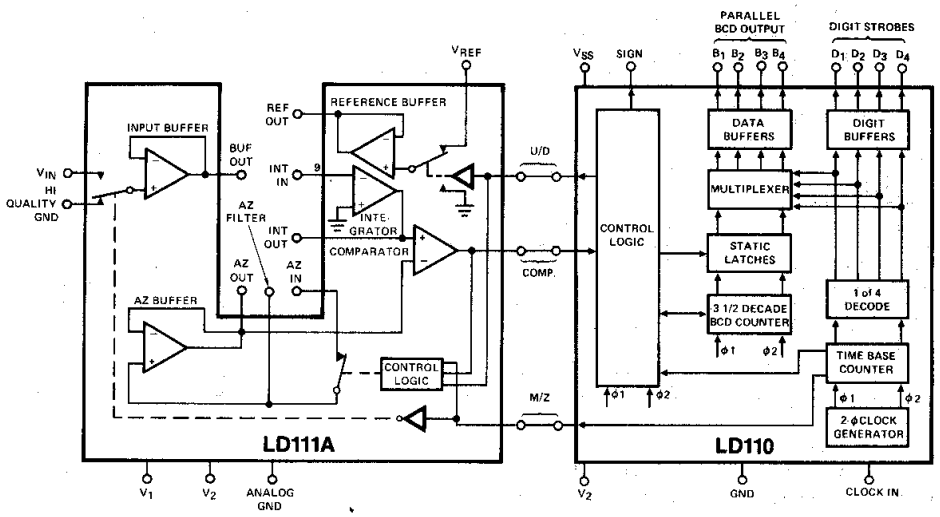
The LD110 and LD111A form a precision 3 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on Siliconix's "Quantized Feedback" technique, intrinsic features include auto-polarity, auto-zero, and ratiometric operation. Except for a stable reference, no critical components are required to achieve rated performance. The technique used offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts. Thus, critical, high resolution performance is not required of either the integrator or the comparator.

The monolithic LD111A high performance analog processor contains a bipolar comparator, a bipolar integrating amplifier, a bipolar reference amplifier, two MOSFET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. The high impedance input and reference buffer amplifiers eliminate source loading errors and provide the outstanding temperature coefficient inherent in this system. Break-before-make switch action insures that neither the analog input nor the reference voltage will be shorted to ground at any time.

The PMOS LD110 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3½ digits of BCD data as well as overrange, underrange and polarity information. Nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2 and 4.

Both devices are supplied in the 16-pin plastic DIP, and are specified for operation over the 0 to 70°C temperature range.

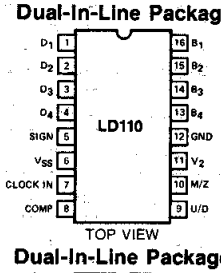
FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "0" AT U/D AND M/Z INPUTS.

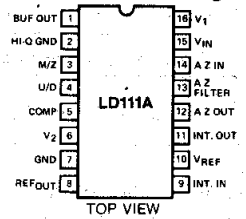
PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

Order Numbers:
LD110CJ and LD111ACJ
See Package 8

ABSOLUTE MAXIMUM RATINGS

I_{IN} (Pin 15, 2) ..... ±1 mA
$V_1 - V_2$ (LD111A) ..... 30 V
V_{SS} ..... 6 V
$V_{SS} - V_2$ (LD110) ..... 20 V
V On Any Pin Relative to V_{SS} (LD110) ..... 0.3 V to −20 V
V_{REF} ..... V_1

Operating Temperature ..... 0 to 70°C
Storage Temperature ..... −65 to 125°C
Power Dissipation (Package)* ..... 750 mW

*Device mounted with all leads welded or soldered to PC Board. Derate 6.3 mW/°C above 25°C.

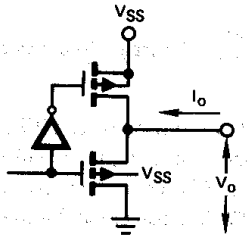
ELECTRICAL CHARACTERISTICS[1]

$T_A = 25°C$

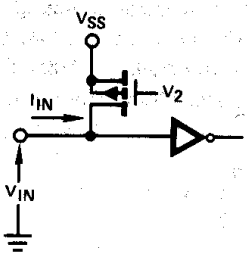
	PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE NOTED: $V_1 = +12$ V, $V_2 = -12$ V, $V_{SS} = 5$ V, $V_{REF} = 8.2$ V, $R_1 = 100K\ \Omega$	LIMITS MIN[2]	LIMITS TYP[3]	LIMITS MAX	UNIT
SYSTEM	Analog Input Range	V_{ANALOG}		−2 V		2 V	% rdg
	Linearity				0.02		
	Noise		Peak-to-Peak Noise Apparent When Going From One Steady Reading to Another		0.1		LSB
	Gain T.C.				5		ppm/°C
	Normal Mode Rejection	NMR	$f_{noise} = 60$ Hz		40		dB
	Clock Frequency	f_{IN}	50% Duty Cycle		30.7	250	kHz
	ON Resistance, Auto Zero Switch	$r_{DS(on)}$	$V_{AZ(in)} = -4.0$ V, $I_S = -30\ \mu A$		6	20	K Ω
INPUT	Clock Input Current, Low	I_{CL}	$V_{CLOCK\ in} = 0.4$ V	−500			μA
	Input Bias Current	I_{IN}			4		pA
	Comp. LD110	I_{INL}	$V_{IN} = -12$ V	−1500	−700	−50	μA
AMP	Reference Buffer	I_{source}	V_{INL} (U/D) = 0.8 V, $V_{OUT} = 0$		−800	−400	μA
	AZ Buffer	I_{sink}	$V_{AZ} = -4$ V, $V_{OUT} = 0$ V		800		
	Input Buffer	I_{sink}	$V_{IN} = -2$ V, $V_{OUT} = 0$ V	400	800		
	Input Buffer	I_{source}	$V_{IN} = 2$ V, $V_{OUT} = 0$ V		−100	−50	
	AZ Buffer	V_{offset}	$V_{OUT} = 0$ V	−100		100	mV
OUTPUT	Measure/Zero Voltage, Low	V_{OL1}	$I_{OL} = 150\ \mu A$			0.6	V
	Measure/Zero Voltage, High	V_{OH1}	$I_{OH} = -200\ \mu A$	2.4			
	Up/Down Logic Voltage, Low	V_{OL2}	$I_{OL} = 250\ \mu A$			0.6	
	Up/Down Logic Voltage, High	V_{OH2}	$I_{OH} = -200\ \mu A$	2.4			
	Analog Comparator Voltage	V_{OH3}	$I_{OH} = -100\ \mu A$	2.4			
	Digits, Bits, Voltage, Low	V_{OL3}	$I_{OL} = 1.6$ mA			0.6	
	Sign Voltage, Low	V_{OL4}	$I_{OL} = 1.6$ mA			0.65	
	Data Bits Voltage, High	V_{OH4}	$I_{OH} = -200\ \mu A$	2.4			
	Digits, Sign Voltage, High	V_{OH5}	$I_{OH} = -800\ \mu A$	2.4			
SUPPLY	V_1 Supply Current, LD111A	I_1			2.2	4	mA
	V_2 Supply Current, LD111A	I_{2A}		−4	−1.8		
	V_2 Supply Current, LD110	I_{2D}		−23	−17		
	V_{SS} Supply Current, LD110	I_{SS}			17.4	24	
	Power Supply Rejection Ratio, V_1	$PSRR_1$		80	85		dB
	Power Supply Rejection Ratio, V_2	$PSRR_2$		60	65		
	Reference Voltage Rejection		$R_{REF} = R_2 = 100K\ \Omega$, $V_{IN} = 2$ V		1		%Δrdg/ ΔV_{REF}

NOTES:
1. Refer to PROCESS OPTION FLOWCHART for additional information.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

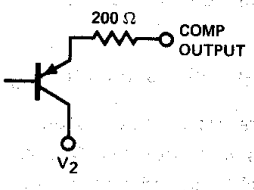
INPUT/OUTPUT SCHEMATICS



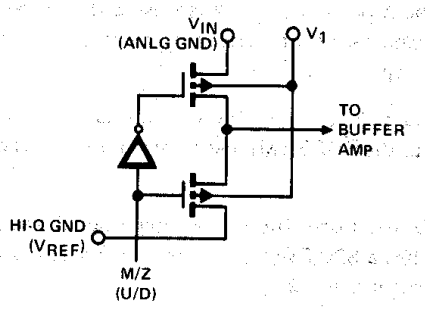
LD110 OUTPUT BUFFERS
(Digits, Bits, Sign, M/Z, U/D)



LD110 COMPARATOR, CLOCK INPUTS



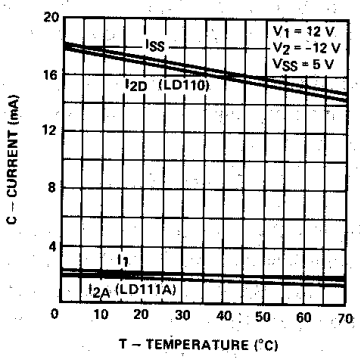
LD111A Comparator Output



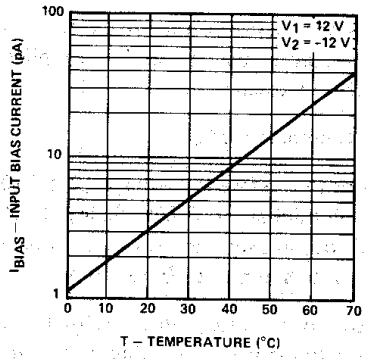
LD111A Inputs (V_{IN}, V_{REF})

TYPICAL CHARACTERISTICS

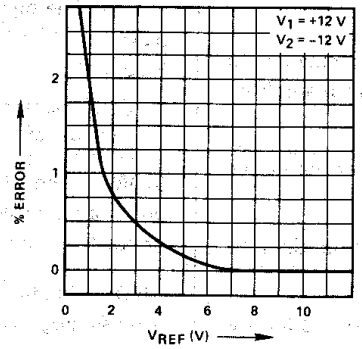
Supply Currents vs Temperature



Input Bias Current vs Temperature



Ratio Operation
(V_{IN}/V_{REF} = Constant)



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DESCRIPTION OF PIN FUNCTIONS—LD111A

BUF OUT – The output of this unity gain input buffer amplifier is applied to the integrator summing node through a scaling resistor R_2. The value of this resistor is typically 10K Ω for a 200.0 mV full scale and 100K Ω for a 2.000 V full scale. The digital output is inversely proportional to the value of this resistor.

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \times \frac{R_1}{R_2} \times 8192$$

HI-QUALITY GND – This pin, typically connected to a High Quality Ground point for single ended inputs *can be used as the inverting input for differential signals.* The digital output will be $V_{IN} - V_{HI\text{-}Q}$. When using this differential mode, it is important that resistor R_3 be less than resistor R_2 for proper operation.

M/Z – Measure/Zero Logic Input. Internal level shifting drivers operate the PMOS switches in response to this digital signal.

U/D – Up/Down Logic Input. The logic signal applied to this pin operates a SPDT switch to provide Quantized pulses of charge to the integrator.

COMP – This analog comparator output is an open collector configuration which goes to V_2 when "low."

V_2 – Negative Supply Voltage. Recommended level is –12 V ±10%.

GND – Analog Processor Ground. Should be kept separate from Digital Grounds.

REF_{out} – This buffered voltage output of the SPDT U/D switch, converted to a current by resistor R_1, supplies the reference current to the integrator.

INT. IN – Integrator Summing Node.

V_{REF} – A stable positive reference voltage (2 to 10 V) applied to this pin is the standard to which the input voltage V_{IN} is measured. Ratio measurements can be made by applying a variable to this input (1.0 to 10 V).

INT. OUT – The output of the integrating amplifier is made available for application to the Auto-Zero amplifier by means of resistor R_4.

AZ OUT – The output of the unity gain Auto-Zero amplifier provides a second negative reference current to the integrator through resistor R_3.

AZ FILTER – The Auto-Zero Capacitor (C_{AZ}) connected to this pin stores D.C. voltage components to balance amplifier offset and drift components.

AZ IN – This input is switched into the AZ filter during the zeroing interval.

V_{IN} – Analog Voltage Input. The A/D System digitizes the voltage appearing at this input.

V_1 – Positive Supply Voltage. The recommended level is +12 volts ±10%.

DESCRIPTION OF PIN FUNCTIONS — LD110

V_{SS} – Positive Supply Voltage. Recommended level is +5 V ±10%.

V_2 – Negative Supply Voltage. Recommended level is –12 V ±10%.

CLOCK IN – This input accepts a TTL or MOS level clock to drive the synchronous digital circuitry. Acceptable duty cycles on the external clock range from 30% high, 70% low to 70% high, 30% low for clock frequencies from 2 kHz to 250 kHz. Although any clock frequency between 2 kHz and 250 kHz may be used, clock frequencies that are integer divisions of $2048F_L$ ($F_{IN} = 2048F_L/n$, n = 1, 2, 3, . . . , 51), (F_L = Line Frequency) provide measure and zero periods that are integer multiples of the line frequency period ($T_{zero} = n/F_L$, $T_{measure} = 2n/F_L$). Line frequency interference is minimized by the selection of one of these 51 frequencies.

This input has an active pull-up to V_{SS}.

M/Z – Measure/Zero Logic Output. This 0 to 5 volt logic output successively provides Autozero and Measurement intervals of 2048 and 4096 clock periods respectively. This output is compatible with CMOS logic and directly interfaces with the LD111A analog processor.

U/D – Up/Down Logic Output. This output has logic levels of 0 and +5 volts to provide pulse-width modulation of the reference current when used with the LD111A analog processor. This output is CMOS compatible.

COMP – Analog Comparator Input. This input has an active pull-up to V_{SS} for a comparator "high" state. This pin must be pulled down to V_2 for a "low" comparator state.

An End-of-Conversion Signal can be decoded from the three interconnecting logic lines (M/Z, U/D, Comp) using the following CMOS logic.

$$\overline{M/Z + U/D + Comp} = E.O.C.$$

B_1, B_2, B_3, B_4 – BCD Data Bit Output. B_4 represents the most significant bit and B_1 the least significant bit of the BCD output. Bit 4 of digit 4 goes high for an underrange condition (less than 100 counts). These outputs are compatible with 1 standard TTL load.

MUX Underrange = $B_4 \times D_4$ (5% of full scale)

D_1, D_2, D_3, D_4 – Digit Strobe Outputs. D_4 is the most significant and D_1 the least significant digit of the 3 1/2 digit output. The digit strobes are each selected in turn when the BCD data bits for that digit appear at the bit outputs (see Figure 4).

MUX Overrange = $\overline{D_1 + D_2 + D_3 + D_4}$
(100% of full scale, count ≥ 2000)

SIGN – Sign of Analog Input Polarity. This TTL level output is a static signal which is either 0 or V_{SS} for a negative or positive input polarity respectively.

GND – Digital Processor Ground. Should be kept separate from Analog Grounds. Common connection should be made at the power supply.

FUNCTIONAL OPERATION

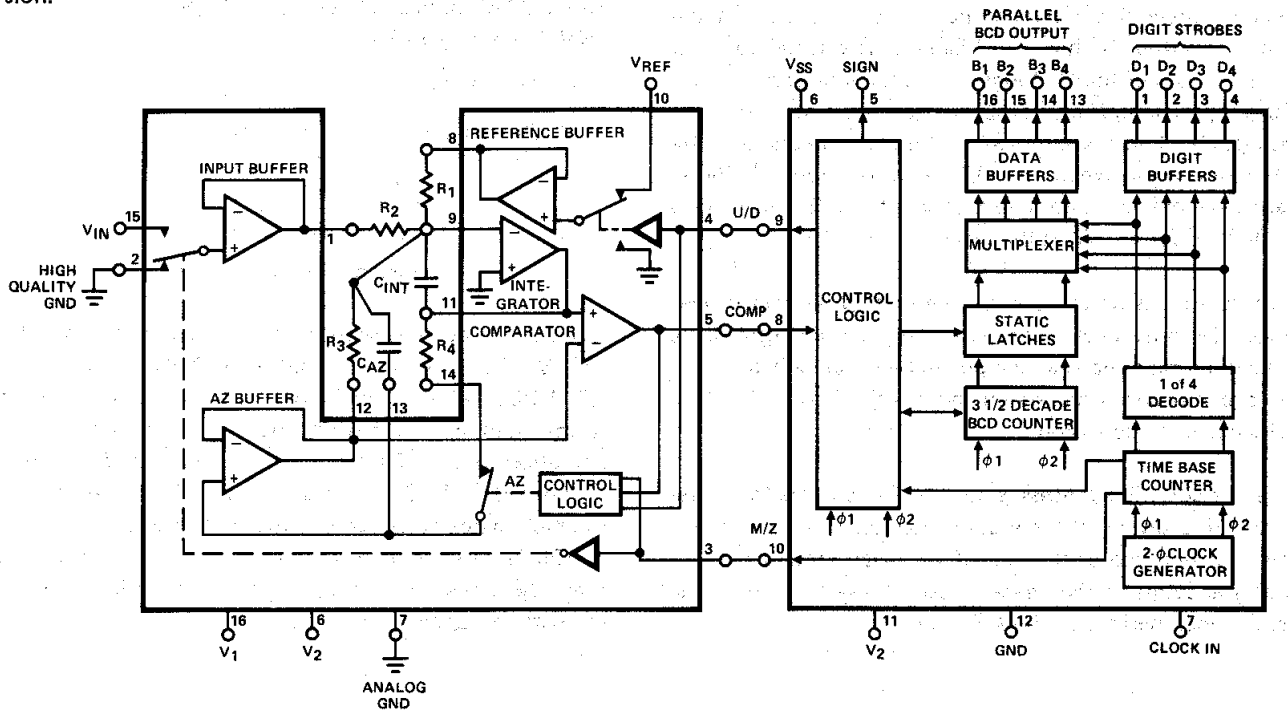
The Connection Diagram of Figure 1 should be referred to along with the timing diagrams of Figures 2, 3, and 4 in this discussion of functional operation.

Time Base Counter: An external clock signal using either TTL or MOS logic levels drives a 2-ϕ clock generator on the synchronous digital chip. The clock frequency is divided by the time base counter into sampling intervals of 6144 pulses of which 4096 constitute the measurement interval/and 2048 the auto-zero interval. Intermediate frequency divisions are utilized by both the control logic and the 1 of 4 decoder for the digit enables and bit scan.

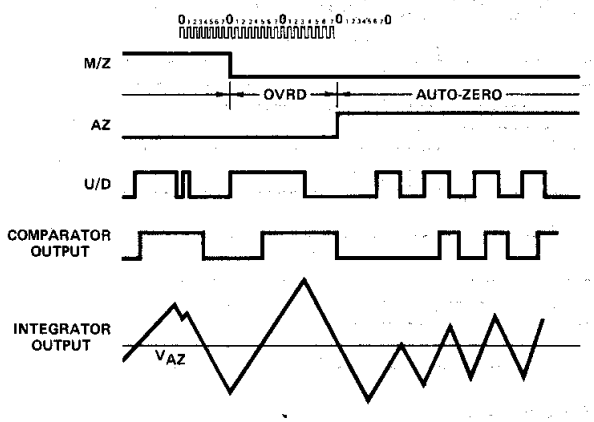
AUTO-ZERO INTERVAL

The Auto-Zero interval provides a means to null out the offset voltages of the amplifiers used in the LD110/LD111A system. In addition, it automatically establishes a second tracking reference voltage necessary for bipolar A/D conversion.

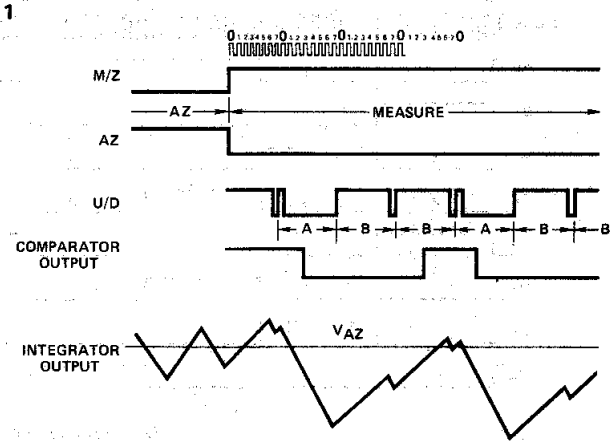
The Auto-Zero sequence is initiated when the M/Z (Measure/Zero) signal switches the input buffer amp to analog ground. After a brief count-correcting override period, the AZ switch is closed connecting the AZ amplifier and Integrator together in a closed-loop second-order system. During this time the control logic ignores the comparator output and pulses the U/D switch at a 50% duty cycle of 4 clock periods "Up" and 4 "Down" (see Figure 2). Equilibrium of this closed-loop system is attained when the average currents through R_1 and R_3 are equal and opposite. This is achieved when V_{AZ}, the Auto-Zero voltage, is equal to $-\frac{1}{2} V_{REF}$ ($R_1 = R_3$). Establishing V_{AZ} and storing it on C_{AZ} gives the U/D logic the capability of switching either a + or – reference current to the integrator during conversion. Thus when U/D is "Up," $I_1 + I_3 = -V_{REF}/2R_1$ and when U/D is "Down," $I_1 + I_3 = V_{REF}/2R_1$. The Auto-Zero interval is of sufficient duration to insure that V_{AZ} will be well established.



Connection Diagram
Figure 1



Auto-Zero Timing
Figure 2



Measure Interval Timing
Figure 3

MEASUREMENT INTERVAL

The "Quantized Feedback" conversion system is characterized by a single phase Digitization interval in which a digital control system feeds back quantized units of charge in response to the sampled state of an analog comparator. These quanta of charge balance the charge being supplied to the integrator by the analog voltage. The magnitude ($V_{REF}/2R_1$ x $6/f_{clock}$) of the Quantized charge being fed back and its sign (+ or –) arise from the fact that the control logic has two U/D duty cycles available during the Measure interval as shown in Figure 3.

The U/D logic is "up" one clock cycle and "down" 7 cycles for a high comparator output in the clock cycle preceding a set of 8 cycles. This will be designated duty cycle "A." With a low comparator output in clock cycle number 7 the U/D logic will be "up" for 7 cycles and "down" for 1 cycle in the following 8 clock cycles. This is duty cycle "B." The effect of these two reference current duty cycles on the integrator output is shown in Figure 3. It can be seen that the "up" state of the U/D logic drives the integrator output voltage up. The up/down BCD counter increments by each clock pulse when the U/D logic is "up" and decrements by each clock pulse when the U/D logic is "down." Consequently the net count goes up 6 counts for a "B" duty cycle and down 6 for an "A" duty cycle.

Input polarity is determined by the first appearance of two consecutive duty cycles of the same type. The control logic would determine the analog input to be negative if two "A" duty cycles occur in succession and positive if two "B" duty cycles occur in succession.

Since the counting process is done by increments (or decrements) of 6 during the measure interval, a short override interval is required at the end of the Measurement to "fine tune" the count to the nearest LSB. This occurs within the first 32 clock periods of the AZ interval.

Following the count correcting override sequence; the contents of the BCD counters and sign flip-flop are loaded into the internal latches. Counter states of less than 100 or greater than 1999 are decoded as underrange or overrange conditions respectively. The underrange signal is forced on Bit 4 during D_4 time. The overrange signal will be used to blank the display during the zero interval giving a visual overrange cue by means of a blinking display.

The BCD data stored in the latches is continuously scanned every 32 clock periods (8 clock times per digit). This data format is shown in Figure 4. Sign information is available as a static signal on a separate pin (high for +, low for –).

The BCD data output is an interlaced scan of digits 1, 3, 2, and 4 where digit 4 is the most significant digit. All outputs are active high and TTL compatible.

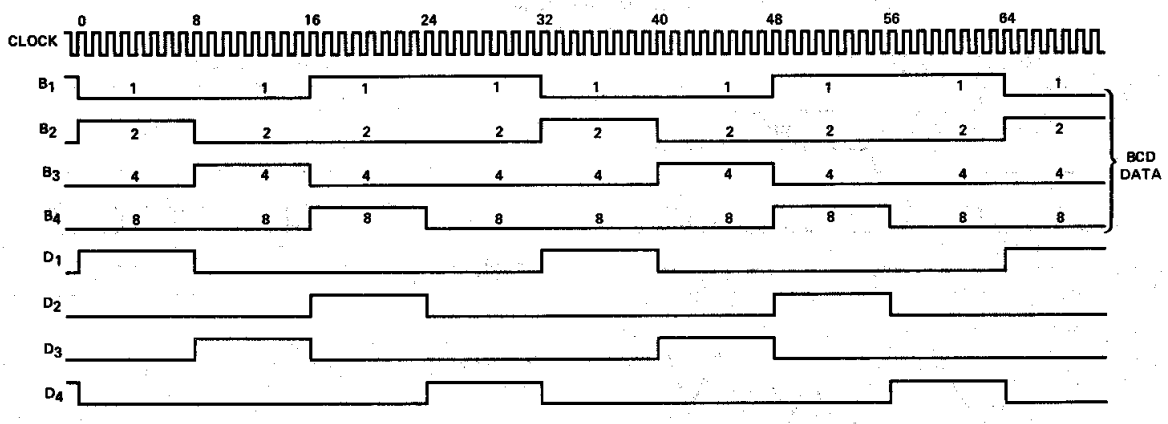
APPLICATIONS INFORMATION (Refer to Figure 5)

1. Power Supplies

a) The recommended supply voltages are:

V_1 = 12 V ±10%
V_2 = –12 V ±10%
V_{SS} = 5 V ±10%
V_{REF} = 2.00 V to 10 V

Operation is possible with V_1 and V_2 supplies from ±9 V to ±15 V. These minimum voltages (±9 V) require that the LD110/LD111A system be operated on the 200.0 mV scale to maintain input buffer linearity. It should be realized that operation below ±10.8 volts is not guaranteed. V_2 voltages greater than –13.2 V allows the LD110 to dissipate a considerable amount of power (400 mW, warm to the touch). A 150 Ω resistor in series with pin 11 of the LD110 will limit the current resulting in cooler operation and longer life with large values of V_2.



Data Output Format (Output = 1492)
Figure 4

APPLICATIONS INFORMATION (Cont.)

2. Input Protection. Under normal operating conditions the inputs of the LD111A should not be exposed to a voltage exceeding either V_1 or V_2 (see absolute maximum ratings). In many applications however, such as a DMM/DVM, the V_{IN} or V_{REF} input may have a high voltage source connected which is capable of supplying destructive currents into the LD111A. To prevent such an occurrence, a current limiting resistor should be placed in series with the appropriate input pin. The 1 mA maximum current rating should be observed. A 1M Ω resistor in series with pin 15 of the LD111A would offer input protection up to a 1000 V overvoltage.

3. Operation Over the Full Sampling Range. Any sampling rate from 1/3 to 40 samples/second can be accommodated by simply changing the values for C_{INT} and C_{AZ} (R_3 and R_4 will remain as shown in Figure 5).

To find the proper value for C_{INT} and C_{AZ}, (shown as C_1 and C_2 respectively on Figure 5) find the needed clock frequency for a specific sampling rate from the following relationship.

$$f_{clock} = \text{Sampling Rate} \times 6144$$

Once the clock frequency has been determined, the values for C_{INT} and C_{AZ} can be found.

$$C_{INT} \cong \frac{200\,\mu\text{F/sec}}{f_{clock}}$$

$$C_{AZ} \cong 10\,C_{INT}$$

4. Resistor Selection. Resistor R_2 is the scaling resistor and is selected to provide 10 nA per LSB into the integrator summing junction. Thus,

$$R_2 = \frac{V_{IN(\text{Full Scale})}}{(2000\ \text{Counts})\ (10\ \text{nA/Count})}$$

$$= 100\text{K}\ \Omega\ (2.000\ \text{V Scale})$$

$$= 10\text{K}\ \Omega\ (200.0\ \text{mV Scale})$$

$$= 1\text{K}\ \Omega\ (20.00\ \text{mV Scale})$$

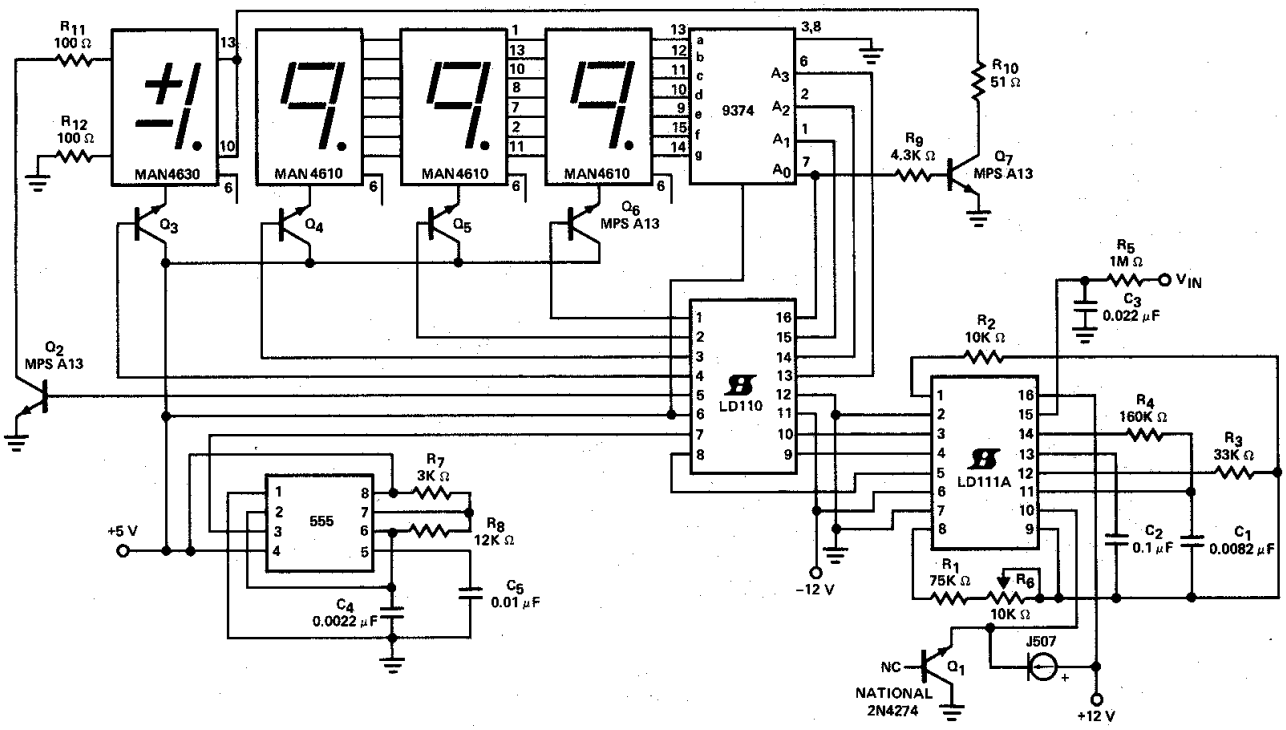
The reference resistor R_1 is chosen to satisfy the relationship

$$R_1\ (\text{Trimmed}) = \frac{V_{REF}}{81.92\ \text{V}}\ \text{M}\Omega$$

5. 20.00 mV Scale (10 μV Resolution). The improved noise performance of the LD111A allows it to be used in a 20.00 mV DPM when R_2 is selected to be 1K Ω. This high resolution range, while useful, does not have the same degree of zero and LSD stability as the 200.0 mV and 2.000 V ranges. Extreme care in layout is required to minimize noise and offsets at V_{IN} and Hi-Q GND.

6. Ratio Operation. The LD110/LD111A is a ratio measuring system — the output being

$$\text{Count} = \frac{V_{IN}}{V_{REF}}\ \frac{R_1}{R_2}\ 8192$$

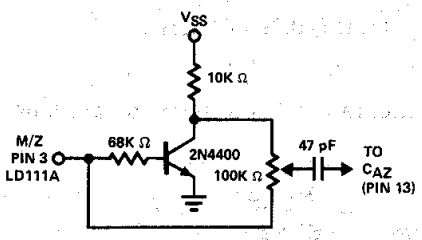


3½ Digit DVM (±200.0 mV) Common Anode Display
Figure 5

APPLICATIONS INFORMATION (Cont.)

The high impedance input and reference buffer amplifiers offer a system with ratio operation and minimal source loading. The ratio curve shown with the typical characteristics illustrates the ratio performance.

7. Zero Adjustment. The LD110/LD111A converter set is an Auto-zeroing system. Many applications exist, however, in which a means of nulling out external offsets is needed. The circuit of Figure 6 provides this offset nulling feature.

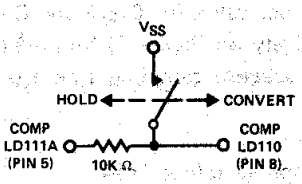


Offset Nulling Circuit
Figure 6

8. Replacing the LD111 with the LD111A. The LD111A offers a significant improvement in linearity, noise and temperature stability over the LD111. It also eliminates the need for the integrator clamp zener required on the LD111. The LD111A is a plug-in replacement for the LD111.

9. Data Valid (End-of Conversion). The BCD data from the LD110 is changed only once per conversion, at the end of the override interval. The 3½ digits of data are then repeatedly multiplexed out during the rest of the zero and for the full Measure Interval. Since the data cannot change during the Measure Interval and since the Measure Interval occurs once each sampling interval, this high state of the M/Z line can be used as a Data Valid or End-of-Conversion signal.

10. "Hold". The last conversion of the LD110/LD111A may be held indefinitely by means of the added circuitry shown in Figure 7. Forcing the comparator input of the LD110 to the high state eliminates any future data transfers. The resistor protects the LD111A comparator output. Opening the connection to V_{SS} allows normal comparator action and data transfer. The first conversion after a "hold" will always be in error since the AZ voltage has not been maintained during "hold".



"Hold" Circuit
Figure 7